System-on-a-Chip, 66MHz Octal Pin Electronics w/PMU

ISL55169

ISL55169 is a highly integrated system on a chip (SOC) pin electronics solution aimed at incorporating every analog function (with some digital support functionality) required on a per channel basis for Automated Test Equipment (see figure below.) The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.

Features

- 66MHz
- 7.5ns Minimum Pulse Width
- Pin Electronics Driver
  - 2 Level Driver with On-Chip Buffers
  - 8V Driver Output Swings
  - Extremely Low Leakage over a 16V HiZ Range
- Pin Electronics Comparator
  - Extremely Low Leakage over a 16V Input Range
  - 16V Comparator Input Voltage Range
- Per-Chip PMU
  - FV, FI, MV, MI
  - 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
  - 12V Super Voltage Capability
- Deskew
  - Propagation Delay Adjustment
  - Falling Edge Adjustment (up to ±5ns range)
  - Auto Calibration via PLL
- On-Chip DC Levels
  - 4 Levels/Channel
  - 8 Levels/Central PMU
  - 16 Bits per Level
  - 16 Bit per Level Offset Correction
  - 16 Bit per Level Gain Correction
- 3 Bit Serial CPU Port
  - Load Internal Registers and Memory
  - Read Back Internal States
- Flexible Digital Inputs and Outputs
  - Adjustable Threshold for High Speed Inputs
  - 50Ω/100Ω Input Termination Options
  - 50Ω Serial Terminated High-Speed Comparator Outputs
- Package/Power Dissipation
  - 128 Lead, 14mm x 20mm MQFP with Heat Slug
  - Pdq ≤ 500mW/Channel; Pdq ≤ 4.0W/Chip

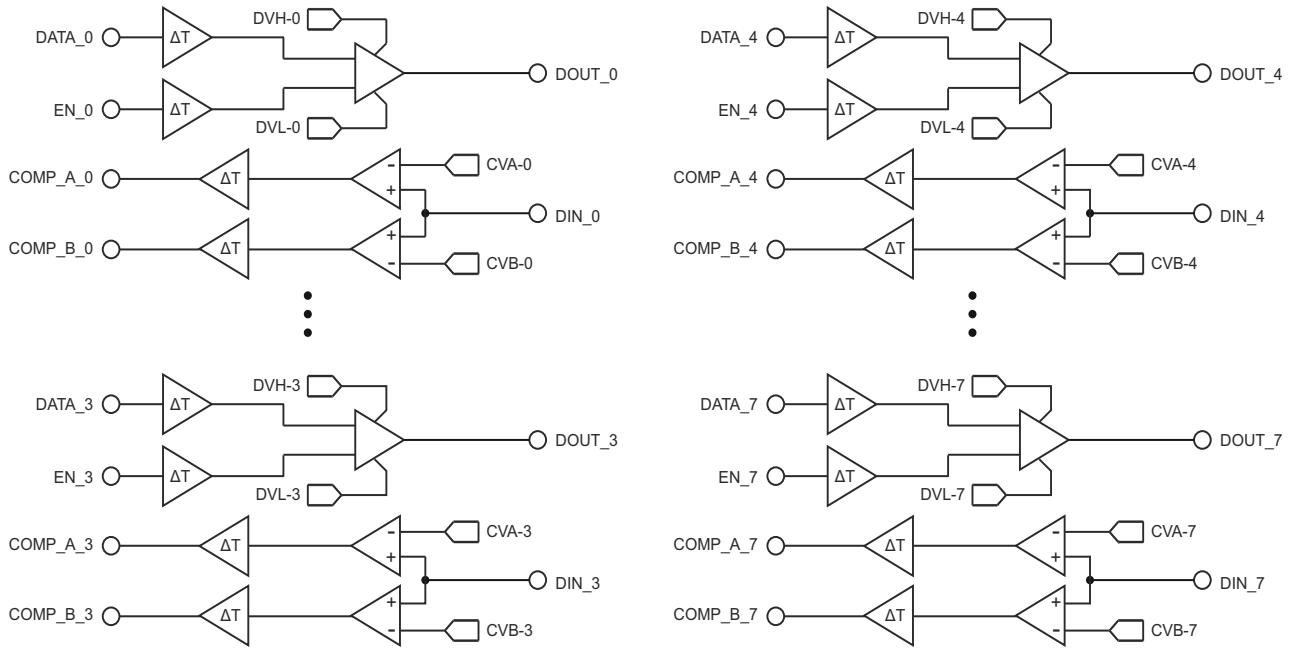


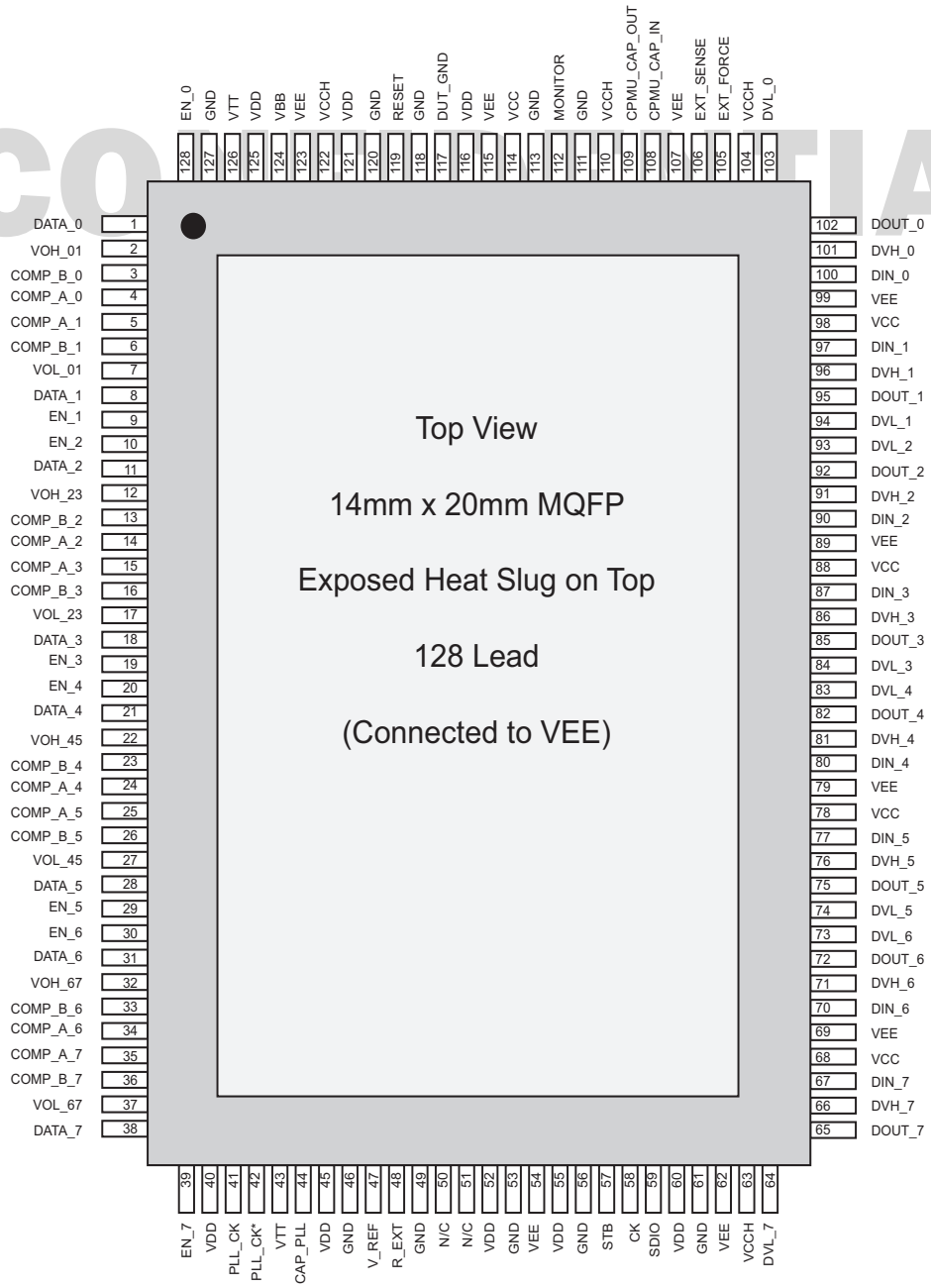
Table of Contents

Pin Descriptions

Pin #	Pin Name	Description
102, 100 1, 128 4, 3 101, 103	DOUT_0, DIN_0 DATA_0, EN_0 COMP_A_0, COMP_B_0 DVH_0, DVL_0	Channel 0 driver output and comparator input pins. Channel 0 driver data and enable inputs. Channel 0 comparator outputs. Channel 0 driver high and low levels.
95, 97 8, 9 5, 6 96, 94	DOUT_1, DIN_1 DATA_1, EN_1 COMP_A_1, COMP_B_1 DVH_1, DVL_1	Channel 1 driver output and comparator input pins. Channel 1 driver data and enable inputs. Channel 1 comparator outputs. Channel 1 driver high and low levels.
92, 90 11, 10 14, 13 91, 93	DOUT_2, DIN_2 DATA_2, EN_2 COMP_A_2, COMP_B_2 DVH_2, DVL_2	Channel 2 driver output and comparator input pins. Channel 2 driver data and enable inputs. Channel 2 comparator outputs. Channel 2 driver high and low levels.
85, 87 18, 19 15, 16 86, 84	DOUT_3, DIN_3 DATA_3, EN_3 COMP_A_3, COMP_B_3 DVH_3, DVL_3	Channel 3 driver output and comparator input pins. Channel 3 driver data and enable inputs. Channel 3 comparator outputs. Channel 3 driver high and low levels.
82, 80 21, 20 24, 23 81, 83	DOUT_4, DIN_4 DATA_4, EN_4 COMP_A_4, COMP_B_4 DVH_4, DVL_4	Channel 4 driver output and comparator input pins. Channel 4 driver data and enable inputs. Channel 4 comparator outputs. Channel 4 driver high and low levels.
75, 77 28, 29 25, 26 76, 74	DOUT_5, DIN_5 DATA_5, EN_5 COMP_A_5, COMP_B_5 DVH_5, DVL_5	Channel 5 driver output and comparator input pins. Channel 5 driver data and enable inputs. Channel 5 comparator outputs. Channel 5 driver high and low levels.
72, 70 31, 30 34, 33 71, 73	DOUT_6, DIN_6 DATA_6, EN_6 COMP_A_6, COMP_B_6 DVH_6, DVL_6	Channel 6 driver output and comparator input pins. Channel 6 driver data and enable inputs. Channel 6 comparator outputs. Channel 6 driver high and low levels.
65, 67 38, 39 35, 36 66, 64	DOUT_7, DIN_7 DATA_7, EN_7 COMP_A_7, COMP_B_7 DVH_7, DVL_7	Channel 7 driver output and comparator input pins. Channel 7 driver data and enable inputs. Channel 7 comparator outputs. Channel 7 driver high and low levels.
Central Resource Pins		
47	V_REF	External precision voltage reference.
48	R_EXT	External precision reference resistor.
41, 42	PLL_CK, PLL_CK*	PLL reference input frequency.
124	VBB	Analog voltage that sets the threshold for the high speed digital inputs.
108, 109	CPMU_CAP_IN, CPMU_CAP_OUT	Compensation capacitor for the central PMU.
44	CAP_PLL	PLL filter capacitor.
117	DUT_GND	Analog voltage input used to track ground at the DUT.
105, 106	EXT_FORCE, EXT_SENSE	External PMU connection pins.
112	MONITOR	Analog voltage output of the PPMU.
CPU Interface		
58, 59, 57	CK, SDIO, STB	3 bit serial port (Clock, Data and Strobe).
119	RESET	Chip reset.
Power Supplies		
63, 104, 110, 122	VCCH	High voltage positive power supply.
68, 78, 88, 98, 114	VCC	Positive supply voltage.

Pin #	Pin Name	Description
54, 62, 69, 79, 89, 99, 107, 115, 123	VEE	Negative supply voltage.
40, 45, 52, 55, 60, 116, 121, 125	VDD	Digital power supply.
46, 49, 53, 56, 61, 111, 13, 118, 120, 127	GND	Digital ground.
43, 126	VTT	Digital input termination power supply.
2, 12, 22, 32	VOH_01, VOH_23, VOH_45, VOH_67	Comparator output high level power supply.
7, 17, 27, 37	VOL_01, VOL_23, VOL_45, VOL_67	Comparator output low level power supply.

Pin Configuration



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCCH	VCC – 0.4		VEE + 18	V
VCC	0		VEE + 18	V
VEE	–4.5		0	V
VCCH – VEE	0		+18	V
VDD	0		+5	V
VTT	GND – 0.4		VDD + 0.4	V
VDD – VEE		+8		V
VOH		VDD + 0.4V		V
VOL		GND – 0.5		V
Output Voltage				
DOUT	VEE		VCCH	V
Digital Input Pins				
DATA, EN, CK, SDIO, STB, PLL_CK(*)	GND – 0.25		VDD + 0.25	V
Output Currents				
COMP_A, COMP_B	–80		80	mA
SDIO	–20		20	mA
External References				
Voltage on R_EXT	GND – 0.25		VDD – 0.25	V
V_REF	GND – 0.25		VCC + 0.25	V
R_EXT	8		12	KΩ
VBB	GND – 0.25		VDD + 0.25	V
EXT_SENSE	VEE – 0.4		VCCH + 0.4	V
EXT_FORCE	VEE – 0.4		VCCH + 0.4	V
Thermal Information				
Maximum Junction Temperature			150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCCH	VCC		VEE +16.5	V
VCC	+6		VEE + 16.5	V
VEE	–4		–2.7	V
VDD	+3.25		+3.45	V
GND		0		V
VCCH – VEE		+16		V
VDD – VEE		+7.5		V
Comparator Output Supplies				
VOH		VDD		V
VOL		GND		V
VOH – VOL	0.4		VDD – GND	V
VTT	GND		VDD	V
Digital Inputs (DATA/*; EN/*)				
CK, SDIO, STB, RESET	GND		VDD	V
Driver Levels				
DVH, DVL	VEE + 1		VCC – 1	V
Threshold Levels				
CVA, CVB	VEE + 2		VCCH – 2	V
CVA_PPMU, CVB_PPMU	VEE + 2		VCCH – 2	V
VBB	0.5		2.0	V
PMU Levels				
V-FV	VEE + 1		VCCH – 1	V
V-CI-Lo	VEE + 1		VCCH – 3	V
V-CI-Hi	VEE + 3		VCCH – 1	V
V-CI-Hi – V-CI-Lo	–1		+1	V
External Load Capacitance			1	nF
External References				
V_REF	+2.99		+3.01	V
R_EXT	9.99		10.01	KΩ
PLL-CK	50		100	MHz
VBB	0.8		2.4	V
EXT_SENSE	VEE		VCCH	V
EXT_FORCE	VEE		VCCH	V
DUT_GND	–300		+300	mV
Miscellaneous				
Junction Temperature Range	+25		100	°C
CPU Port CK Frequency	10		25	MHz

DC Characteristics

NOTE: For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supplies

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +13.5V, VCC = +8.25V, VEE = –3.5V, VCC–VEE = +17V, VDD = +3.5V, VTT = 0V, VOH = +3.0V, VOL = 0V. Power consumption is calculated using the typical current values and the nominal supply levels.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd
PLL_CK = 50MHz, Data Rate = Static							
11400	VCCH	All delay elements bypassed.	30	50	75	mA	650mW
11100	VCC		25	35	45	mA	285mW
11300	VCC		300	410	500	mA	1,353mW
11200	VEE		75	100	140	mA	300mW
						Total	2.6 Watts
PLL_CK = 100MHz, Data Rate = Static							
11410	VCCH	All delay elements bypassed.	30	50	75	mA	650mW
11110	VCC		25	35	45	mA	285mW
11310	VCC		350	450	550	mA	1,485mW
11210	VEE		75	100	140	mA	300mW
						Total	2.7 Watts
PLL_CK = 50MHz, Dynamic							
12400	VCCH	33 MHz Operation. All channels configured as a ring oscillator. All delay elements enabled, CD = Min Delay, CFEA = Mid.	30	53	75	mA	689mW
12100	VCC		80	100	125	mA	800mW
12300	VDD		400	525	600	mA	1,733mW
12200	VEE		130	170	210	mA	510mW
						Total	3.7 Watts
PLL_CK = 100MHz, Dynamic							
12410	VCCH	33 MHz Operation. All channels configured as a ring oscillator. All delay elements enabled, CD = Min Delay, CFEA = Mid.	30	53	75	mA	689mW
12110	VCC		100	125	150	mA	1,000mW
12310	VDD		540	650	740	mA	2,145mW
12210	VEE		155	195	235	mA	585mW
						Total	4.4 Watts

DC Electrical Specifications – CPU Port

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH		2.0			V
17110	VIL				0.8	V
17120	Iin (Input Leakage Current)	Tested @ +3V.	–100	0	+100	nA
17200	VOH (SDIO Only)	Output Current = 8mA	2.4			V
17210	VOL (SDIO only)	Input Current = 8mA.			0.8	V

DC Electrical Specifications – Analog Pins

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
10999	V_REF Input Current	Note 1	–1	0	+1	µA
10998	DUT_GND Input Current	Note 1; Tested at 0V.	–100	0	+100	nA
10997	EXT_FORCE, EXT_SENSE HiZ Leakage	Note 1; Tested at 0V	–100	0	+100	nA
10996	EXT_FORCE, EXT_SENSE HiZ Leakage	Note 1; Tested at VCCH and VEE.	–200	0	+200	nA
	Capacitance on EXT_FORCE	All other switched open. Limits established by characterization and are not production tested.		25		pF
	Capacitance on EXT_SENSE	All other switched open. Limits established by characterization and are not production tested.		8		pF

NOTES:
1. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V.

DC Electrical Specifications – PLL

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V. PLL = 50MHz (T = 20ns).

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential Inputs PLL_CK/PLL_CK*						
	Differential Input Swing - VIH	Note 2; VIH = 2.1V, VIL = 1.9V; VIH = 1.1V, VIL = 0.9V.	0.2		VDD	V
	Differential Input Swing - VIL	Note 2; VIH = 2.1V, VIL = 1.9V; VIH = 1.1V, VIL = 0.9V.	0		VDD	V
	Crossing Voltage	Note 2; VIH = 2.1V, VIL = 1.9V; VIH = 1.1V, VIL = 0.9V.	0.5		2.25	V
18100	Input Leakage Current	PLL–ZA = 0; PLL–ZB = 0; Tested @ +3V.	–100	0	+100	nA
18110	Differential Input Resistance	(PLL–ZA = 1; PLL–ZB = 0) or (PLL–ZA = 0; PLL–ZB =1)		105		Ω

NOTES:
2. Limits established by characterization and are not production tested.

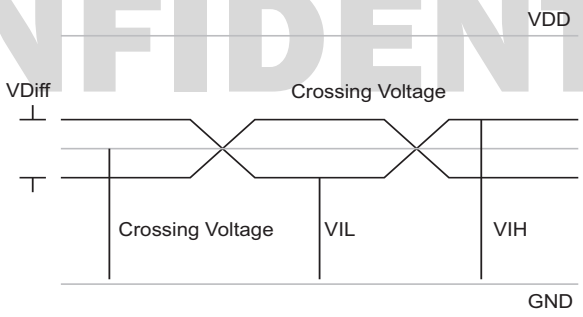


FIGURE 1.

DAC

There are 3 on-chip internal DACs per channel used for:

1. DC Level
2. DC Level Offset Correction
3. DC Level Gain Correction

These on-chip DACs are not used off-chip explicitly as stand-alone outputs. Rather, they are internal resources that are used by every functional block. The DACs are tested many times over by the DC tests for driver, comparator, and PMU. However, the DACs are specifically tested independently from all other functional blocks to verify basic functionality.

DC Electrical Specifications – DAC

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Level DAC Test						
16100	Span	Notes 3, 4, 5; Span = DAC (FFFF) – DAC (0000)	7.5	8.0	8.5	V
16110	Linearity	Notes 3, 4, 5, 6	–10	0	+10	mV
16120	Bit Test	Notes 3, 4, 5; 7	–10	0	+10	mV
16150	Major Carry Error	Notes 3, 4, 5; DAC Code 8000 – 7FFF – 1LSB	–10	0	+10	mV
16190	Level Droop	VR1 (or VIR), DAC Code = 0000Hex, No load, all levels.	–600		+600	µV/ms
Offset DAC Test						
16200	+ Adjustment Range	Notes 3, 4, 8; Code 0000, FFFF relative to midscale (7FFF)	+4.8	+5.3	+5.8	% of Span
16210	– Adjustment Range	Notes 3, 4, 8; Code 0000, FFFF relative to midscale (7FFF)	–5.8	–5.3	–4.8	% of Span
16220	Linearity	Notes 3, 4, 6, 8	–5	0	+5	mV
16230	Bit Test	Notes 3, 4, 7, 8	–5	0	+5	mV
16250	Major Carry Error	Notes 3, 4, 8; DAC Code 8000 – 7FFF – 1LSB	–5		+5	mV
Gain DAC Test						
16300	+ Adjustment Range	Notes 3, 4, 9	1.07	1.10	1.15	V/V
16310	– Adjustment Range	Notes 3, 4, 9	.850	.89	.922	V/V
16320	Linearity	Notes 3, 4, 6, 9	–20	0	+20	mV/V
16330	Bit Test	Notes 3, 4, 7, 9	–20	0	+20	mV/V
16350	Major Carry Error	Notes 3, 4, 9; DAC Code 8000 – 7FFF – 1LSB	–5		+5	mV/V
Noise						
16400	DAC Noise Test	Notes 3, 4, 9, 10			+3	mV
Offset DAC Calibration						
16260	DAC in VR0		–202		+202	mV
16270	DAC in VR1		–404		+404	mV
16280	DAC in VR2		–808		+808	mV
16290	DAC in VIR		–101		+101	mV
Gain DAC Calibration						
16360	Gain DAC Calibration		.8825		1.1175	V/V

NOTES:

3. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.
4. DAC tests performed using the PMU in FV mode and the MONITOR output VR1.
5. Offset and Gain DACs both programmed to mid scale (Code 7FFF).
6. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, **DFFF**, EFFF, FFFF
7. Bit Test - Waling 1 and walking 0 to determine the correct bit weight: 1's - 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0000; 0's - 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE
8. Level and Gain DACs both programmed to mid scale (Code 7FFF).
9. Level and Offset DACs both programmed to mid scale (Code 7FFF).
10. FV = 0V; VR2; Measured @ DOUT_0; RMS measurement.

PMU - Force Voltage

The sequence of events performed for FV Testing is:

1. Program FV
2. Force current at DOUT_0
3. Measure the voltage at DOUT_0

FV Tests:

1. VR0 tested in IR5
2. VR1 tested in IR5
3. VR2 tested in IR6 and IR7 (no load)
4. VR2 tested in IR0 – IR7 (max load)

DC Electrical Specifications – PMU Force Voltage

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV (Post Calibration)						
14200	Output Force Error	VR0, Cal0; FV VR0 Test Points	–10	–0.1	+10	mV
14201	Output Force Error	VR1, Cal1, FV VR1 Test Points	–20	–0.6	+20	mV
14202	Output Force Error	VR2, Cal2, FV VR2 Test Points	–30	+1.73	+30	mV
	FV Temperature Coefficient	VR0; Note 11		–150		µV/°C
	FV Temperature Coefficient	VR1, Note 11		–300		µV/°C
	FV Temperature Coefficient	VR2, Note 11		–600		µV/°C
NOTES: 11. Limits established by characterization and are not production tested.						

TABLE 1.

Range	Cal Points	FV Test Points
VR0 IR5	0V/0µA +3V/0µA	–.5V/0µA +1.5V/0µA +3.5V/0µA
VR1 IR5	0V/0µA +5V/0µA	–1V/0µA +3V/0µA +7V/0µA
VR2 IR6 & IR7 Only	0V/0µA +10V/0µA	–1V/0µA +6V/0µA +11V/0µA
VR2 IR0 – IR7	0V/0µA +10V/0µA	+2V/–Imax +8V/+Imax

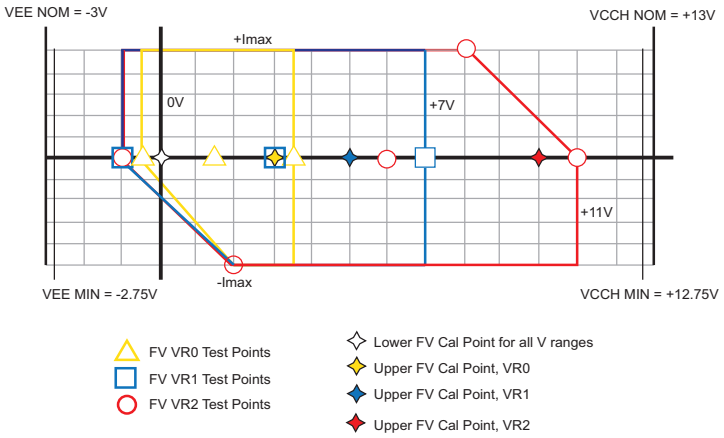


FIGURE 2.

DC Electrical Specifications – PMU Measure Current

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V. MI tested in VR2, IR0 – IR7. MI tests performed after a 2-point software calibration.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MI (Post Calibration)						
14100	Measure Current Error	MI Test Points, IR0	–15	–0.275	+15	nA
14101	Measure Current Error	MI Test Points, IR1	–40	1.29	+40	nA
14102	Measure Current Error	MI Test Points, IR2	–160	12.7	+160	nA
14103	Measure Current Error	MI Test Points, IR3	–640	46.4	+640	nA
14104	Measure Current Error	MI Test Points, IR4	–2.56	.146	+2.56	µA
14105	Measure Current Error	MI Test Points, IR5	–10	.70	+10	µA
14106	Measure Current Error	MI Test Points, IR6	–40	2.17	+40	µA
14107	Measure Current Error	MI Test Points, IR7	–160	6.78	+160	µA
	MI Temperature Coefficient	IR5; Limits established by characterization and are not production tested.		+100		nA/°C

TABLE 2.

Range	Cal Points	MITest Points
VR2 IR6 & IR7 Only	+5V/+8 • Imax +5V/–.8 • Imax	–1V/0µA +11V/0µA +2V/–Imax +8V/+Imax

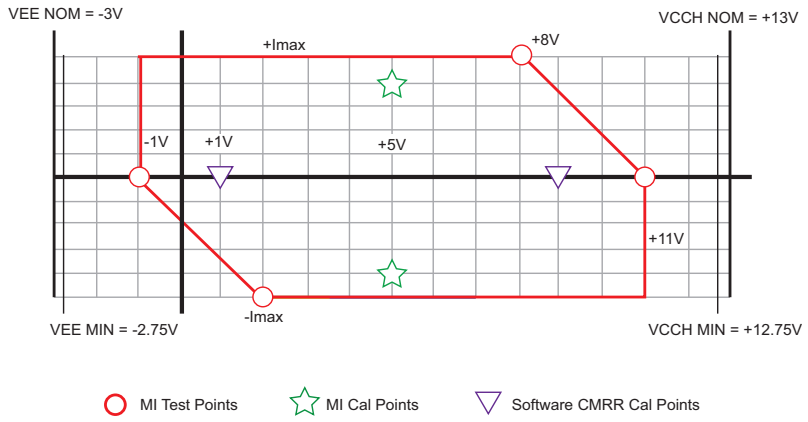


FIGURE 3.

PMU Force Current

The sequence of events performed for FI Testing is:

1. Program FI to the desired current
2. Force voltage with external PMU at DOUT_0
3. Measure the current at DOUT_0.

FI is tested in all 8 current ranges post software CMRR calibration.

DC Electrical Specifications – PMU Force Current

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Post Calibration FI Error						
14800	Force Current Error	FI Test Points, IR0	–15	0.01	+15	nA
14801	Force Current Error	FI Test Points, IR1	–40	–0.64	+40	nA
14802	Force Current Error	FI Test Points, IR2	–160	–5.02	+160	nA
14803	Force Current Error	FI Test Points, IR3	–640	–13.1	+640	nA
14804	Force Current Error	FI Test Points, IR4	–2.56	–0.051	+2.56	µA
14805	Force Current Error	FI Test Points, IR5	–10	0.292	+10	µA
14806	Force Current Error	FI Test Points, IR6	–40	1.72	+40	µA
14807	Force Current Error	FI Test Points, IR7	–160	4.66	+160	µA
	FI Temperature Coefficient	IR5; Limits established by characterization and are not production tested.		+250		nA/°C

TABLE 3.

Range	Cal Points	MITest Points
IR0 – IR7	+5V/+8 • Imax +5V/–.8 • Imax	–1V/0µA +8V/0µA +2V/–Imax +11V/+Imax

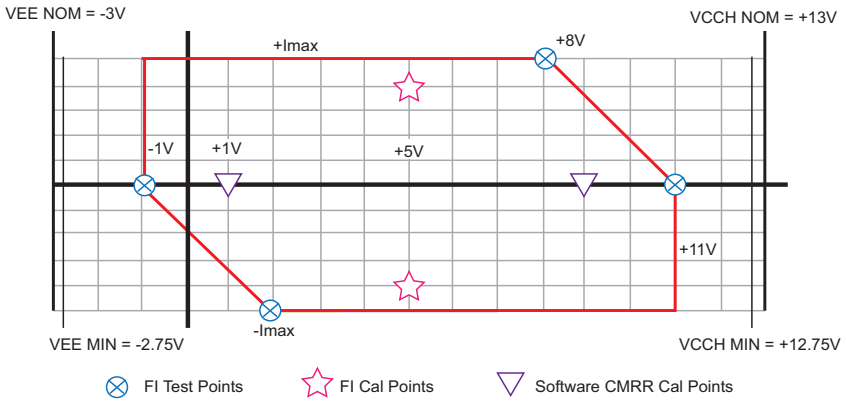


FIGURE 4.

Measure Voltage - Monitor

The sequence of events performed for testing the MONITOR is:

1. Program FV to the desired voltage (in VR2, IR5, Iload = 0)
2. Measure the voltage at DOUT_0
3. Measure the voltage at MONITOR
4. Calculate the difference to determine the error.

MONITOR is tested post 2-point software calibration.

DC Electrical Specifications – Measure Voltage (Monitor)

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V unless otherwise noted.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14710	HiZ Leakage Current	Note 12; Tested at MONITOR = 0V, VCCH, VEE	–200	0	+200	nA
19100	Output Impedance	Tested at +5V, Iout = 0µA, 1mA		0.6	1.0	kΩ
14720	Voltage Error	Tested at MONITOR = 0V, VCCH, VEE	–10	0.2	+10	mV
	MV Temperature Coefficient	Limits established by characterization and are not production tested.		<50		µV/°C
14741	DUT_GND Error	Note 13	–10	–0.2	+10	mV

NOTES:
12. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V.
13. DUT_GND = ±300mV, FV Mode, V-FV = +3V, measured at Test & Cal relative to GND.

TABLE 4.

Range	Cal Points	MV Test Points
IR5	0V/0µA +10V/0µA	–1V/0µA +5V/0µA +11V/0µA

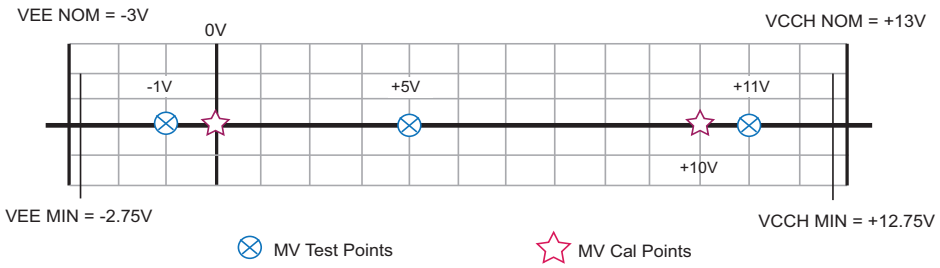


FIGURE 5.

DC Electrical Specifications – Measure Voltage (Comparator)

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V. The window comparator thresholds are tested using a binary search algorithm at the digital outputs COMP_A and COMP_B.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14600	Threshold Error, VR0	VR0, Cal0; Note 14	–15	–0.24	+15	mV
14601	Threshold Error, VR1	VR1, Cal1, Note 15	–20	–0.45	+20	mV
14602	Threshold Error, VR2	VR2, Cal2, Note 16	–30	+0.76	+30	mV
14603	Threshold Error, VIR	VIR, Cal3, Note 17	–10	0.056	+10	mV
	MV Temperature Coefficient	VR0, Note 18		–150		µV/°C
	MV Temperature Coefficient	VR1, Note 18		–300		µV/°C
	MV Temperature Coefficient	VR2, Note 18		–600		µV/°C
	MV Temperature Coefficient	VIR, Note 18		–75		µV/°C

NOTES:
14. PMU comparator threshold test points, VR0, test the comparator outputs using a binary search.
15. PMU comparator threshold test points, VR1, test the internal references via Test & Cal Mux.
16. PMU comparator threshold test points, VR2, test the comparator outputs using a binary search.
17. PMU comparator threshold test points, VIR, test the internal references via Test & Cal Mux.
18. Limits established by characterization and are not production tested.

TABLE 5. PPMU Comparator Threshold

V Range	Cal Points	Test Points
VR0	0V +3V	–.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +10V	–1V +6V +11V
VIR	–.8V +.8V	–1V 0V +1V

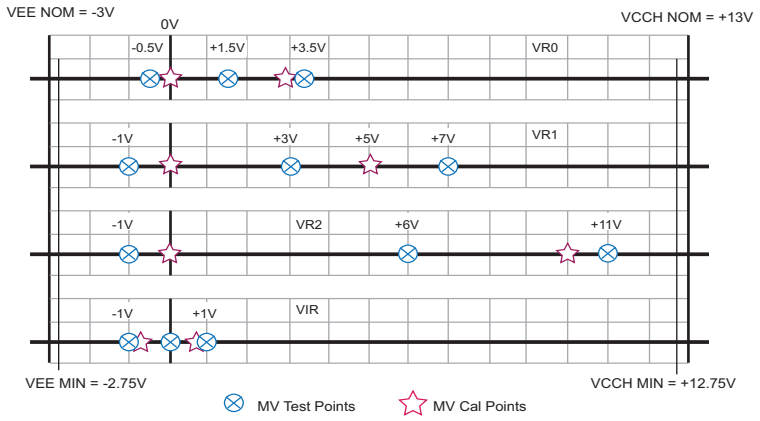


FIGURE 6.

DC Electrical Specifications – Voltage Clamp Low

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14400	Low Voltage Clamp Error	Low voltage clamp test points, VR0	–100	0.1	+100	mV
14410	Low Voltage clamp Error	Low voltage clamp test points, VR1	–100	–0.3	+100	mV
14420	Low Voltage clamp Error	Low voltage clamp test points, VR2	–100	2.7	+100	mV

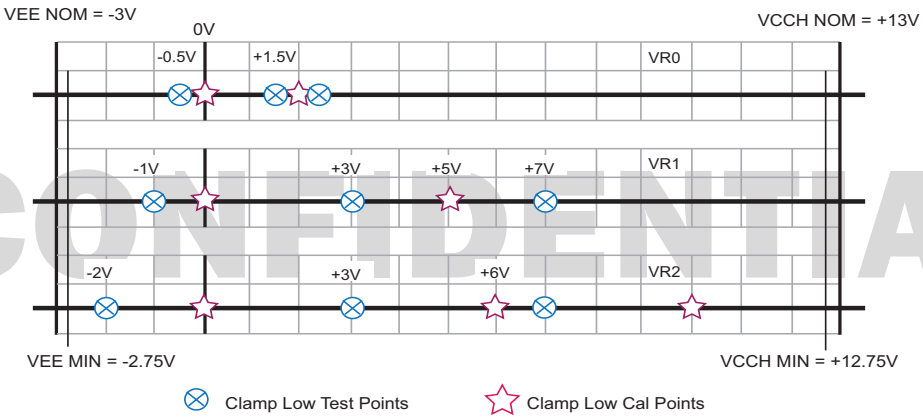


FIGURE 7.

TABLE 6.

V Range	Cal Points	Test Points
VR0	0V +2V	–.5V +1.5V +2.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +6V	–1V +3V +7V

DC Electrical Specifications – Voltage Clamp High

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14440	High Voltage Clamp Error	High voltage clamp test points, VR0	–100	0.1	+100	mV
14450	High Voltage Clamp Error	High voltage clamp test points, VR1	–100	0.3	+100	mV
14660	High Voltage Clamp Error	High voltage clamp test points,, VR2	–100	–1.2	+100	mV

TABLE 7.

V Range	Cal Points	Test Points
VR0	0V +3V	+1V +1.5V +3.5V
VR1	+1V +5V	–1V +3V +7V
VR2	+1V +10V	+1V +5V +11V

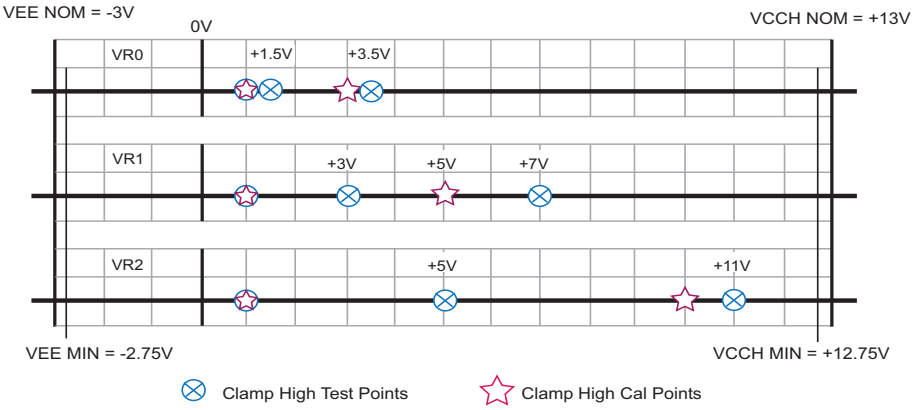


FIGURE 8.

Current Clamps

Current clamps are tested in all 8 current ranges and are tested in a non-calibrated state. The sequence of events to test the high current clamps are:

1. Program I-Cl-Hi
2. Program FV = +5V
3. Program the tester PMU to +4V
4. Measure the current at DOUT_0

The sequence of events to test the low current clamps are:

1. Program I-Cl-Lo
2. Program FV = +5V
3. Program the tester PMU to +6V
4. Measure the current at DOUT_0.

DC Electrical Specifications – Current Clamps

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
13500	High Current Clamp	I-Cl-Hi = FFFF, Gain = FFFF, Offset = FFFF	Imax	1.25 • Imax	1.5 • Imax	mA
13520	Low Current Clamp	I-Cl-Lo = 0000, Gain = FFFF, Offset = 0000	–1.5 • Imax	–1.25 • Imax	–Imax	mA

DC Electrical Specifications – Resistor Values

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Sense Resistors						
19000	IR0			500		kΩ
19010	IR1			125		kΩ
19020	IR2			31.25		kΩ
19030	IR3			7.81		kΩ
19040	IR4			1.95		kΩ
19050	IR5			500		Ω
19060	IR6			125		Ω
19070	IR7			31.25		Ω
FET Switches to DIN_#						
19105	Con-CPMU-F-C#			40		Ω
19107	Con-CPMU-S-C#			6		kΩ
19109	Con-Ext-S-C#			6		kΩ
19111	Con-Ext-F-C#			40		Ω
19112	Con-DIN-C#	Con-DinC# and Con-DOUT-C# tested together. The		.6		kΩ
19112	Con-DOUT-C#	Con-DinC# and con-DOUT-C# tested together. The		.6		kΩ
FET Switches to DOUT_#						
19106	Con-CPMU-S-D#			6		kΩ
19108	Con-Ext-S-D#			6		kΩ
19110	RT-Con-Ext-F-D#			40		Ω
19113	RT-Con#			40		Ω
Central PMU Switches						
19101	Con-EF-CF			40		Ω
19102	Con-ES-CF			6		kΩ
19103	Con-EF-CS			6		kΩ
19104	Con-ES-CS			6		kΩ

DC Electrical Specifications – CMRR

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V. FV Mode, VR2, Iout = 0 (Open switch), tight loop, measure MI @ MONITOR, test @ +1V and +9V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14203	Measured CMRR, IR0		–2		+2	nA/V
14213	Measured CMRR, IR1		–8		+8	nA/V
14223	Measured CMRR, IR2		–32		+32	nA/V
14233	Measured CMRR, IR3		–128		+128	nA/V
14243	Measured CMRR, IR4		–512		+512	nA/V
14253	Measured CMRR, IR5		–2		+2	µA/V
14263	Measured CMRR, IR6		–8		+8	µA/V
14273	Measured CMRR, IR7		–32		+32	µA/V

DC Electrical Specifications – Driver

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
13300	HiZ Leakage (DOUT + DIN)	Tested @ DOUT = 0V, Con-DOUT-C# = 1	–5	–0.2	+5	nA
13310	HiZ Leakage (DOUT + DIN)	Tested @ DOUT = VCCH, VEE, Con-DOUT-C# = 1	–15	+0.4	+15	nA
13100	DVH, DVL Post Cal Error (Range 0)	VR0 Test Points	–10	+0.2	+10	mV
13120	DVH, DVL Post Cal Error (Range 1)	VR1 Test Points	–20	–0.4	+20	mV
13140	DVH, DVL Post Cal Error (Range 2)	VR2 Test Pionts	–30	+0.8	+30	mV
	DVH, DVL Temperature Coefficient (Range 2)	VR1, Note 19		–300		µV/°C
13320	DOUT Output Impedance	Note 20		48		Ω
13321	DVH, DVL DC Output Current	Note 21	±35			mA
	DVH, DVL AC Output Current	Note 19	±70			mA
	Output Capacitance at DOUT	Notes 19, 22		9		pF
Digital Inputs DATA & EN						
13210	VIH (DATA – VBB; EN – VBB)	DATA, EN = 1.9V, VTT = 0V	400			mV
13220	VIL (VBB – DATA; VBB – EN)	DATA, EN = 1.1V, VTT = 0V	400			mV
13230	Input Leakage Current	Tested @ +3V; Note 23	–100	0	+100	nA
13240	Input Resistance to VTT	Notes 24 or 25	70	105	130	Ω
13231	VTT Input Leakage	Tested @ +1.5V; Note 23	–1	0	+1	µA
13232	VBB Input Leakage	Tested @ +1.5V	–100	0	+100	nA

NOTES:
19. Limits guaranteed by characterization and are not production tested.
20. DVH = 3.0V, 19.2mA sourced @ DOUT Radj = 0000; DVL = 0V, 19.2mA sunk @ DOUT Radj = 0000.
21. DOUT forcing +5V and shorted to GND, forcing 0V and shorted to +5V.
22. DIN pin floating, Con-DOUT-C# = 1, all other switches open.
23. Data#-ZA = 0; Data#-ZB = 0; En#-ZA = 0; En#-ZB = 0.
24. Data#-ZA = 1; Data#-ZB = 0; En#-ZA = 1; En#-ZB = 0.
25. Data#-ZA = 0; Data#-ZB =1; En#-ZA = 0; En#-ZB = 1.

TABLE 8.

V Range	Cal Points	Test Points
VR0	0V +3V	–0.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +5V	–2V +3V +7V

DC Electrical Specifications – Comparator

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V unless otherwise noted. The window comparator thresholds are tested using a binary search algorithm at the digital outputs COMP_A and COMP_B.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14500	Post Calibration Threshold Error, VR0	Note 26	–15	–0.24	+15	mV
14501	Post Calibration Threshold Error, VR1	Note 27	–20	–0.45	+20	mV
14502	Post Calibration Threshold Error, VR2	Note 28	–30	+0.76	+30	mV
	Temperature Coefficient, VR0	Note 29		–150		µV/°C
	Temperature Coefficient, VR1	Note 29		–300		µV/°C
	Temperature Coefficient, VR2	Note 29		–600		µV/°C
13360	Comparator Output Impedance	VOH = +3V, sourcing 20mA; VOL = 0V, Sinking 20mA; Note 30		40		Ω
	DIN Input Capacitance	Con-DIN-C# = 1, all other switches open; Note 30		4		pF

NOTE:
26. Comparator threshold test points, VR0, test the comparator outputs using a binary search.
27. Comparator threshold test points, VR1, test teh internal references via Test & Cal Mux.
28. Comparator threshold test points, VR2, test the comparator outputs using a binary search.
29. Limits guaranteed by characterization and are not production tested.
30. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V.

TABLE 9.

V Range	Cal Points	Test Points
VR0	0V +3V	–0.5V +1.5V +3.5V
VR1	0V +5V	–1V +3V +7V
VR2	0V +10V	–1V +6V +11V

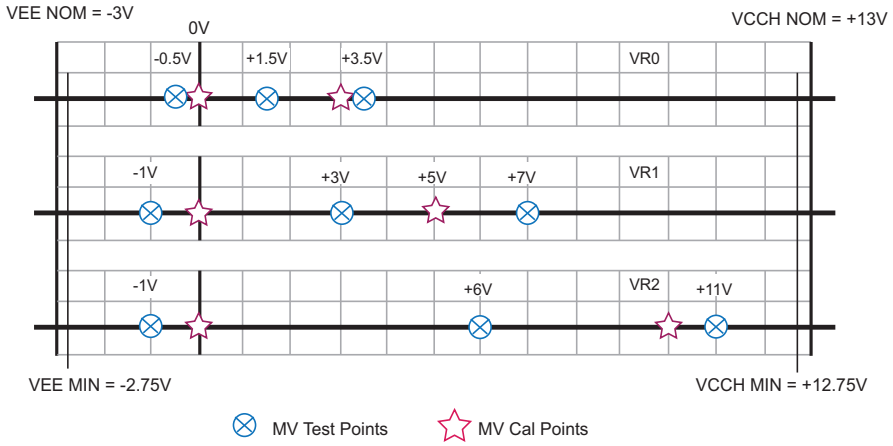


FIGURE 9.

AC Electrical Specifications – Driver

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall times						
22230	3V	Tested @ 20% and 80%; Note 31		2.0	4.0	ns
	Fmax	50MHz (T = 20ns); Note 32	66			MHz
	Minimum Pulse Width	Notes 31, 32		5.0	7.0	ns
Propagataion Delay						
	DATA to DOUT	Notes 31, 32, 33, 35		18		ns
	EN to DOUT	Notes 31, 32, 34, 35		18		ns
	ΔTpd vs. Temperature	50MHz (T = 20ns); Notes 31, 32, 35		+24		ps/°C
	ΔTpd vs. Temperature	100MHz (T = 10ns); Notes 31, 32, 35		+25		ps/°C
	ΔTpd vs. Duty Cycle	50MHz (T = 20ns); Notes 31, 32, 35, 36		100		ps
	ΔTpd vs. Duty Cycle	100MHz (T = 10ns);; Notes 31, 32, 35, 36		100		ps
	ΔTpd vs. Frequency	50MHz (T = 20ns); Notes 31, 32, 35, 37		<100		ps
	ΔTpd vs. Frequency	100MHz (T = 10ns); Notes 31, 32, 35, 37		<100		ps

AC Characteristics

NOTE: For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – CPU Port

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Set-Up Time						
27100	SDIO to Rising CK		10			ns
27110	STB to Rising CK		10			ns
Hold Time						
27120	SDIO to Rising CK		10			ns
27130	STB to Rising CK		10			ns
27140	CK Minimum Pulse Width High		18			ns
27150	CK Minimum Pulse Width Low		18			ns
27160	CK Period		40		100	ns
Propagation Delay						
27180	Rising CK to SDIO Out				10	ns
27170	Reset Minimum Pulse Width		100			ns

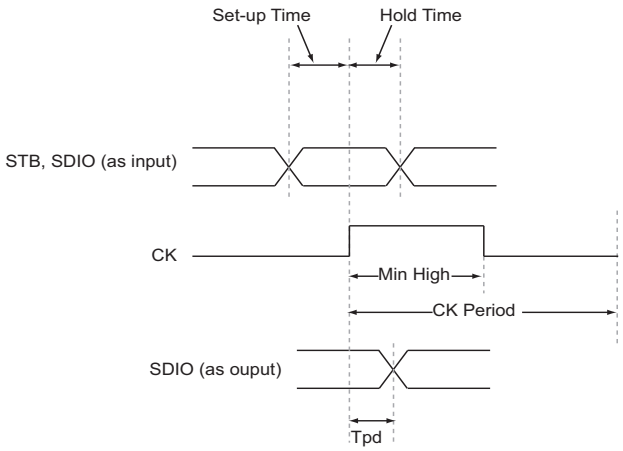


FIGURE 10.

AC Electrical Specifications – Driver

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Driver Path Jitter (DATA to DOUT) 1σ	Notes 31, 32, 35		13		ps
		50MHz (T = 20ns); Notes 31, 32, 38		16		ps
		100MHz (T = 10ns);; Notes 31, 32, 38		16		ps

NOTES:
31. DVH = 5V, DVL = –1V, into 50Ω to +1V. Configured in ring oscillator mode resulting in 0V to +3V signal at DOUT. Tested at 20% – 80% points.
32. Limits guaranteed by characterization and are not production tested.
33. DATA to DOUT. Tested at DOUT = 1.5V.
34. EN to DOUT. Tested at 2.25V and 0.75V.
35. All delay elements bypassed.
36. T = 100ns. Duty Cycle varies from 10% to 90%.
37. Input frequency varies from 10MHz to 50MHz.
38. All delay elements enabled, CD = Min Delay, CFEA - Mid.

AC Electrical Specifications – Comparator

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. Limits guaranteed by characterization and are not production tested. All delay elements bypassed unless otherwise noted.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Fmax	50MHz (T = 20ns)	66			MHz
	Minimum Pulse Width	VOH = 2V, VOL = 0V, DIN = 0V to 3V. CVA, CVB = 1.5V		5.0	7.0	ns
	Comparator Equivalent Bandwidth	Notes 39, 40		300		MHz
	Comparator Equivalent Bandwidth	Notes 39, 41		350		MHz
	Propagation Delay (DOUT to COMP_A, _B)			14		ns
	Output Rise Time (COMP_A, _B)			1.0		ns
	ΔTpd vs. Common Mode Input Voltage	0V to 1V; 4V to 5V; compare at signal midpoint; VR2		<100		ps
	ΔTpd vs. Swing	±1.5V input vs. ±100mV input; compare at signal midpoint; VR2		200		ps
	ΔTpd vs. Input Slew Rate	Notes 40, 42		100		ps
	ΔTpd vs. Input Slew Rate	Notes 41, 42		100		ps
	ΔTpd vs.Duty Cycle	100MHz (T = 10ns); Note 43		<100		ps
	ΔTpd vs. Temperature	100MHz (T = 10ns); 3V input signal, compared at midpoint; VR2		+16		ps/°C
	Comparator Path Jitter (DOUT to COMP_A, _B) 1σ			6		ps
		50MHz (T = 20ns); Note 38		8		ps
		100MHz (T = 10ns);; Note 38		7		ps

NOTES:

39. 10% – 90% BW = 0.35/((Tr-input)**2 – (Tr-measured)**2) ** 0.5. 3V input; Tr/Tf(input) = 1.2ns.
40. Driver active and used as a termination voltage (programmed to 0V).
41. Driver in HiZ..
42. 3V, 1.2ns input rise time vs. 3V, 5ns input rise time. VR2.
43. 3V input. Compare at signal midpoint. 100ns period. 10% to 90%; VR2.

Ring Oscillator

All loop delay measurements are taken with:

- The driver and comparator configured as a ring
- Channels tested in pairs
- the remaining channels static

NOTE: The loop time measured when the channel is configured as a ring oscillator does NOT indicate the total round-trip time of the pin electronics as some circuitry in the driver signal paths are bypassed and the circuitry of the ring oscillator control logic is inserted into the overall loop. The total delay measured in this configuration is used as a figure of merit to verify part-to-part AC performance.

AC Electrical Specifications – Ring Oscillator

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V unless otherwise noted.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
20200	Ring Oscillator Loop Delay (minimum loop time)	50MHz (T = 20ns); 100MHz (T = 10ns); Notes 35, 44, 45, 46, 47, 48, 49, 50	26	33	40	ns
20000	Ring Oscillator Loop Delay (max loop time, PLL_CK = 50MHz)	50MHz (T = 20ns); Notes 38, 45, 46, 49, 51	70	83	95	ns
20020	Ring Oscillator Loop Delay (max loop time, PLL_CK = 100MHz)	100MHz (T = 10ns); Notes 38, 45, 46, 49, 51	54	60	66	ns
20100	PLL Lock Test at 50MHz	50MHz (T = 20ns); Note 52	.95	1.1	1.23	V
20120	PLL Lock Test at 100MHz	100MHz (T = 10ns); Note 52	1.4	1.6	1.8	V

NOTES:
44. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC – VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V.
45. Tested in channel pairs 0/1; 2/3; 4/5; 6/7.
46. Ring configured DATA through Comp A.
47. Ring configured DATA through Comp B.
48. Ring configured EN through data path through Comp A via D#-XOR, CPU-En# = 1.
49. Ring triggered on a rising edge.
50. Ring triggered on a falling edge.
51. Delay elements programmed to maximum delay. FEA elements programmed to mid-code.
52. PLL voltage measured @ CAP_PLL pin.

AC Electrical Specifications – Coarse Delay

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +12.75V, VCC = +7.75V, VEE = –2.75V, VCC–VEE = +15.5V, VDD = +3.25V, VTT = 0V, VOH = +3.0V, VOL = 0V. Channels tested in pairs 0/1, 2/3, 4/5, 6/7. All other channels static.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA, EN, COMP A, B; PLL_CK = 50MHz (T = 20ns)						
25100	Tmin (Tpd+, Tpd– with CD = 0)	Channel 0 configured as a ring oscillator. All other channels static	2.2	2.9	3.6	ns
25110	Full Scale Delay (Tpd+, Tpd–)		15	19.375	25	ns
25115	Resolution (step size over all codes)			625		ps
DATA, EN, COMP A, B; PLL_CK = 100MHz (T = 10ns)						
25120	Tmin (Tpd+, Tpd– with CD = 0)		1.6	2.2	2.8	ns
25130	Full Scale Delay (Tpd+, Tpd–)		7.5	9.6785	12.5	ns
	Resolution (step size over all codes)	Limits guaranteed by characterization and are not production tested.		312.5		ps

AC Electrical Specifications – Coarse Falling Edge Adjust

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. VCCH = +13V, VCC = +8V, VEE = –3V, VCC–VEE = +16V, VDD = +3.3V, VTT = 0V, VOH = +3.0V, VOL = 0V. Channels tested in pairs 0/1, 2/3, 4/5, 6/7. All other channels static.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DATA, EN, PLL_CK = 50MHz (T = 20ns)						
25200	Tmin (Tpd+, Tpd–; Sel-XX-CFEA = 0; Code = 1000)		8	10.5	13	ns
25210	ΔTpd– Full Scale Acceleration (Code 0000 relative to 1000)		–7.0	–5.3	–3.7	ns
25220	ΔTpd– Full Scale Delay (Code 1111 relative to 1000)		3.1	4.5	5.9	ns
25215	Resolution (step size over all codes)			625		ps
25225	ΔTpd+ vs. all CFEA codes		–500		+500	ps
DATA, EN, PLL_CK = 100MHz (T = 10ns)						
25230	Tmin (Tpd+, Tpd–; Sel-XX-CFEA = 0; Code = 1000)		5.0	6.1	7.2	ns
25240	ΔTpd– Full Scale Acceleration (Code 0000 relative to 1000)		–3.3	–2.5	–1.8	ns
25250	ΔTpd– Full Scale Delay (Code 1111 relative to 1000)		1.6	2.3	3.0	ns
	Resolution (step size over all codes)	Limits guaranteed by characterization and are not production tested.		312.5		ps
25256	ΔTpd+ @ codes 0000 and 1111		–300		+300	ps

AC Electrical Specifications – CPMU

Junction Temperature = +50°C to +70°C, V_REF = 3.00V, R_EXT = 10.0kΩ, VBB = +1.5V, CK = 33MHz, DUT_GND = 0V. Limits guaranteed by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Force Settling Time						
	IR0	1 nF load. 0V to 5V input signal. PMU Sense = DOUT.		1,000		µs
	IR1			600		µs
	IR2			400		µs
	IR3			160		µs
	IR4			40		µs
	IR5			40		µs
	IR6			40		µs
	IR7			40		µs
Current Force Settling Time						
	IR0	–Imax to +Imax into an external resistive load equal to Rsense for each current range.		350		µs
	IR1			170		µs
	IR2			130		µs
	IR3			130		µs
	IR4			130		µs
	IR5			130		µs
	IR6			130		µs
	IR7			130		µs
MI Settling Time (through MONITOR)						
	IR0	–Imax to +Imax into an external resistive load equal to Rsense for each current range.		250		µs
	IR1			130		µs
	IR2			130		µs
	IR3			130		µs
	IR4			130		µs
	IR5			130		µs
	IR6			130		µs
	IR7			130		µs
	MV Settling Time (through MONITOR)	0V to 5V input at DOUT; Tr = 2ns.		5		µs

Chip Overview

ISl55169 is a highly integrated System-on-a-Chip (SOC) pin electronics solution aimed at incorporating every analog function (with some digital support functionality) required on a per channel basis for Automated Test Equipment. The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.

CPU Control

All configuration set up and the writing to and reading back of the internal registers is controlled through the 3 bit serial data CPU port. The CPU port is typically used to set up the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. This chart shows how to program each internal signal.

Real Time Control

All real time control and observation is accomplished via the high speed input and output signals:

- DATA_0 – DATA_7 (Single Ended Inputs)
- EN_0 – EN_7 (Single Ended Inputs)
- COMP_A_0 – COMP_A_7 (Single Ended Outputs)
- COMP_B_1 – COMP_B_7 (Single Ended Outputs)

Analog References

All on-chip analog functions are related to one of several off-chip precision reference inputs:

- PLL_CK
- V_REF
- R_EXT

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, part to part, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

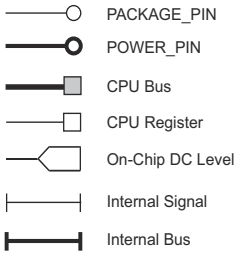
1. all capital letters (i.e. DATA_0, CK, SDIO)
2. underscores for clarity (i.e. DATA_0, COMP_B_1)
3. shown next to an I/O circle in any schematic.

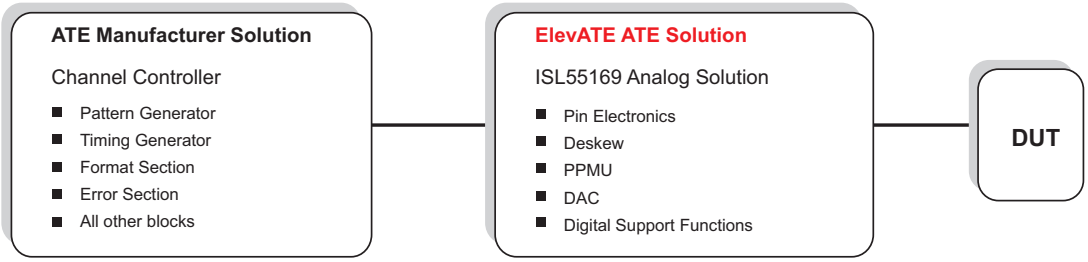
CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1. the first letter in a word is always a capital letter
2. subsequent letters within the same word are small
3. dashes (but never an underscore) for clarity
4. NOT shown with an I/O circle in any schematic.

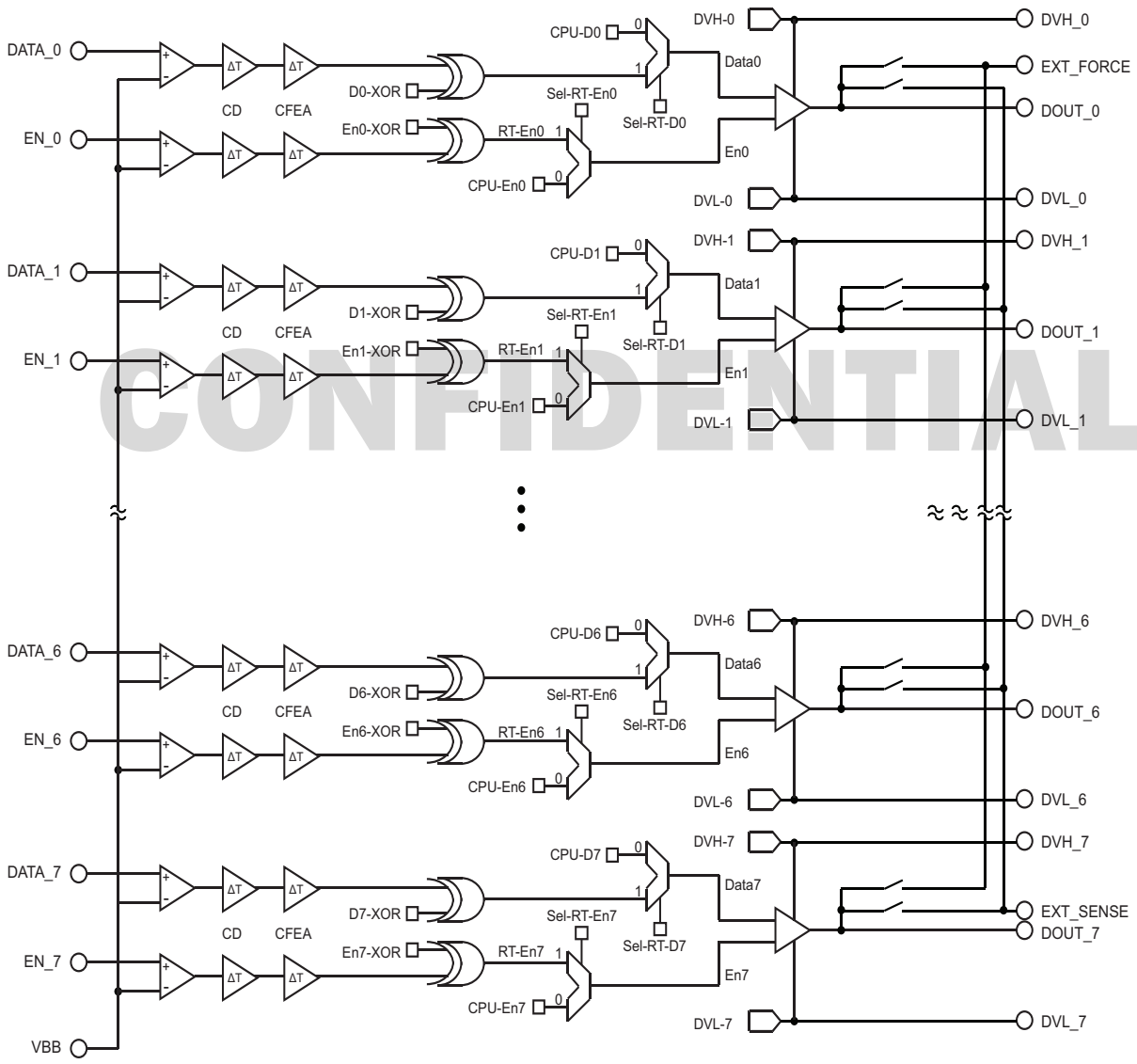
Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.



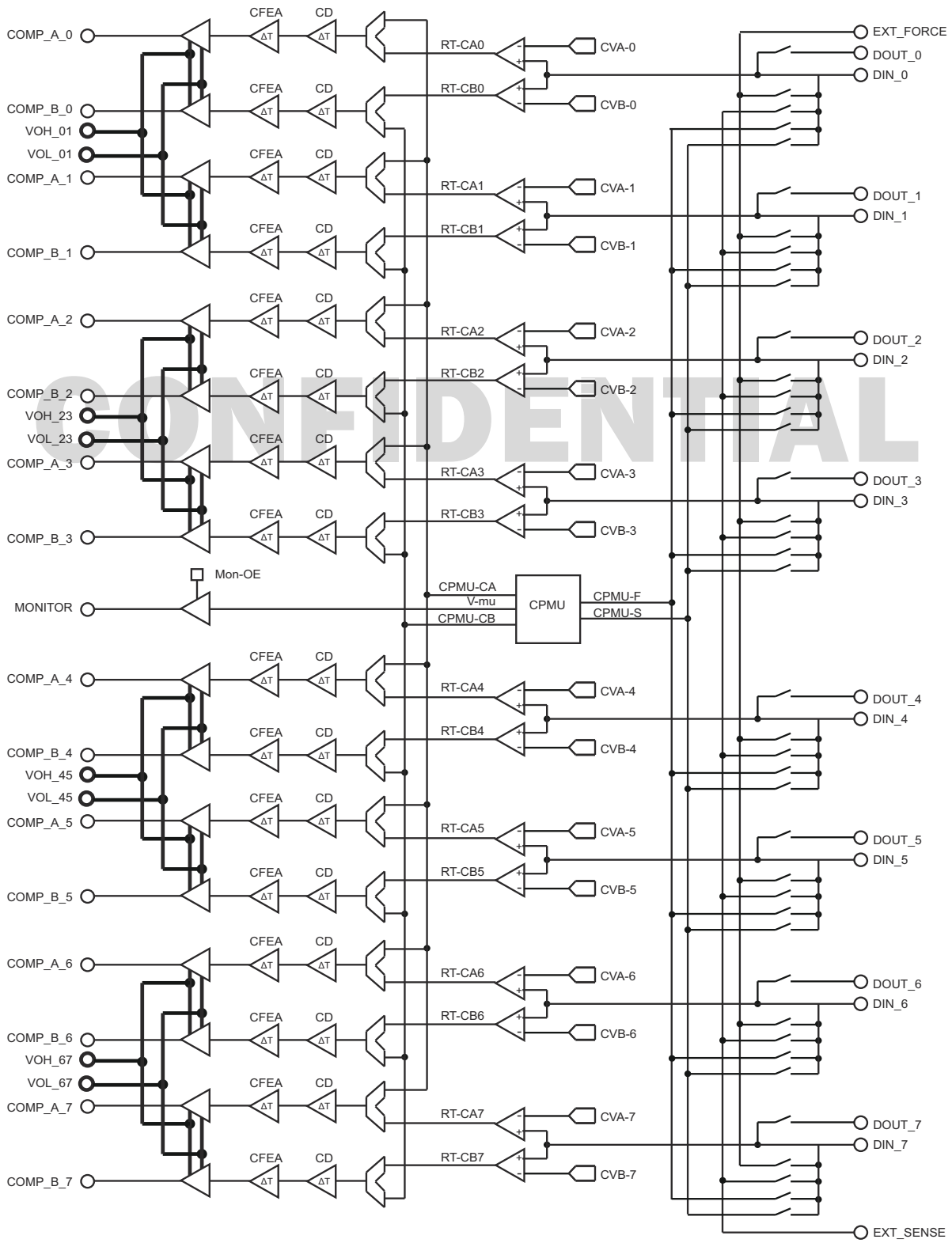


Circuit Diagrams

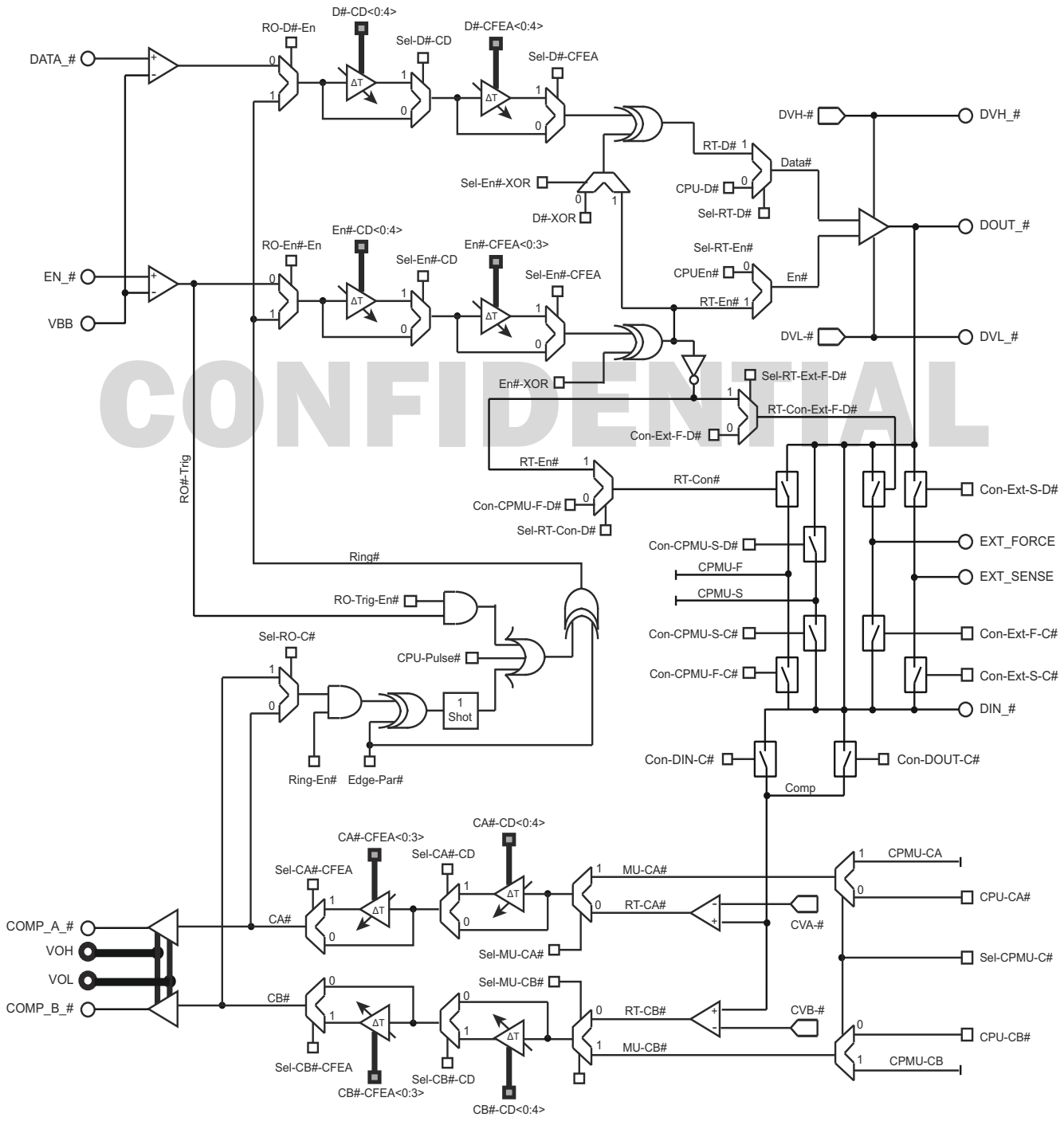
Driver Path



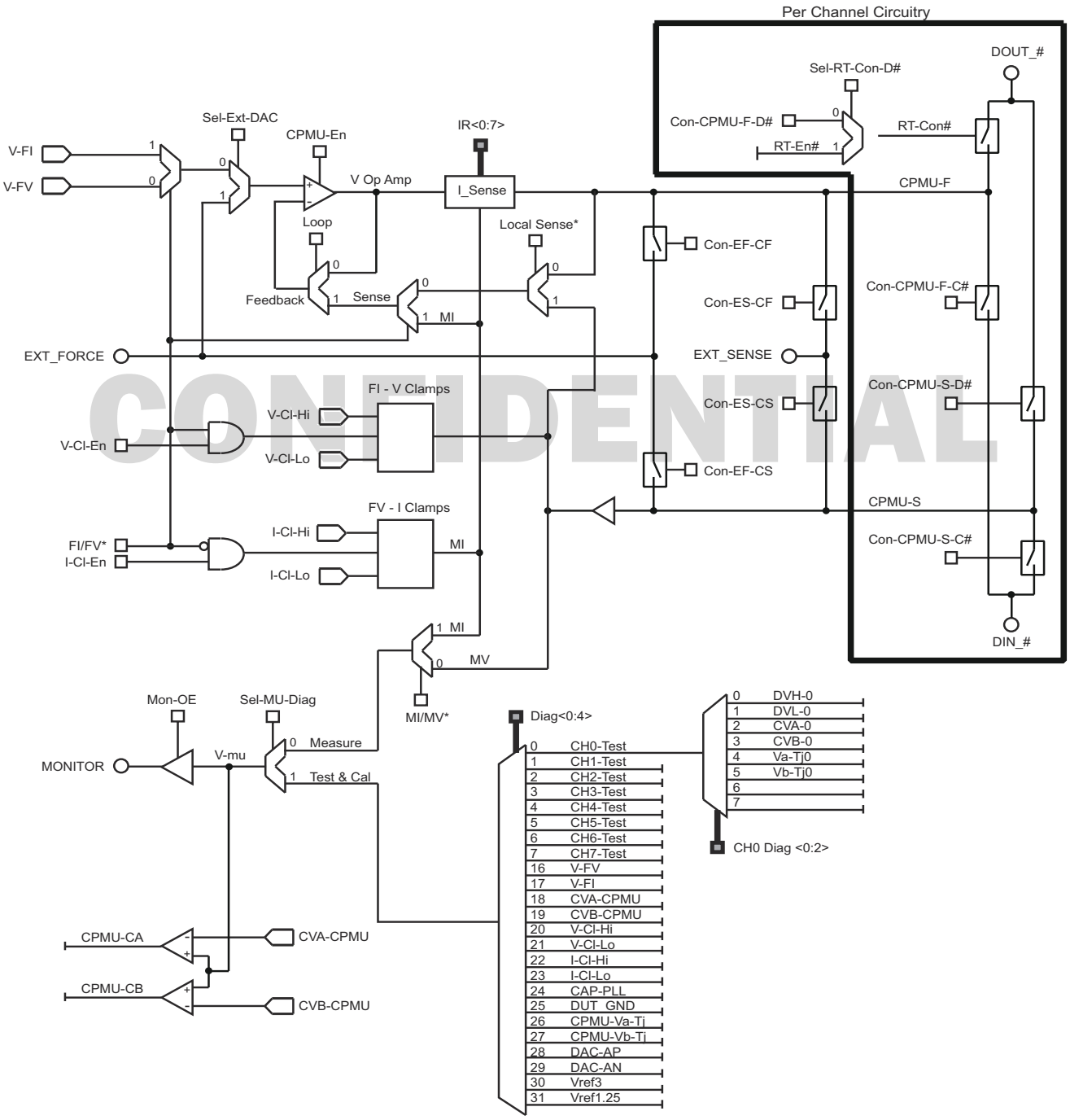
Comparator Path



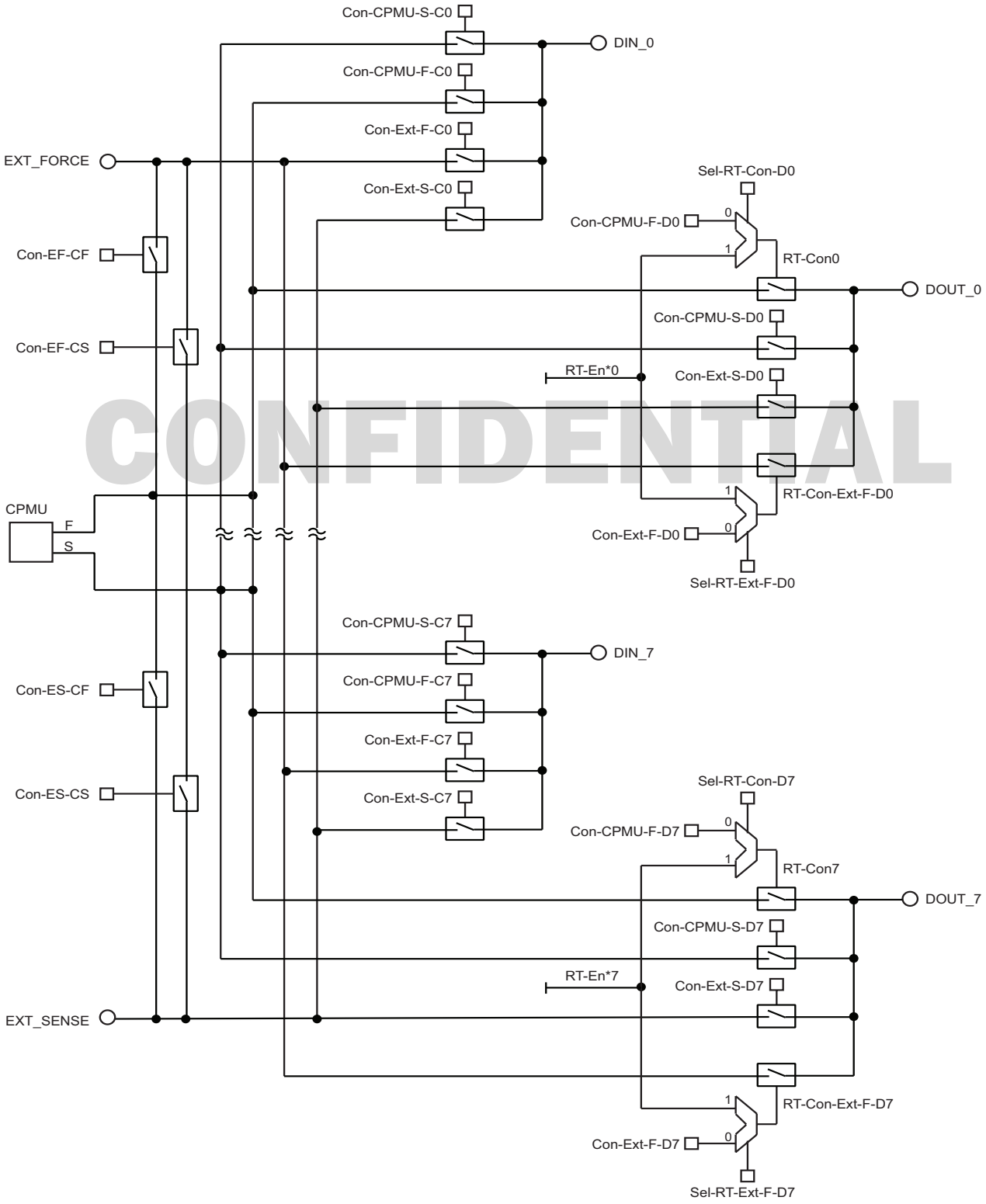
Per Channel Detailed Diagram



Central PMU



CPMU, Force, and Sense Routing Matrix



Channel Configuration

ISl55169 has a flexible architecture in that each channel may be configured as:

- 1 I/O channel
- 2 dedicated channels:
  - 1 drive only channel
  - 1 receive only channel

Configuration control is performed with on-chip switches controlled by the CPU port. Each channel may be configured independently, as there are no channel-to-channel restrictions.

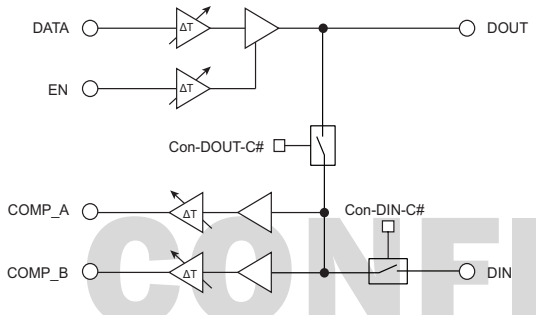


FIGURE 10.

Single I/O Channel

By setting Con-DOUT-C# = 1 and Con-DIN-C# = 0, an I/O channel is configured.

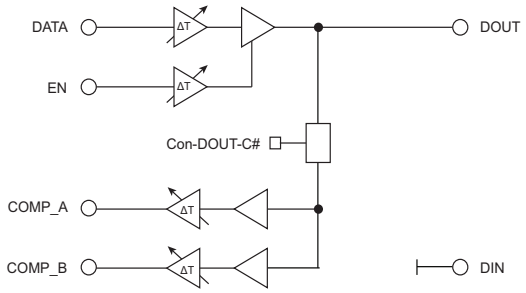


FIGURE 11.

Two Dedicated Channels

By setting Con-DOUT-C# = 0 and Con-DIN-C# = 1, independent drive-only and receive-only channels are established.

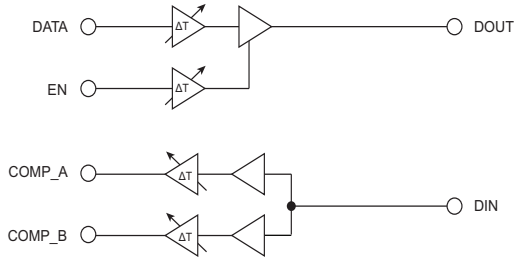


FIGURE 12.

PLL

The on-chip PLL is used to establish and maintain the range and resolution of all coarse delay and coarse falling edge adjust delay circuitry automatically. There is no other method to program these delay elements.

There are internal clamps which help guarantee that the PLL locks to the PLL_CK signal. The setting of the frequency clamps depends upon the PLL_CK frequency.

TABLE 10.

F Clamp<1:0>	PLL_CK Frequency
00	<70MHz
01	70MHz – 105MHz
10	Reserved (do not use)
11	Reserved (do not use)

Internal Control Bits

There are internal control bits that establish the operating conditions of the digital logic and the delay elements. The recommended setting for the V-Swing bits is:

- V-Swing 1 = 0
- V-Swing 0 = 1

Coarse Delay

All coarse delay elements used in the data, enable, and comparator paths are identical. The full scale delay range is equal to the period of PLL_CK, with 5 bit edge placement resolution.

TABLE 11.

T (PLL_CK)	CD Range	CD Resolution
10ns	9.6875ns	312.5ps
20ns	19.375ns	625ps

Coarse Falling Edge Adjust

All CFEA delay elements used in the data, enable, and comparator paths are identical. The full-scale delay range is equal to ±T/4, with 4-bit edge placement resolution.

TABLE 12.

T (PLL_CK)	CFEA Range	CFEA Resolution
10ns	–2.5ns to +2.1875ns	312.5ps
20ns	–5ns to +4.375ns	625ps

PLL Range

PLL_CK is allowed to vary between 50MHz and 100MHz.

$$50MHz \leq PLL\_CK \leq 100MHz$$

PLL Input Terminations

PLL_CK / PLL_CK* inputs have on-chip termination options which support 3 different termination schemes:

1. No termination (open circuit)
2. 100Ω across the differential inputs
3. 50Ω single ended termination.

All of these termination schemes may be realized without requiring any external resistors.

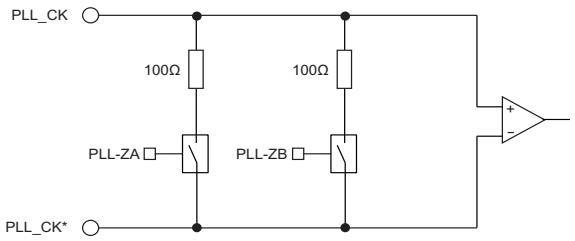


FIGURE 13.

The selection of any on-chip termination is made through the CPU port. PLL-ZA and PLL-ZB are the internal control bits which select the termination option. Their addresses are listed in the memory map tables.

TABLE 13.

PLL-ZA	PLL-ZB	Termination Option
0	0	No Termination
0	1	100Ω Differential
1	0	100Ω Differential
1	1	50Ω Single-Ended

100Ω Differential Termination

By selecting either, but not both, 100Ω terminators, a 100Ω resistance is connected between the differential inputs, thus cleanly terminating 50Ω transmission lines on the PCB without any external components.

50Ω Single-Ended Termination

Selecting both 100Ω terminators creates a single ended 50Ω termination. The inverting input then becomes the termination voltage for the input signal, and the appropriate termination voltage level must be applied to this pin.

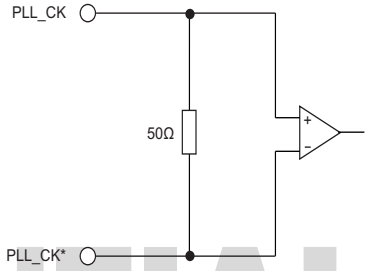


FIGURE 14.

Driver

Detailed Block Diagram

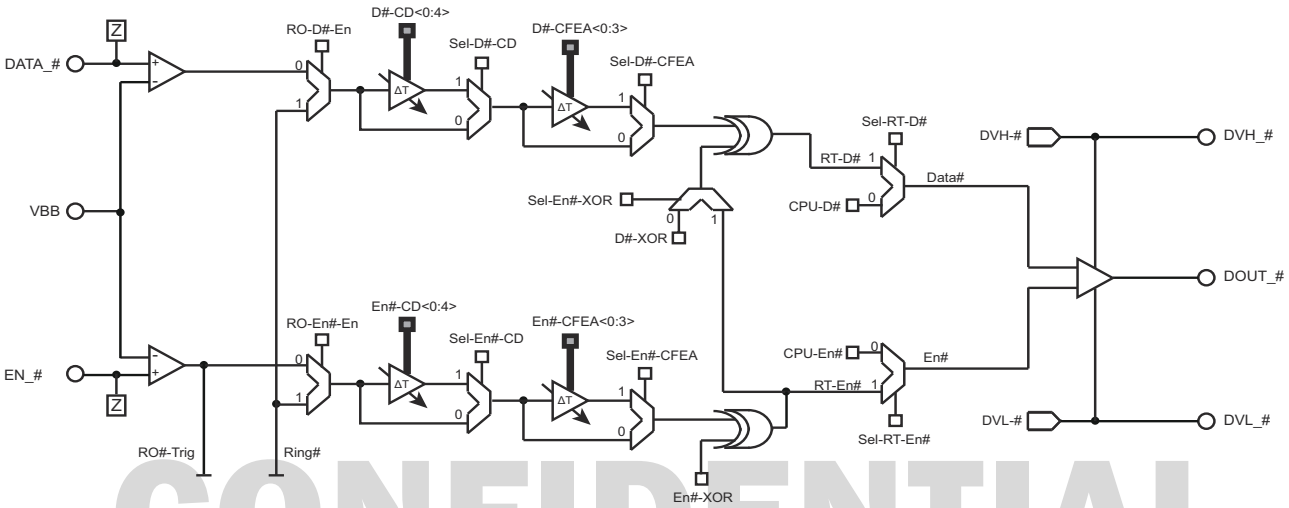


FIGURE 15.

Driver High Speed Digital Inputs

Each channel has two high speed single ended digital inputs, DATA and EN, which control the real time operation of the driver.

Universal Inputs

DATA_0 - DATA_7 and EN_0 - EN_7 are differential inputs whose inverting input is connected to VBB, an analog input voltage that establishes the threshold for the inputs. This programmable threshold capability allows the acceptance of most standard technologies which operate between VDD (+3.3V) and ground without requiring any external translation.

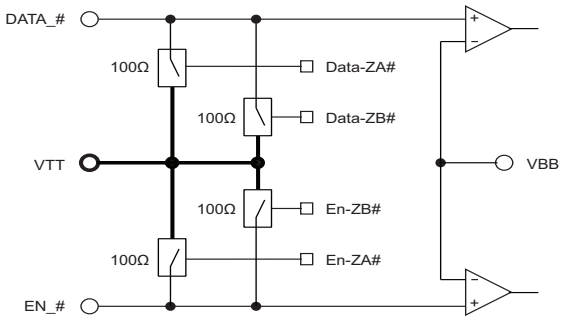


FIGURE 16.

Input Terminations

Each data and enable input may be terminated by:

- No input termination
- 100Ωto VTT
- 50Ω to VTT

TABLE 14.

Data-ZA#; En-ZA#	Data-ZB#; En-ZB#	Termination
0	0	None
0	1	100Ω to VTT
1	0	100Ω to VTT
1	1	50Ω to VTT

Ring Oscillator Mode

Each channel's data or enable path may be placed in a ring oscillator mode, where the comparator is fed back into the driver. This mode is used mainly for test and calibration purposes.

TABLE 15.

RO-D#-En	Data Source
0	DATA_#
1	Ring#

RO-En#-En	Enable Source
0	En_#
1	Ring#

Driver Timing Adjust

Each channel's high speed DATA and EN inputs have timing adjustment capability with the following characteristics:

1. Separate and independent delay circuitry for the DATA and EN paths
2. Separate and independent delay circuitry for each channel
3. Propagation delay adjust (both rising and falling edge Tpd are delayed equally)
4. Timing delay range and resolution established by an external frequency (PLL_CK)

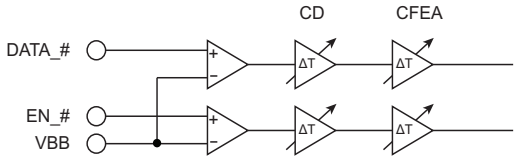


FIGURE 17.

Data and Enable Propagation Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

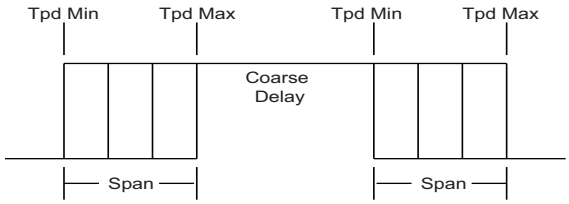


FIGURE 18.

Coarse Delay Adjust

The coarse delay circuitry divides the overall delay range (span) into 32 equal segments, and then selects one of those delays. The delay section may be bypassed via the CPU port.

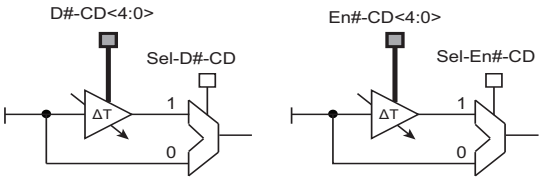


FIGURE 19.

TABLE 16.

CD<4:0>	PLL_CK	ΔTpd+, –
00000	X	ΔTpd+, – = 0
11111	T = 10ns	ΔTpd+, – = +9.6875ns Resolution = 312.5ps
11111	T = 20ns	ΔTpd+, – = +19.375ns Resolution = 625ps

TABLE 17.

Sel-D#-CD	Data Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Sel-En#-CD	Enable Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Power Reduction Mode

If the coarse delay is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse delay function.

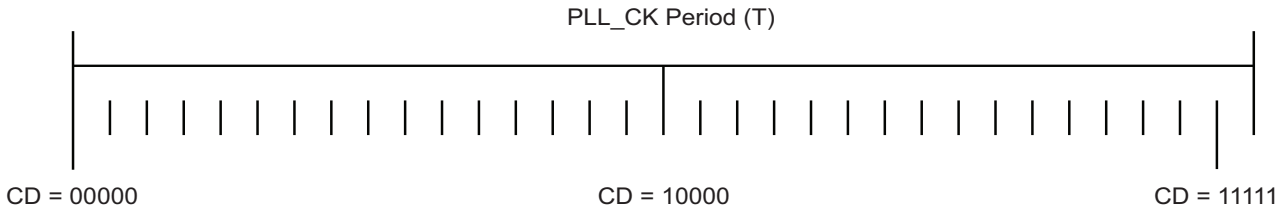


FIGURE 20. COARSE DELAY

Coarse Falling Edge Delay Adjust

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

Coarse falling edge adjust divides the overall delay range (span), set by the period of PLL_CK, into 16 equal segments, and allows the falling edge propagation delay of the signal to be modified from -8 to +7 segments.

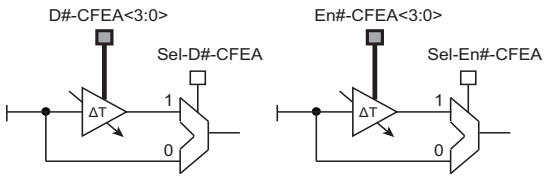


FIGURE 21.

The CFEA section may be bypassed by the select bit, which is set by the CPU port. The address of each select bit is listed in the memory map tables.

TABLE 18.

CFEA<3:0>	PLL_CK	ΔTpd –
0000 1000 1111	T = 10ns	Resolution = 312.5ps ΔTpd– = –2.5ns ΔTpd– = 0ns ΔTpd– = +2.1875ns
0000 1000 1111	T = 20ns	Resolution = 625ps ΔTpd– = –5.0ns ΔTpd– = 0ns ΔTpd– = +4.375ns

TABLE 19.

Sel-D#-CFEA	Data Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

Sel-En#-CFEA	Enable Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

Power Reduction Mode

If the coarse falling edge adjust section is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse FEA function.

Data and Enable Signal Processing Options

Once the driver Data and Enable signals pass through the deskew elements, several additional processing options exist:

1. Inverting the Data and Enable pattern
2. XORing Data and Enable
3. CPU control and over Data and Enable

The control lines to select and program these options are established by the CPU port, and are normally set up in advance of, and held static during, real time operation.

Pattern Inversion

The polarity of both Data and Enable may be independently inverted by an XOR gate located in series with the signal path. This feature is a convenient method of changing the polarity quickly without having to recompile any code.

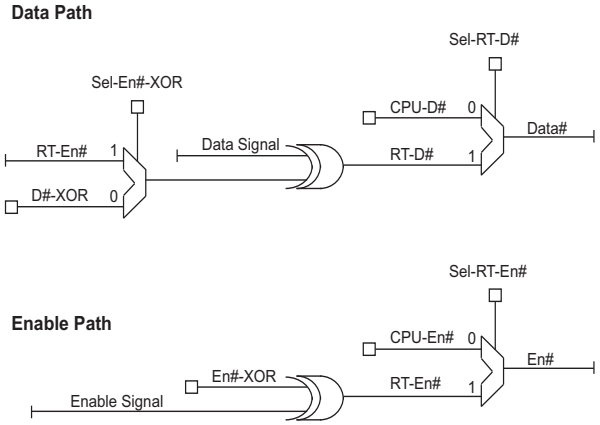


FIGURE 22.

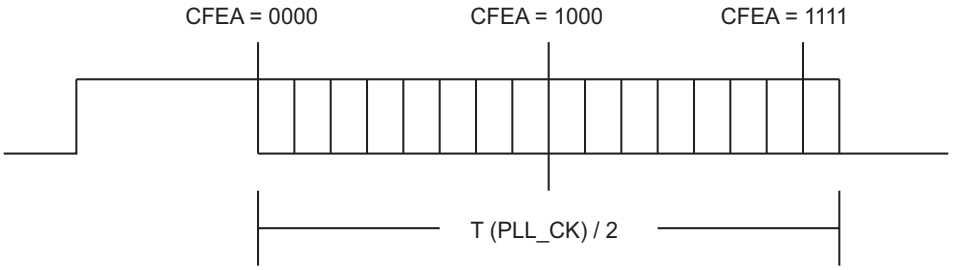


FIGURE 23. COARSE FALLING EDGE ADJUST

TABLE 20.

Sel-En#-XOR	D#-XOR	RT-D#
0	0	DATA_#
0	1	DATA_#*
1	X	Data# XOR En#

En#-XOR	RT-En#
0	EN_#
1	EN_#*

CPU Control

After all driver control signal processing is performed, Data and Enable enter one last stage, where the real time signals may be bypassed and the CPU port can take direct control over the driver. This final logic stage allows the CPU port to exercise driver control regardless of any real time inputs and is the default condition upon power up and reset.

TABLE 21.

Sel-RT-D#	Data # Source
0	CPU-D#
1	RT-D#

Sel-RT-En#	Enable # Source
0	CPU-En#
1	RT-En#

Driver Output Control

The driver has a 50Ω output impedance and is capable of forcing 2 voltage levels, DVH and DVL, as well as going into a high impedance state. The high and low voltage levels are supported by on-chip DC level generators with buffers and are programmed through the CPU port.

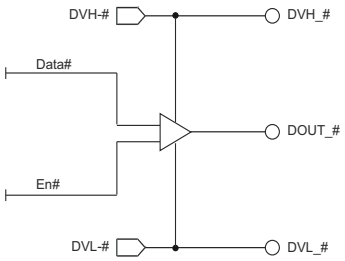


FIGURE 24.

TABLE 22.

En	Data	DOUT
0	X	HiZ
1	0	DVL
1	1	DVH

Driver Control Read Back

The status of the internal nodes Data# and En# may be read back directly via the CPU port. This read-only function is useful for a tester to be able to go out and check the driver inputs at any time.

Output Impedance

The driver is designed to maintain constant output impedance regardless of any changes due to:

1. ambient temperature
2. part to part variation

by tracking a precision and temperature compensated off-chip resistor (R_EXT) with a ratio of 204:1. Nominal conditions are:

R_EXT = 10.00 KΩ

Rout = 49Ω.

Output Impedance Adjustments

The driver output impedance tracks R_EXT equally for DVH and DVL levels. However, it is possible to make fine adjustments to Rout for each drive level separately. This independent adjustment is useful for calibrating waveforms in precision applications and may be used to accommodate any transmission line impedance errors on a load board, as well as to adjust a characteristic in a waveform's DVH vs. DVL performance, without affecting its characteristics when driving the other level.

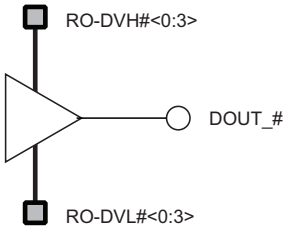


FIGURE 25.

Fine control is programmed through the CPU port, and is normally set up before the execution of any real time patterns. The default condition (reset, power up) is Radj = 0Ω.

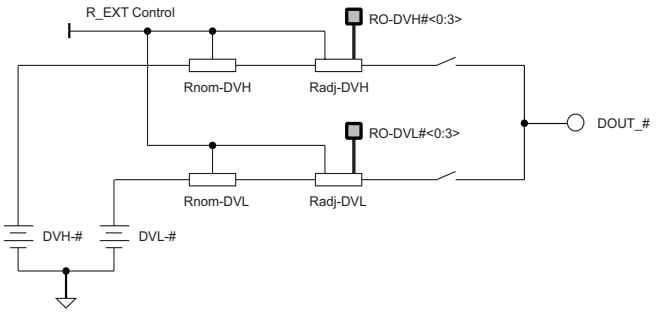


FIGURE 26.

R-nom-DVH and Rnom-DVL track R_EXT equally for all channels. RO-DVH and RO-DVL allow independent per channel adjustments.

Adjustment Range

Each level has a fine adjustment range of ± 10%, or ± 5Ω for R_EXT = 10 kΩ. The total output impedance of the driver is the nominal output impedance plus the fine adjustment.

Rnom = R_EXT / 204 = 10.0 KΩ / 204 = 49Ω

Radj = ± 10% = ± R_EXT / 2,000

Rout = Rnom + Radj = R_EXT / 204 ± R_EXT / 2,000

TABLE 23.

RO-DVH<3:0> RO-DVL<3:0>	Radj-DVH Radj-DVL	Radj-DVH Radj-DVL
0111	+8.92%	+4.375Ω
0110	+7.65%	+3.75Ω
0101	+6.38%	+3.125Ω
0100	+5.1%	+2.5Ω
0011	+3.83%	+1.875Ω
0010	+2.55%	+1.25Ω
0001	+1.28%	+0.625Ω
0000	0%	0Ω
1111	–1.28%	–0.625Ω
1110	–2.55%	–1.25Ω
1101	–3.83%	–1.875Ω
1100	–5.1%	–2.5Ω
1011	–6.38%	–3.125Ω
1010	–7.65%	–3.75Ω
1001	–8.92%	–4.375Ω
1000	–10.2%	–5.0Ω

The numbers in the table are based upon R_EXT = 10.0kΩ.

High Impedance

There are two distinct driver HiZ modes:

1. Fast HiZ
2. Slow Hiz

Fast HiZ

Fast HiZ is used during high speed functional test patterns where the driver is forcing DVH or DVL when enabled. In Fast HiZ, the driver maintains low leakage between VEE and VCC. For DOUT voltages more positive than VCC, the high speed driver starts to turn on. Driver transition times going into and out of high impedance are quicker and more accurate when the driver is in Fast HiZ mode than when in Slow HiZ mode.

It is acceptable and legal for the DUT to exceed VCC in Fast HiZ mode, but the DUT will see a 50Ω load to VCC + 1.25V once that voltage is exceeded. No damage will be done to the driver when it is placed in this condition, as long as DOUT stays below VCCH.

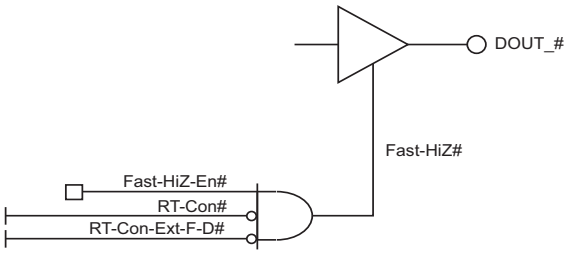


FIGURE 27.

Slow HiZ

In Slow HiZ, the driver maintains a very low leakage current when DOUT is between VEE and VCCH, and therefore the DOUT pin has a wider HiZ voltage compliance range. Slow HiZ is the default state upon power up or reset.

Slow HiZ is selected for a particular channel whenever:

1. Reset or power up occurs
2. CPMU-F is connected to DOUT
3. EXT_FORCE is connected to DOUT
4. The CPU port forces this condition

It may be desirable to force Slow HiZ when the Comparator is testing a large positive voltage in excess of VCC. In Slow HiZ, the driver functions the same as in Fast HiZ, but the driver transition times into and out of HiZ, as well as driver minimum pulse widths, will be slightly slower.

TABLE 24.

Fast-HIZ-En#	RT-Con#	RT-Con-Ext-F-D#	DOUT_# HIZ
0	X	X	Slow HiZ
X	1	X	Slow HiZ
X	X	1	Slow HiZ
1	0	0	Fast HiZ

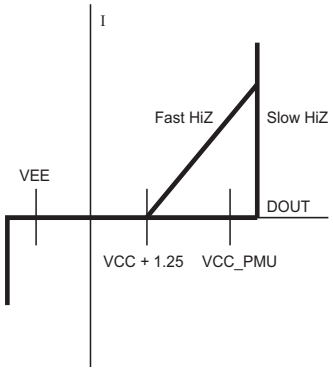


FIGURE 28.

Comparator

Detailed Block Diagram

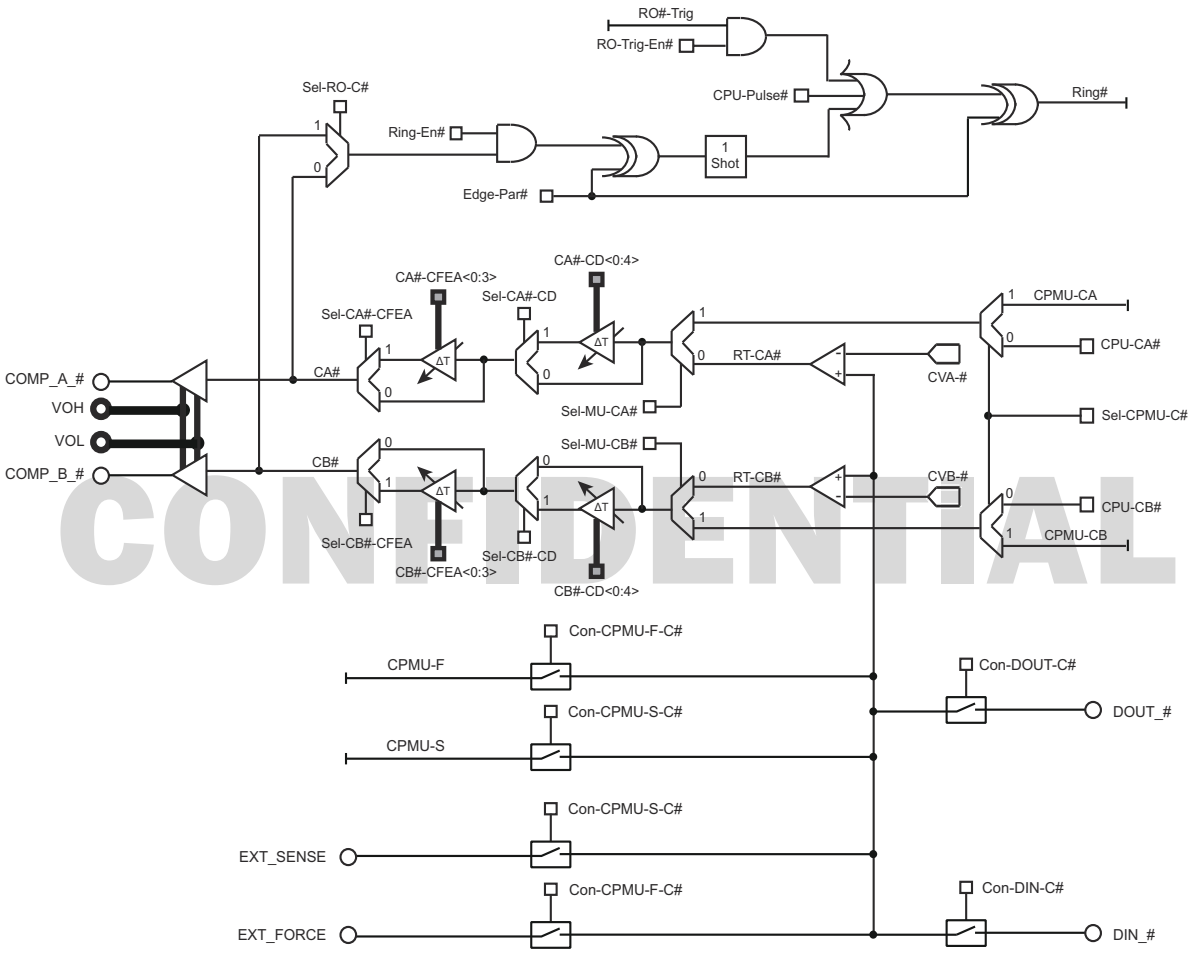


FIGURE 29.

Comparator Overview

The comparator section is used to monitor, measure, and track all activity on the DIN or the DOUT pin. Each channel has a high speed functional dual comparator (Comp_A and Comp_B) with its own independent on-chip threshold generation (CVA and CVB) used to provide real time status of the DUT. The functional comparator maintains extremely low input leakage current when DIN is between the power supply rails VEE and VCCH.

Parametric Comparator

There is one central parametric measurement unit (CPMU) that also has a dual comparator with independent thresholds (CVA-CPMU and CVB-CPMU). The CPMU comparator outputs may be independently routed through any channel's high speed functional comparator paths.

Timing Adjust

Each channel has the ability to adjust the propagation delay and pulse width of the CompA and CompB signals, allowing timing system level timing calibration.

Internal State Readback

Direct access to the internal comparator states RT-CA, RT-CB, CPMU-CA, and CPMU-CB is provided via the CPU port. This access is useful for diagnostic purposes and for any application where DUT status is required without using any error processing circuitry.

Source Selection

There are three sources of comparator signals that may be sent off-chip via the COMP_A and COMP_B outputs for each channel:

1. CPU programmed states
2. Central Parametric Measurement Unit Comparator
3. Functional Comparator

CPU Source Control

The CPU port can set the Compator A and Comparator B status and override any real time input from the CPMU or the high speed functional comparator. This CPU control allows the comparator outputs to be placed in a known state, typically for diagnostic and debugging purposes within a tester. Each channel has separate comparator source selection capability.

TABLE 25.

Sel-CPMU-C#	Comparator CPMU Source
0	CPU Port (CPU-CA#, CPU-CB#)
1	Measurement Unit (CPMU-CA, CPMU-CB)

Functional vs. Measurement Unit Control

Once the source of the measurement unit is selected, each channel may then select either the functional comparator or the measurement unit comparator for that channel's COMP_A and COMP_B signal sources. This source selection is performed separately for comparator A and B of the same channel to allow both functional and parametric information to be simultaneously present at the real time comparator outputs.

TABLE 26.

Sel-CPMU-CA(B)#	Ch# Comparator A(B) Source
0	Ch# Functional Comparator (RT-CA(B)#)
1	CPMU or CPU (MU-CA(B)#)

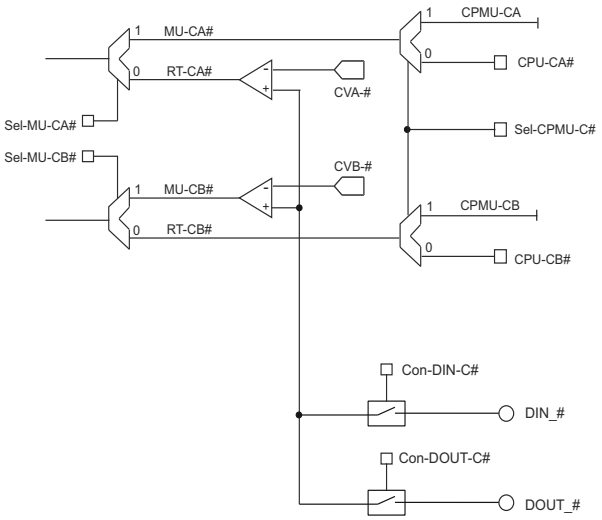


FIGURE 30.

Timing Adjust

Each channel's COMP_A and COMP_B outputs have timing adjustment capability with the following characteristics:

1. Separate and independent delay circuitry for the COMP_A and COMP_B paths
2. Separate and independent delay circuitry for each channel
3. Propagation delay adjust (both rising and falling edge Tpd are delayed equally)
4. Timing delay range and resolution established by an external frequency (PLL_CK.)

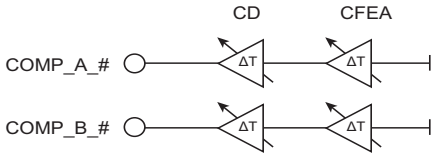


FIGURE 31.

Coarse Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd-) in equal amounts. Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

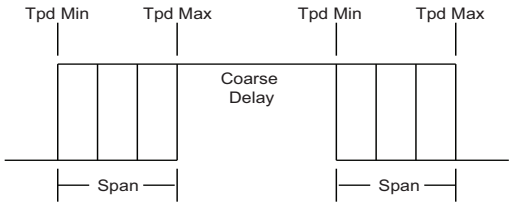


FIGURE 32.

The coarse delay circuitry divides the overall delay range (span) into 32 equal segments, then selects one of those delays. The delay section may be bypassed via the CPU port.

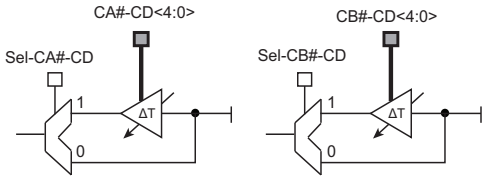


FIGURE 33.

TABLE 27.

CD<4:0>	PLL_CK	ΔTpd+,–
00000	X	ΔTpd+,– = 0
11111	T = 10ns	ΔTpd+,– = +9.6875ns Resolution = 312.5ps
11111	T = 20ns	ΔTpd+,– = +19.375ns Resolution =625ps

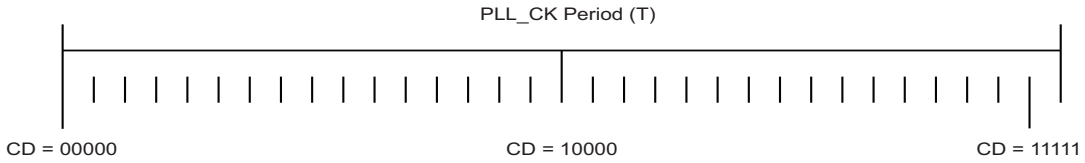


FIGURE 34. COARSE DELAY

TABLE 28.

Sel-CA#-CD	Comp A Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Sel-CB#-CD	Comp B Coarse Delay
0	Coarse Delay Bypassed, Powered Down
1	Coarse Delay Active, Powered Up

Power Reduction Mode

If the coarse delay section is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse delay function.

Coarse Falling Edge Delay Adjust

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd-) while having no effect on the rising edge (Tpd+). Propagation delay adjustment is typically used for removing any pulse width distortion inside a tester.

Coarse falling edge adjust divides the overall delay range (span), set by the period of PLL_CK, into 16 equal segments, and allows the falling edge propagation delay of the signal to be modified from -8 to +7 segments.

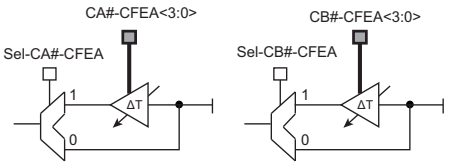


FIGURE 35.

The FEA section may be bypassed by the select bit, which is set by the CPU port. The address of each select bit is listed in the memory map tables.

TABLE 29.

CD<4:0>	PLL_CK	ΔTpd–
0000 1000 1111	T = 10ns	Resolution = 312.5ps ΔTpd– = –2.5ns ΔTpd– = 0ns ΔTpd– = +2.1875ns
0000 1000 1111	T =20ns	Resolution = 625ps ΔTpd– = –5.0ns ΔTpd– = 0ns ΔTpd– = +4.375ns

TABLE 30.

Sel-CA#-CFEA	Comp A Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

Sel-CB#-CFEA	Comp B Coarse Falling Edge Adjust
0	Coarse FEA Bypassed, Powered Down
1	Coarse FEA Active, Powered Up

Power Reduction Mode

If the coarse falling edge adjust section is completely bypassed, the power to the delay cells is shut off and the total chip power consumption is reduced. This feature is useful in applications that do not require the coarse FEA function.

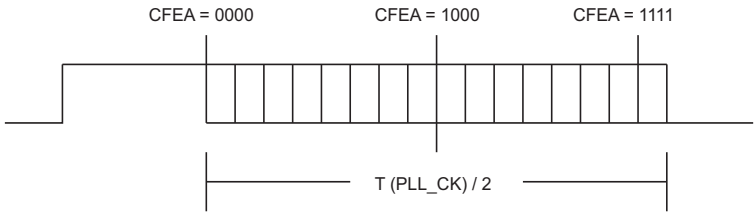


FIGURE 36. COARSE FALLING EDGE ADJUST

Output Stage

Each channel supports two comparator outputs (COMP_A and COMP_B) with the following characteristics:

1. Single ended outputs
2. 50Ω series terminated outputs
3. Programmable high and low levels.

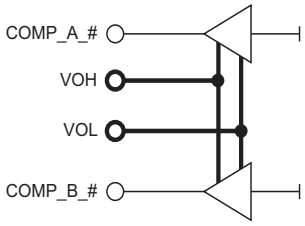


FIGURE 37.

Comparator Output Supply Levels

VOH and VOL are voltage power supply inputs that set the high and low level of COMP_A and COMP_B. VOH and VOL provide the current required to drive the off-chip transmission line, and any DC current associated with any termination used. Therefore, these inputs should be driven by a low impedance and low inductance source with ample current drive.

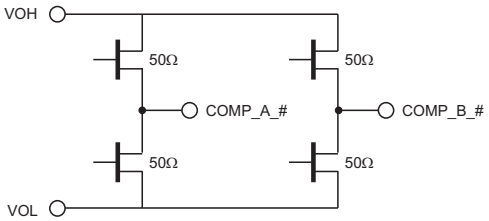


FIGURE 38.

Comparator Source Termination

In this configuration no external components are required and a full amplitude signal is realized at the destination.

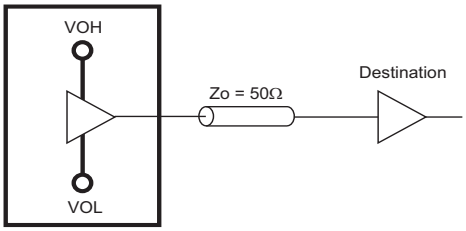


FIGURE 39.

Comparator Source and Destination Termination

In this configuration one external component is required and a 50% amplitude signal is realized at the destination.

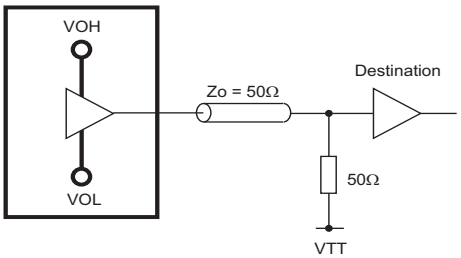


FIGURE 40.

Ring Oscillator

Each channel has test and characterization mode circuitry that places the channel into a ring oscillator mode by feeding back the comparator outputs into the driver inputs. All ring oscillator control lines and modes are independent per channel.

Source Selection

Either comparator output may be selected and fed into either the DATA or EN signal paths.

TABLE 31.

Sel-RO-C#	Feedback Source
0	CA#
1	CB#

Ring Oscillator Enable

The CPU port may enable or disable the ring oscillator mode.

TABLE 32.

Ring-En#	RO Mode
0	Disabled
1	Enabled

Ring Oscillator Edge Parity

The ring oscillator may be positive or negative edge controlled, as selected by the CPU port. A 1-shot in series with the ring insures that a consistent pulse width is generated every time, but the direction of the transition that fires the 1-shot is determined by the Edge-Par# signal.

TABLE 33.

Edge-Par#	Trigger Edge Polarity
0	Positive
1	Negative

Ring Oscillator Start Up

The start-up pulse to activate the ring oscillator can come from two sources:

1. the real time enable input
2. the CPU port

CPU-Pulse# is a one shot pulse generated by writing to the CPU port at the CPU-Pulse# address. When placed in RO mode, one instance of this write transaction will initiate oscillation.

Or, the real time enable input (EN_#) may be used to start up oscillation by injecting 1 narrow pulse (~10 ns to 15 ns). RO-Trig-EN# = 1 activates and enables this start up path.

Ring Oscillator Configuration

When the ring oscillator is used to examine the timing delay of the Enable path, it is usually best to route the RT-EN# signal through the Data path XOR gate, so the Enable path controls the Data input to the driver.

Recommended configuration:

<u>EN as the driver data source:</u>

DATA_# = 0

Sel-En-XOR = 1

En#-XOR = 0

<u>Driver enabled:</u>

Sel-RT-En# = 0

CPU-En# = 1

In this configuration, the enable path carries the pattern information to the driver data input.

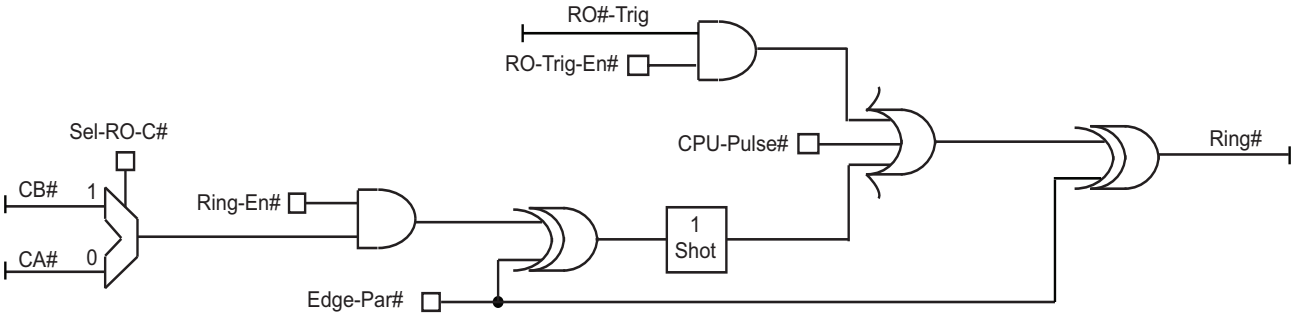
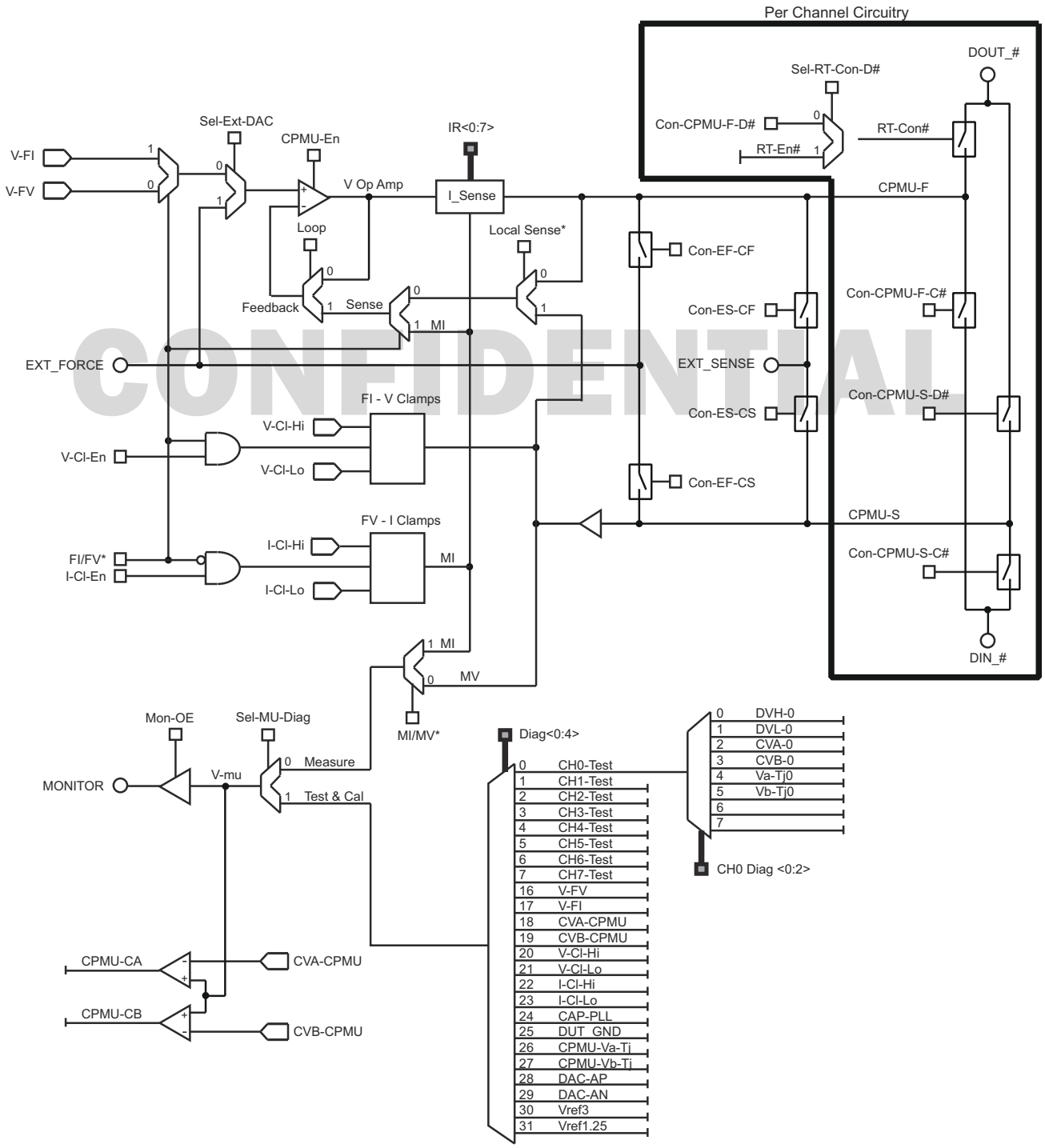


FIGURE 41.

CPMU

Detailed Block Diagram



CPMU Overview

There is one Central Parametric Measurement Unit (CPMU) with the ability to:

- Force Voltage
- Measure Voltage
- Force Current
- Measure Current

The current or voltage measured may be tested via two paths:

- On board CPMU dual comparator
- MONITOR analog voltage output

Each channel may connect to the CPMU and may route the CPMU dual comparator outputs through its COMP_A and COMP_B outputs.

CPMU High Impedance

The CPMU may be placed in an off-state, where it maintains a high impedance between the supply voltages VCCH and VEE. However, it is NOT recommended that the forcing op amp be placed in a high impedance state due to the large transient response when becoming active.

TABLE 34.

CPMU-En	CPMU
0	HiZ
1	Active

Current Ranges

The CPMU can force and sense current up to a maximum of 32mA. In order to achieve the maximum accuracy while measuring lower currents, 8 current ranges are supported:

IR0 – 2µA
IR1 – 8µA
IR2 – 32µA
IR3 – 128µA
IR4 – 512µA
IR5 – 2mA
IR6 – 8mA
IR7 – 32mA

The current range is selected and controlled by the internal registers IR0 through IR7, which are set through the CPU port.

Each range select bit has independent control, allowing a wide variety of make or break combinations when changing current ranges. This flexibility is useful in controlling the transient response of the CPMU over a wide variety of DUT environments.

Activating more than one range simultaneously will have the effect of placing the sense resistors in parallel, thus altering the transfer function. Activating more than one range at the same time is NOT recommended for taking measurements, but may be useful to control the transient response when changing ranges or modes.

Voltage Force

In FV mode, the forced voltage source may be selected from either the on-board DC level V-FV or the voltage present at the external force pin.

TABLE 35.

Sel-Ext-DAC	V Force Source
0	V-FV
1	EXT_FORCE

In this mode, there is a 1:1 correspondence between the voltage source and the forced voltage at DOUT.

CPMU = V-FV or CPMU = EXT_FORCE

Current Force

In FI mode, the forced current voltage source may be selected from either the on-chip DC level V-FI or the voltage present at the external force pin.

TABLE 36.

Sel-Ext-DAC	I Force Source
0	V-FI
1	EXT_FORCE

In this mode, the current forcing voltage source has the following transfer function.

TABLE 37.

V-VI	Current at CPMU
–1V	–Imax
0V	0
+1V	+Imax

CPMU Operating Mode

The decision whether to force current or voltage, or to measure current or voltage, is controlled by internal registers FI/FV* and MI/MV* and are programmed via the CPU port.

TABLE 38.

FI/FV*	CPMU Function
0	Force Voltage
1	Force Current

MI/MV*	CPMU Function
0	Measure Voltage
1	Measure Current

There are no restrictions between what is forced and what is measured. All 4 combinations are possible:

FI/MI

FI/MV

FV/MI

FV/MV

Measurement Unit

There are several ways in which the CPMU can test, monitor, and measure either the voltage or current at either DOUT or DIN of one of the channels.

An on-board window comparator allows 2 bit "Go/No Go" testing. V-mu is the voltage output of the measurement unit, and it corresponds either to the voltage present or the current flowing through one of the DOUT or DIN pins. V-mu is the input to the CPMU window comparator, whose thresholds are set with on-chip DC levels through the CPU port.

The window comparator outputs CPMU-CA and CPMU-CB may be read back through the CPU port, granting direct access to the actual comparator states at any time. It is also possible to route CPMU-CA and CPMU-CB to the COMP_A and COMP_B outputs, and process the CPMU comparator results as a real time test vector.

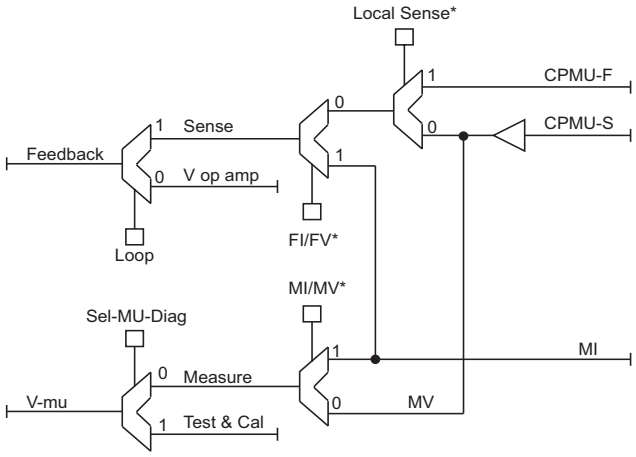


FIGURE 42.

Loop Control

The forcing loop may be configured as a unity gain closed loop that places the forcing op amp into a known and safe state, regardless of the conditions at the selected DOUT or DIN pin.

Sense Options

The sense path is used to precisely control either the voltage or the current present at the selected DOUT or DIN pin.

TABLE 39.

Loop	FI/FV*	Local Sense*	Feedback
0	X	X	V Op Amp
1	1	X	MI
1	0	0	CPMU-F
1	0	1	CPMU-S

Measure Options

The measurement unit (MU) has independent control over whether to measure the current or the voltage of the selected pin. In addition, the MU can connect to an internal test node, typically used for test and characterization.

TABLE 40.

Sel-MU-Diag	MI/MV*	V-mu
1	X	Test & Cal
0	1	MI
0	0	CPMU-S

Monitor

MONITOR is a wide voltage analog output whose voltage source is the measurement unit output (V-mu).

TABLE 41.

Mon-OE	MONITOR
0	HiZ
1	V-mu

MONITOR may be placed into a high impedance state by setting Mon-OE to a low state. This HiZ feature is useful when connecting together multiple MONITOR pins from multiple ICs into one A to D converter, without having to construct an off-chip analog multiplexer.

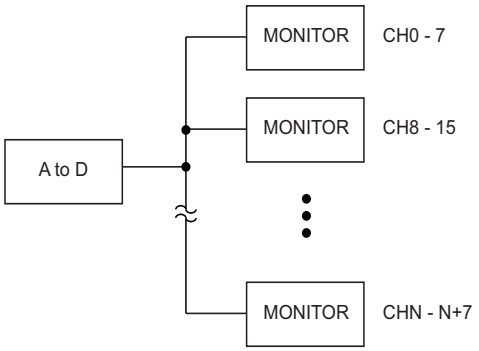


FIGURE 43.

When measuring voltage, MONITOR has a 1:1 transfer function with DIN. When measuring current, MONITOR varies between -1V and +1V for -Imax and +Imax.

TABLE 42.

Mode	MONITOR	DOUT
MV	DIN	DIN
MI	–1V 0V +1V	–Imax 0 +Imax

Diagnostics

The CPMU has access to key internal nodes so that the voltage on these nodes may be monitored. This access is typically used for testing and diagnostic purposes. Some parameters are accessible on a per channel basis.

PER CHANNEL DIAGNOSTIC SELECTION

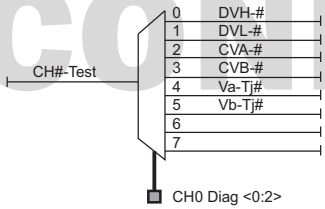


FIGURE 44.

Other test parameters (those associated with the CPMU) are accessible on a central basis only.

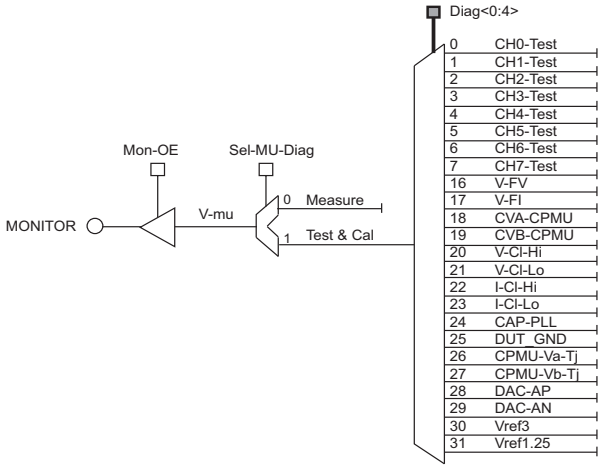


FIGURE 45.

The CPU port has ultimate control over which parameter is selected for the measurement unit signal, which routes to the dual comparator and the MONITOR output.

TABLE 43.

Sel-MU-Diag	MU-Source
0	Measure (MV or MI)
1	Test & Cal

Temperature Sensing

Each channel has its own independent temperature sense capability. There are 2 test voltages (Va-Tj and Vb-Tj) generated on-chip which allow the calculation of the junction temperature. The equation to calculate the junction temperature is:

$$Tj = \{(Va\text{-}Tj - Vb\text{-}Tj) * 1{,}637\} - 221\ °C$$

Va-Tj and Vb-Tj must be read back separately through the CPMU for the calculation to be performed.

FI Voltage Clamps

The CPMU has programmable voltage clamps that limit the voltage swing at the DUT when the CPMU is forcing current. These clamps can be used to protect the DUT when current is being forced into a high impedance node at the DUT.

The clamps may be turned off by setting V-Cl-En = 0, in which case the clamps will remain high impedance between the supply voltages VCC_PMU and VEE.

TABLE 44.

FI/FV*	V-Cl-En	Clamps
0	X	HiZ
1	0	HiZ
1	1	Active

When active, the clamps sense the voltage at CPMU-S. If CPMU-S is within the limits of the high and low clamps, no action is taken. If CPMU-S exceeds the high or low voltage clamp, the CPMU reduces the output current in order for the output voltage to not exceed the clamp. If the voltage at CPMU-S subsequently drops back to within the clamp levels, the CPMU resumes sourcing or sinking its programmed current.

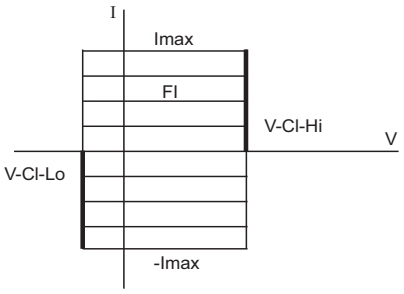


FIGURE 46.

The FI voltage clamps do not function when the PMU is using the tight loop or the local sense feedback point.

FV Current Clamps

The CPMU has programmable current clamps that limit the current when the CPMU is forcing a voltage. These clamps are useful in protecting the DUT from an over current situation.

The clamps may be disabled by setting I-Cl-En = 0.

TABLE 45.

FI/FV*	I-Cl-En	I-Clamps
1	X	Disabled
0	0	Disabled
0	1	Active

When Active, the I-Clamps sense the current. If the current is within the boundaries set by I-Cl-Hi and I-Cl-Lo, no action is taken. If the measured current exceeds the upper or lower current clamp, the CPMU reduces the output voltage in order for the output current to not exceed the clamp. If the current subsequently drops back to within the clamp levels, the PPMU resumes forcing its programmed voltage.

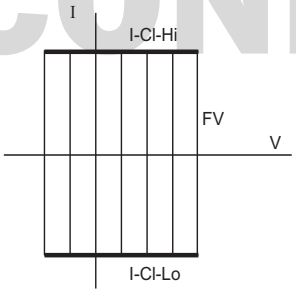


FIGURE 47.

On-Chip Switch Options

CPMU TO DIN CHANNEL CONNECTION

The CPMU can be connected to one or multiple DIN pins simultaneously via the CPU port. Each channel has its own control bit which connects the CPMU to the DIN pin. Care must be exercised to make sure that multiple connections do not occur unless that is the desired configuration.

TABLE 46.

Con-CPMU-F-C#	DIN_# to CPMU-F
0	Disconnected
1	Connected

Con-CPMU-S-C#	DIN_# to CPMU-S
0	Disconnected
1	Connected

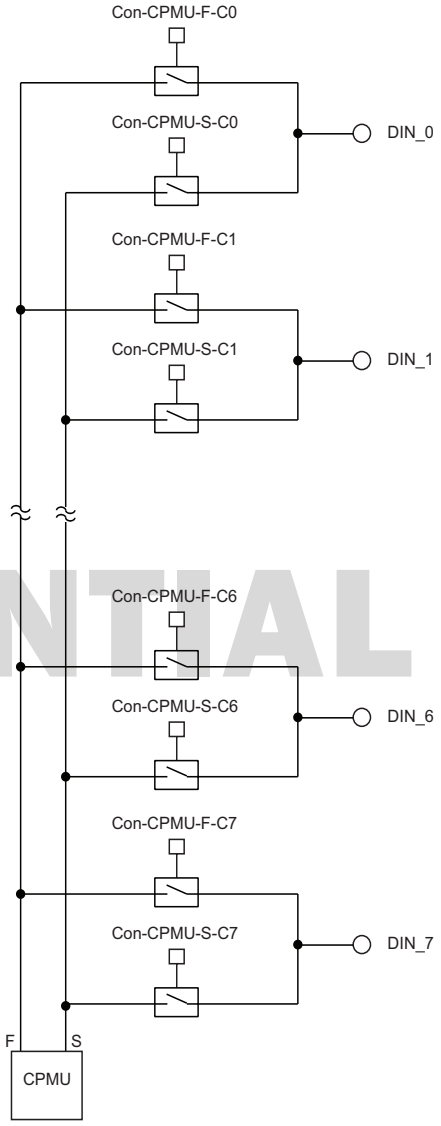


FIGURE 48.

CPMU TO DOUT CHANNEL CONNECTION

The DOUT_# pins have two methods of connecting to the CPMU:

1. CPU Control
2. Real Time Control

There are no restrictions since the CPMU may be connected to any and all channels simultaneously.

CPU Control

The default condition is CPU control. In this mode, the CPU port can connect or disconnect the CPMU to any DOUT_# pin by setting Con-CPMU-F-D# = 1.

Real Time Control

By setting Sel-RT-Con-F-D# = 1, the Enable signal for each path may be selected to connect and disconnect the CPMU to each DOUT_# pin. The RT-En# signal is inverted, allowing for automatic CPMU connectivity to DOUT_# whenever the driver goes into HiZ.

TABLE 47.

Sel-RT-Con-D#	Con-CPMU-F-D#	RT-En#	CPMU-F to DOUT_#
0	0	X	Disconnected
0	1	X	Connected
1	X	0	Connected
1	X	1	Disconnected

Real Time CPMU Control Applications

There are several uses for connecting and disconnecting the CPMU to any particular channel during real time operation. Two common applications are:

1. Super Voltage
2. HiZ Force

Super Voltage

Super Voltage is a very large positive voltage with a slow rise time that is applied to the DUT during test and characterization and is typically associated with flash memory devices. Real time CPMU connectivity allows the driver to go into and out of super voltage from either a high or a low state, with no restrictions. By selecting different CPMU current ranges, the rise time may be adjusted over a very wide dynamic range.

HiZ Force

HiZ force is controlled in the exact same manner as is super voltage, but is used to place the transmission line between the DUT and the pin electronics to a known value, rather than allow it to float at an uncontrolled voltage level. When the driver goes into HiZ, the transmission line will move toward the CPMU voltage. The selected current range will determine how quickly the transmission line will reach the programmed voltage.

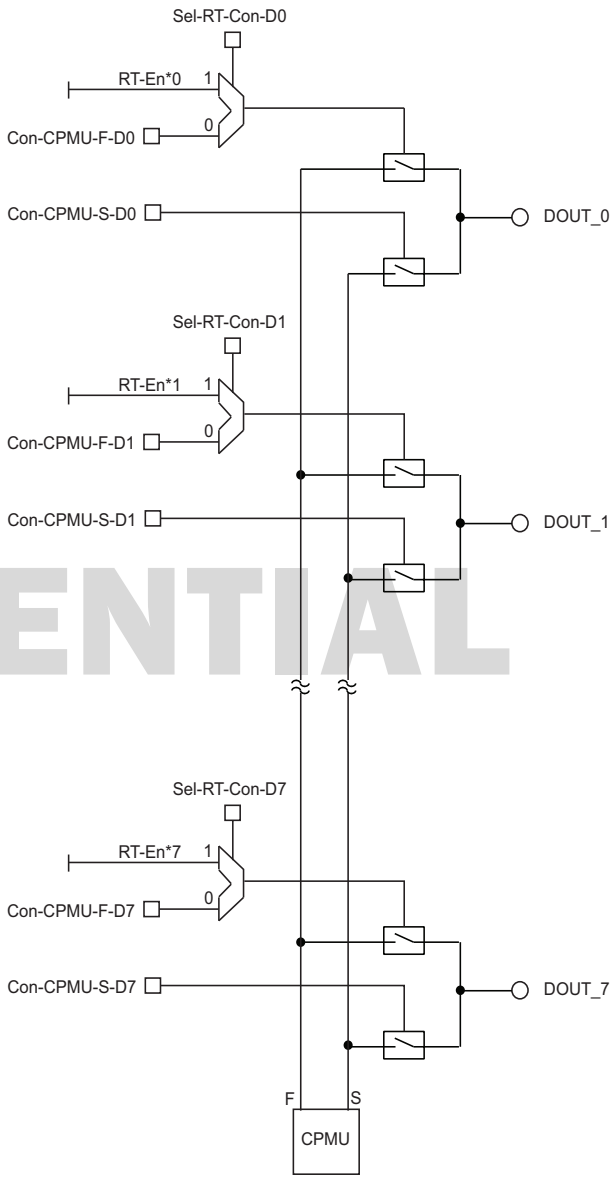


FIGURE 49.

External Force / Sense to DIN

There is a separate control bit for each channel's external force and sense connection to DIN. Therefore it is possible to connect the EXT_FORCE or EXT_SENSE pins to multiple DIN pins simultaneously. Care must be exercised to make sure that multiple connections do not occur unless that is the desired configuration.

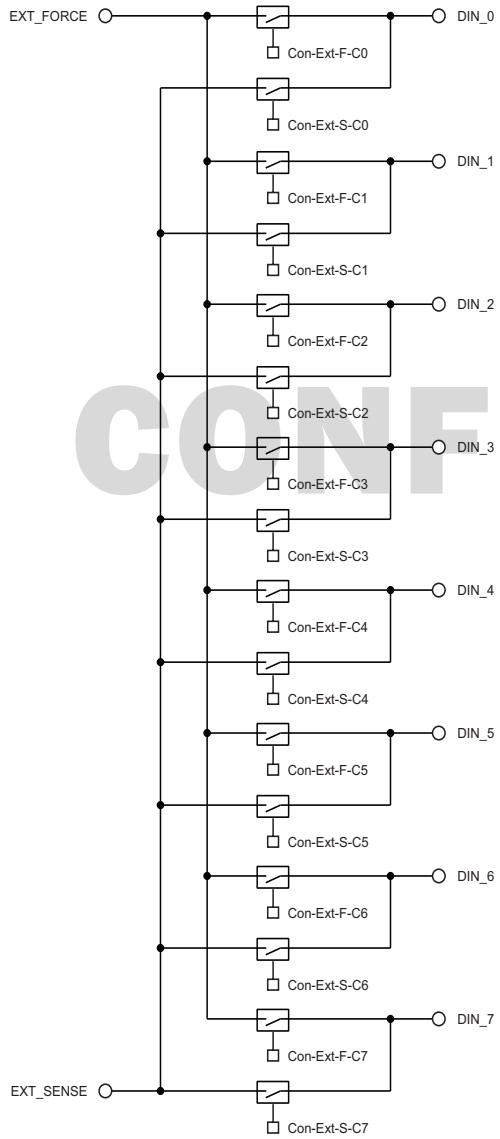


FIGURE 50.

TABLE 48.

Con-Ext-F-C#	EXT_FORCE to DIN_#
0	Open
1	Connected

Con-Ext-S-C#	DIN_# to EXT_SENSE
0	Open
1	Connected

External Force / Sense to CPMU

The EXT_FORCE and EXT_SENSE pins may be directly connected to the CPMU Force (CPMU-F) and CPMU Sense (CPMU-S) nodes without connecting to any DOUT or DIN pins.

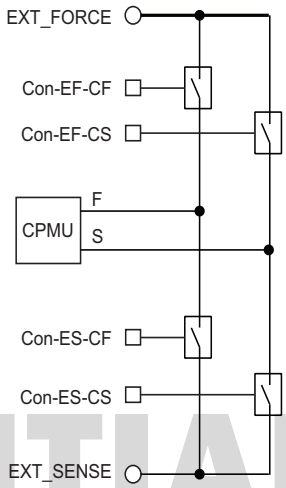


FIGURE 51.

TABLE 49.

Con-EF-CF	EXT_FORCE to CPMU-F
0	Open
1	Connected

Con-EF-CS	EXT_FORCE to CPMU-S
0	Open
1	Connected

Con-ES-CF	EXT_SENSE to CPMU-F
0	Open
1	Connected

Con-ES-CS	EXT_SENSE to CPMU-S
0	Open
1	Connected

External Force / Sense to DOUT

There is a separate control bit for each channel's external force and sense connection to DOUT. Therefore, it is possible to connect the EXT_FORCE or EXT_SENSE pins to multiple DOUT pins simultaneously. Care must be exercised to make sure that multiple connections do not occur unless that is the desired configuration.

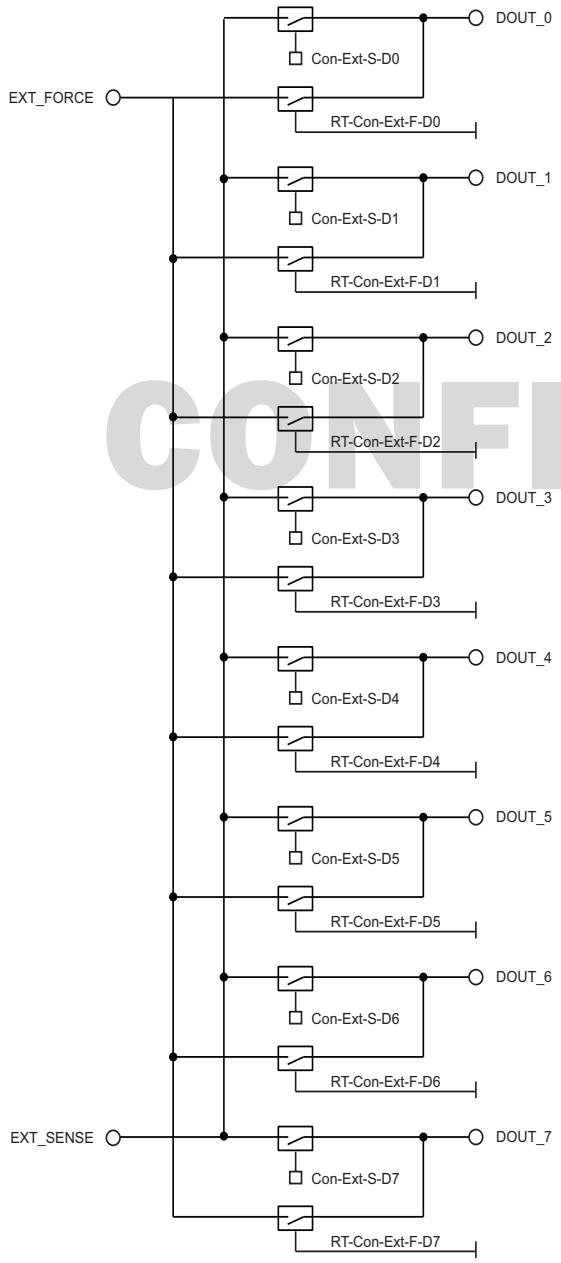


FIGURE 52.

Real Time Force Connection

EXT_FORCE may be connected and disconnected under real time control. The CPU port can configure the EN signal to open and close the connection between EXT_FORCE and DOUT.

TABLE 50.

Sel-RT-Ext-F-D#	RT-En#*	Con-Ext-F-D#	RT-Con-Ext-F-D#	EXT_FORCE to DOUT#
0	X	0	0	Disconnected
0	X	1	1	Connected
1	0	X	0	Disconnected
1	1	X	1	Connected

TABLE 51.

Con-Ext-S-D#	DOUT_# to EXT_SENSE
0	Disconnected
1	Connected

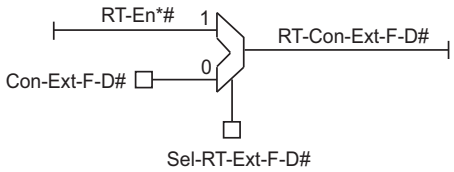


FIGURE 53.

DC Levels

Every functional block requires a variety of DC voltage levels in order to function properly. These levels are all generated on-chip with a 16-bit DAC that is programmed through the CPU port.

There are 4 voltage range options. Various DC levels are grouped together, and the selected voltage range is common for all levels within each group.

The realizable voltage range is restricted by the power supply levels and headroom limitations, especially in VR2. If a level is programmed beyond the recommended operating conditions, saturation will occur and the actual DC level will not match the desired programmed level.

Voltage Range Options vs. Function

Within each DAC group, the voltage range selection is common and is programmed via the CPU port.

CVA-PPMU and CVB-PPMU should only use the IR range when measuring current (MI), and only use VR0, VR1, or VR2 when measuring a voltage (MV).

TABLE 52.

Range Select<1:0>	Voltage Range	Output Voltage Swing	Resolution (LSB)	FS (Full Scale)	Vmid
0	VR0	–.5V to +3.5V	61µV	4	+1.5V
1	VR1	–1V to +7V	122µV	8	+3.0V
2	VR2	–2V to +14V	244µV	16	+6.0V
3	VIR	–1V to +1V	30.5µV	2	0V

Level Programming

Voltage ranges VR0, VR1 and VR2 use the equation:

$$Vout = (Value - Vmid) \bullet Gain + Offset + Vmid + DUT\_GND$$

Current force mode (VIR) uses the equation:

$$Vout = (Value - Vmid) \bullet Gain + Offset + Vmid$$

Value is described by the equation:

$$Value = \{(DAC\ Code) / (2^{N} - 1)\} \bullet FS + Vmid - (FS / 2)$$

$$N = 16;\ 2^{N} - 1 = 65{,}535$$

The voltage range lower and upper limits are:

$$Vmin = Vmid - (FS / 2)$$

$$Vmax = Vmin + FS$$

Level Reference

All DC voltage levels are referenced to GND.

Offset and Gain

Each individual DC level has an independent 13-bit offset and gain correction. These correction values allow the desired output level to be loaded simultaneously across multiple pins without having to correct for per pin errors.

TABLE 53.

Offset Code	Offset Value	Gain Code	Gain Value
0000H	–5.4% of FS	0000H	0.875
7FFFH	0	7FFFH	1.0
FFFFH	+5.4% of FS	FFFFH	1.125

Device Under Test Ground

The actual ground reference level at the DUT may be different than that used by the DAC reference. DUT_GND is a high impedance analog voltage input that provides a means of tracking the destination ground, and making an additional offset to the programmed level so the programmed level is correct with respect to the DUT. DUT_GND is superimposed upon all channels.

The input at DUT_GND should be:

1. filtered for noise
2. stable
3. reflect the actual ground level at the DUT

DUT_GND is NOT added into the DC level when forcing or measuring a current by the PPMU.

V_REF

V_REF is an analog input voltage that is used to program the on-chip DC levels. V_REF should be held at +3.0V with respect to GND. Any noise or jitter on V_REF will contribute to the noise floor of the chip and,therefore, V_REF should be as quiet and stable as possible.

There is one V_REF pin shared by all channels.

V_REF Sensitivity

The above equations that predict the DAC output assume that V_REF = 3.0V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio before being multiplied by the gain.

$$Level = Programmed\ Level\ *\ (1 - (V\_REF - 3.0))$$

Offset adjust has ample range to correct for deviations in V_REF in addition to any offset requirements. As long as V_REF is held stable after calibration, deviation in V_REF from 3.0V will not affect DC accuracy.

Voltage Range Options vs. Function

Different functional blocks require different DC level voltage ranges. The allowed combinations are listed in the table below.

TABLE 54. RANGE DECODE

GROUP	FUNCTIONAL BLOCK	VR0	VR1	VR2	VIR	RANGE SELECT
Drive	Driver (DVH, DVL, VTT)	√	√	√		Drive0(1)<1:0>
Comp	Comparator Thresholds (CVA, CVB)	√	√	√		Comp0(1)<1:0>
PPMU	PPMU Comparator Thresholds (CVA-PPMU, CVB-PPMU)	√	√	√	√	PPMU0(1)<1:0>
FV	Voltage Clamps (V-Cl-Hi, V-Cl-Lo) PPMU Voltage Force (V-FV)	√	√	√		FV0(1)<1:0>
FI	PPMU Current Force (V-FI, I-Cl-Hi, I-Cl-Lo)				√	N/A
	Tracks DUT_GND (FV, MV)					
	Does NOT Track DUT_GND (FI, MI)					

DC Calibration

The part is designed and tested to meet its DC accuracy specifications after a two-point, two-iteration calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. In general, most calibration points will be at 20% and 80% of the full scale value for that range. (The actual calibration points are listed separately for each functional block in the DC specification section.)

The test points are broken into two categories:

1. inner test
2. outer test

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

In general, the inner test will be performed against tighter, more accurate limits. But every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration technique.

Typical Calibration andTest Point Set-up

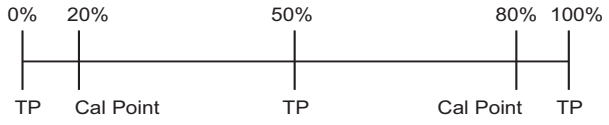


FIGURE 54.

System Level DC Accuracy Limits

Other calibration schemes and techniques, using more or fewer calibration points or different test points, may also be employed. The resulting system level accuracy may be superior or inferior to the part's specified limits and will depend on the details of the particular application.

Calibration Procedure

1. Calibrate the MONITOR
2. Calibrate the offset DAC
3. Calibrate the Gain DAC
4. Calibrate CMRR (Software Cal)
5. Calibrate MI (Software Cal)
6. Calibrate the DC Level

Level Calibration

INITIALIZE

- Select desired voltage range (VR0, VR1, VR2, VIR)
- Set Gain = 1.0; Offset = 0.0V

MEASURE

- Set Level 1 = Cal Point 1. Measure Output1' (low)
- Set Level 2 = Cal Point 2. Measure Output2' (high)

CALCULATE

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) - Gain' o (Level2 - Vmid)

FINISH

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

External References & Components

Several precision references control on-chip performance of various functions.

1. V_REF (Voltage)
2. R_EXT (Resistance)
3. PLL_CK (Frequency)

VOLTAGE

V_REF is used as a reference voltage for all DAC and DC level settings.

RESISTANCE

R_EXT has two functions:

- set the driver output impedance
- set the bias levels for the logic in the high speed data and enable paths

TRANSMISSION LINE INDUCTORS AND RESISTORS

Depending on the particular application and specific details of the PC board layout, a series inductor with a parallel resistor may or may not be placed at the DOUT pin to compensate for the capacitance on that node. The actual inductor and resistor value is application specific.

FREQUENCY

PLL_CK is used to establish the range and the resolution of the coarse delay and the coarse falling edge adjust sections.

COMPENSATION PINS

CPMU_CAP_IN and CPMU_CAP_OUT are used for an off-chip capacitor used to compensate the CPMU op amp. An external capacitor must be connected between these two pins.

The actual value of the external compensation pins may vary over application requirements. The smaller the value of the capacitor, the faster the CPMU will respond and settle. The larger the value, the more stable the CPMU will be.

PLL FILTER CAPACITOR

A capacitor at pin CAP_PLL is used to adjust the filter of the PLL. The other end of the capacitor should be connected to ground.

POWER SUPPLY RESTRICTIONS

The following guidelines must be met to support proper operation:

1. VCCH ≥ VCC
2. VCC ≥ VDD; VEE ≤ GND
3. VDD ≥ GND
4. VDD ≥ V_REF

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

Power Supply Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCCH
3. VCC
4. VDD
5. V_REF

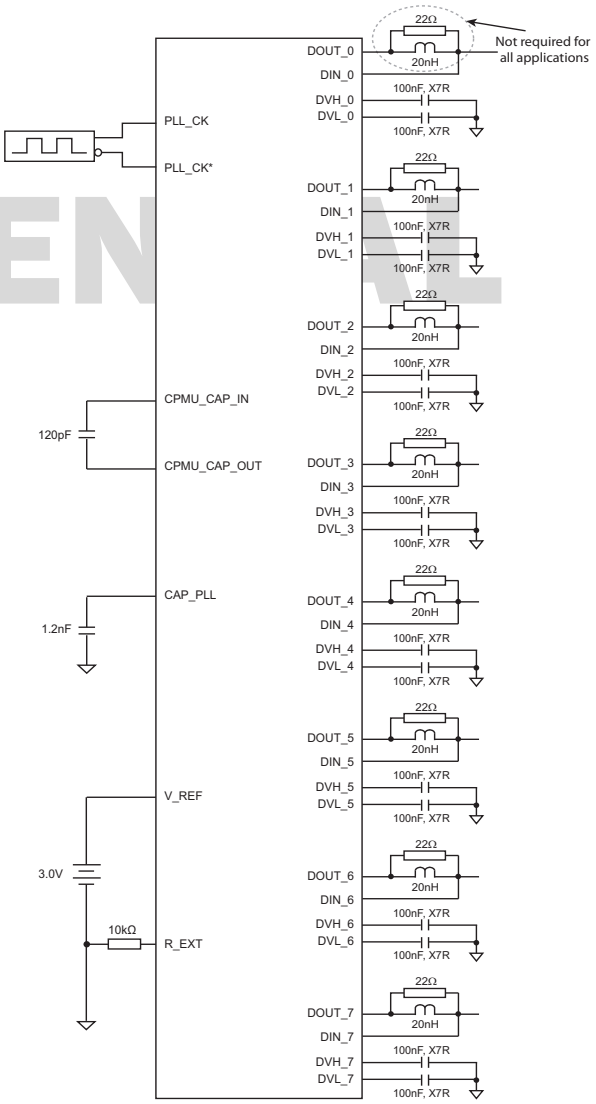


FIGURE 55.

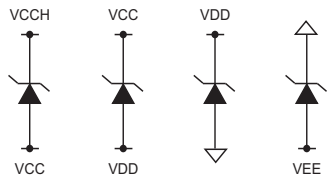


FIGURE 56.

CPU Port

All on-chip DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip (typically used for diagnostic purposes.)

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back. CK is the CPU port clock signal that transfers data back and forth. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction. STB remains high for the duration of the transaction, and must go low before another transaction may begin.

Clock Requirements

It is recommended that the CK be running at all times as it refreshes the DC levels throughout the chip. However, the CK may be stopped momentarily in order to make the chip quieter to support extremely accurate low noise measurements. The duration of these measurements should be short enough to minimize any droop on the levels.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached. Each group of registers with a common WE is shown in the memory map tables with a common background color.

The registers in the WE group will be written to if WE = 1. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.WE is read back as a don't care (X) value.

Read vs. Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type.

TABLE 55.

1st SDIO Bit	CPU Transaction Type
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

Parallel Write

The second SDIO bit of a transaction indicates whether a parallel write occurs. The parallel write is a convenient way to save time when identical information needs to go to multiple channels.

TABLE 56.

2nd SDIO Bit	CPU Transaction Type
0	Data goes to the selected channel
1	Data goes to all channels

A parallel write ignores the particular channel address, and writes the information into the same location on all channels. During a parallel write, all channels on the chip will write the data to the selected destinations in parallel, regardless of which channel's address is input into the chip.

Reset

RESET is an external hardware reset signal that places all internal registers and control lines into a low state. Reset must be executed after a power up sequence. RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power up sequence.

RESET is active high.

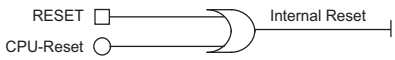


FIGURE 57.

In addition, the CPU port can execute a reset (as a write only transaction). If the Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one-shot pulse that performs the same function as an external RESET.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 57.

D15 ... D4	D3 ... D0
Product ID (032 Hex)	Die Revision

The product ID is hard-wired into the part and is unique to the part and will not change over time. The die revision may change over time if there are product updates.

Protocol Timing Diagram

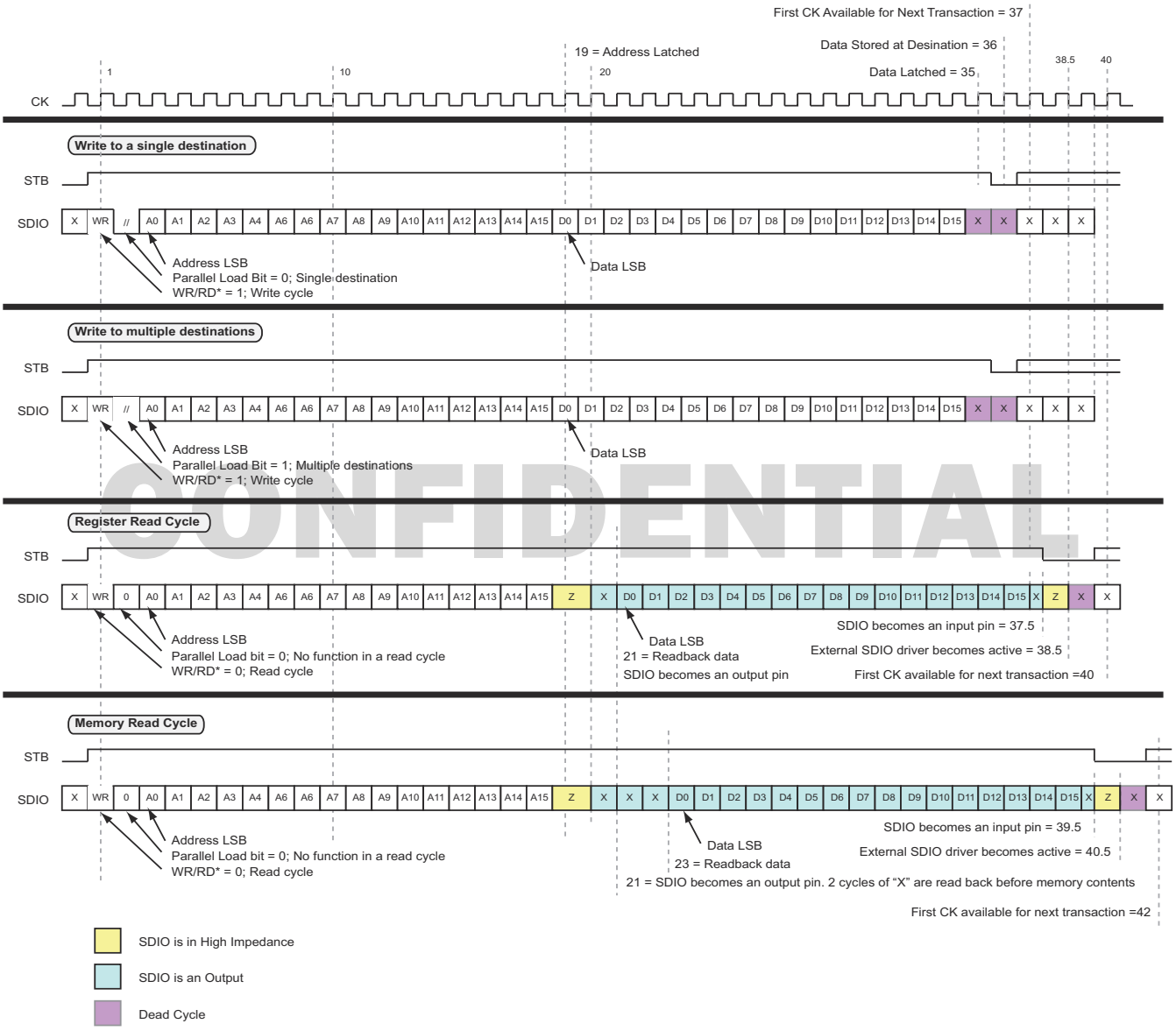


FIGURE 58.

Memory Space

Information is stored on-chip in two ways:

1. RAM
2. Registers

Each storage mechanism is then broken into two categories:

1. Per pin resources
2. Central resources

The address space is partitioned into several different segments to clearly mark the resource type and function.

TABLE 58.

Per Pin Resource RAM Storage																
Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	Channel 0 DC Levels
0	0	0	0	0	0	0	0	0	0	1	A4	A3	A2	A1	A0	Channel 0 DC Level Offset Values
0	0	0	0	0	0	0	0	0	1	0	A4	A3	A2	A1	A0	Channel 0 DC Level Gain Values
0	0	0	0	0	0	0	0	0	1	1	A4	A3	A2	A1	A0	Not Used
•	•				•				•	•			•			Channels 1 - 6
0	0	0	0	0	0	1	1	1	0	0	A4	A3	A2	A1	A0	Channel 7 DC Levels
0	0	0	0	0	0	1	1	1	0	1	A4	A3	A2	A1	A0	Channel 7 DC Level Offset Values
0	0	0	0	0	0	1	1	1	1	0	A4	A3	A2	A1	A0	Channel 7 DC Level Gain Values
0	0	0	0	0	0	1	1	1	1	1	A4	A3	A2	A1	A0	Not Used
Central Resource RAM Storage																
Register Bit	Central Bit	Unused Bits							DAC Function		Resource Address					Description
0	1	0	0	0	0	0	0	0	0	0	A4	A3	A2	A1	A0	Central Resource DC Levels
0	1	0	0	0	0	0	0	0	0	1	A4	A3	A2	A1	A0	Central Resource Offset Values
0	1	0	0	0	0	0	0	0	1	0	A4	A3	A2	A1	A0	Central Resource Gain Values
0	1	0	0	0	0	0	0	0	1	1	A4	A3	A2	A1	A0	Not Used
Per Pin Resource Register Storage																
Register Bit	Central Bit	Channel Address							Resource Address							Description
1	0	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 0 Registers
1	0	0	0	0	0	0	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 1 Registers
1	0	0	0	0	0	0	1	0	A6	A5	A4	A3	A2	A1	A0	Channel 2 Registers
1	0	0	0	0	0	0	1	1	A6	A5	A4	A3	A2	A1	A0	Channel 3 Registers
1	0	0	0	0	0	1	0	0	A6	A5	A4	A3	A2	A1	A0	Channel 4 Registers
1	0	0	0	0	0	1	0	1	A6	A5	A4	A3	A2	A1	A0	Channel 5 Registers
1	0	0	0	0	0	1	1	0	A6	A5	A4	A3	A2	A1	A0	Channel 6 Registers
1	0	0	0	0	0	1	1	1	A6	A5	A4	A3	A2	A1	A0	Channel 7 Registers
Central Resource Register Storage																
Register Bit	Central Bit	Unused Bits							Resource Address							Description
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Central Resource Registers

Address Space

PER PIN DC LEVELS

Channel 0 RAM Storage																
Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DVH-0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	DVL-0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	CVA-0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	CVB-0
0	0	0	0	0	0	0	0	0	0	0	4 - 31					Not Used
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	DVH-0 Offset
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	DVL-0 Offset
0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	CVA-0 Offset
0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	CVA-B Offset
0	0	0	0	0	0	0	0	0	0	1	4 - 31					Not Used
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	DVH-0 Gain
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	DVL-0 Gain
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	CVA-0 Gain
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	CVA-B Gain
0	0	0	0	0	0	0	0	0	1	0	4 - 31					Not Used
0	0	0	0	0	0	0	0	0	1	1	0 - 31					Not Used
⋮					⋮						⋮					⋮

Channel 7 RAM Storage																
Register Bit	Central Bit	Channel Address							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	DVH-7
0	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	DVL-7
0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	0	CVA-7
0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	CVB-7
0	0	0	0	0	0	1	1	1	0	0	4 - 31					Not Used
0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	DVH-7 Offset
0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	1	DVL-7 Offset
0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0	CVA-7 Offset
0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	1	CVB-7 Offset
0	0	0	0	0	0	1	1	1	0	1	4 - 31					Not Used
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	DVH-7 Gain
0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	DVL-7 Gain
0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0	CVA-7 Gain
0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	CVB-7 Gain
0	0	0	0	0	0	1	1	1	1	0	4 - 31					Not Used
0	1	0	0	0	0	1	1	1	1	1	0 - 31					Not Used

CENTRAL RESOURCE DC LEVELS

CPMU RAM Storage																
Register Bit	Central Bit	Unused							DAC Function		Resource Address					Description
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	V-FV
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	V-FI
0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	CVA-CPMU
0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	CVB-CPMU
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	V-CI-Hi
0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	V-CI-Lo
0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0	I-CI-Hi
0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	I-CI-Lo
0	1	0	0	0	0	0	0	0	0	0	8 - 11, 16 - 31					Not Used
0	1	0	0	0	0	0	0	0	0	0	12 - 15					DAC Configuration
0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	V-FV Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	1	V-FI Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0	CVA-CPMU Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	CVB-CPMU Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	V-CI-Hi Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	1	V-CI-Lo Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	I-CI-Hi Offset
0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	1	I-CI-Lo Offset
0	1	0	0	0	0	0	0	0	0	1	8 - 11, 16 - 31					Not Used
0	1	0	0	0	0	0	0	0	0	1	12 - 15					DAC Configuration
0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	V-FV Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	V-FI Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	0	CVA-CPMU Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	0	1	1	CVB-CPMU Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	V-CI-Hi Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	1	V-CI-Lo Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	1	1	0	I-CI-Hi Gain
0	1	0	0	0	0	0	0	0	1	0	0	0	1	1	1	I-CI-Lo Gain
0	1	0	0	0	0	0	0	0	1	0	8 - 11, 16 - 31					Not Used
0	1	0	0	0	0	0	0	0	1	0	12 - 15					DAC Configuration
0	1	0	0	0	0	0	0	0	1	1	0 - 31					Not Used

DAC configuration addresses should be programmed to Data = 7FFF Hex for proper DAC operation.
DAC configuration addresses are write only. They cannot be read back.

Per Pin Driver Registers

Channel 0 – 7 Control Registers (0 ≤ # ≤ 7)																				
Register Bit	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	#	0											WE	En-ZB#	En-ZA#	WE	Data-ZB#	Data-ZA#	Driver Terminations
1	0	#	1	WE	Fast-HiZ-En#	WE	Sel-En#-XOR	En#-XOR	D#-XOR	WE	Sel-RT-En#	CPU-En#	WE	Sel-RT-D#	CPU-D#	WE	0	WE	0	Driver Configuration
1	0	#	2							WE	RO-DVH#3	RO-DVH#2	RO-DVH#1	RO-DVH#0	WE	RO-DVL#3	RO-DVL#2	RO-DVL#1	RO-DVL#0	Driver Output Impedance
1	0	#	3	En#	Data#					WE	Con-CPMU-S-D#	WE	Sel-RT-Con-D#	Con-CPMU-F-D#	WE	Con-Ext-S-D#	WE	Sel-RT-Ext-F-D#	Con-Ext-F-D#	DOUT Switch Connections
1	0	#	4		WE	Sel-D#-CFEA	WE	D#-CFEA3	D#-CFEA2	D#-CFEA1	D#-CFEA0	WE	Sel-D#-CD	WE	D#-CD4	D#-CD3	D#-CD2	D#-CD1	D#-CD0	Data Deskew
1	0	#	5		WE	Sel-en#-CFEA	WE	En#-CFEA3	En#-CFEA2	En#-CFEA1	En#-CFEA0	WE	Sel-En#-CD	WE	En#-CD4	En#-CD3	En#-CD2	En#-CD1	En#-CD0	Enable Deskew
1	0	#	6														WE	Drive#-RS1	Drive#-RS0	Driver Voltage Range
1	0	#	7– 63																	Not Used

Read Only

Per Pin Comparator Registers

Channel 0 – 7 Control Registers (0 ≤ # ≤ 7)																				
Register Bit	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	0	#	64 40H						WE	CPU-CB#	CPU-CA#	WE	Sel-CPMU-C#	0	0	0	WE	Sel-MU-CB#	Sel-MU-CA#	Comparator Configuration
1	0	#	65 41H					WE	Con-DIN-C#	WE	Con-DOUT-C#	WE	Con-CPMU-S-C#	WE	Con-CPMU-F-C#	WE	Con-Ext-S-C#	WE	Con-Ext-F-C#	DIN Switch Control
1	0	#	66 41H		WE	Sel-CA#-CFEA	WE	CA#-CFEA3	CA#-CFEA2	CA#-CFEA1	CA#-CFEA0	WE	Sel-CA#-CD	WE	CA#-CD4	CA#-CD3	CA#-CD2	CA#-CD1	CA#-CD0	Comp A Deskew
1	0	#	67 43H		WE	Sel-CB#-CFEA	WE	CB#-CFEA3	CB#-CFEA2	CB#-CFEA1	CB#-CFEA0	WE	Sel-CB#-CD	WE	CB #-CD4	CB #-CD3	CB #-CD2	CB #-CD1	CB #-CD0	Comp B Deskew
1	0	#	68 44H														WE	Comp#-RS1	Comp#-RS0	Comparator Threshold Range
1	0	#	69 45H								WE	CPU-Pulse#	WE	RO-D#-En	RO-En#-En	Edge-Par#	RO-Trig-En#	Sel-RO-C#	Ring-En#	Ring Oscillator
1	0	#	70 46H	RT-CB#	RT-CA#	CPMU-CB	CPMU-CA									WE	Ch#Diag2	Ch#Diag1	Ch#Diag0	Diagnostics
1	0	#	71- 128																	Not Used

Write Only

Read Only

Central Resource Registers

Central Resource Control Registers																				
Register Bit	Central Bit	Channel Address	Resource Address	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Description
1	1	0	0	WE	I-Ci-En	WE	CPMU-En	WE	V-Ci-En	WE	0	WE	Local-Sense*	WE	Loop	WE	MI/MV*	WE	FI/FV*	CPMU Configuraiton
1	1	0	1					WE	Mon-OE	WE	Sel-Ext-DAC	WE	Con-ES-CS	WE	Con-ES-CF	WE	Con-EF-CS	WE	Con-EF-CF	External Force/Sense
1	1	0	2		WE	FV-RS1	FV-RS0	WE	CPMU-RS1	CPMU-RS0	WE	IR7	IR6	IR5	IR4	IR3	IR2	IR1	IR0	Current Range Threshold Range
1	1	0	3									WE	Sel-MU-Diag	WE	Diag4	Diag3	Diag2	Diag1	Diag0	Diagnostics
1	1	0	4								WE	F Clamp1	F Clamp0	WE	V-Swing1	V-Swing0	WE	PLL-ZB	PLL-ZA	PLL
1	1	0	5																	Not Used
1	1	0	6	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPU Reset
1	1	0	7 - 126																	Not Used
1	1	0	127	Product-ID11	Product-ID10	Product-ID9	Product-ID8	Product-ID7	Product-ID6	Product-ID5	Product-ID4	Product-ID3	Product-ID2	Product-ID1	Product-ID0	Die-Rev3	Die-Rev2	Die-Rev1	Die-Rev0	Die ID

Write Only

Read Only

Package Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows the equation:

$$Tj = Pd \cdot \theta JA + Ta$$

Tj = Junction Temperature

Pd = Power Dissipation

θJA = Thermal Resistance (Junction to Ambient)

Ta = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ JC) plus the resistance from the case to ambient (θCA)

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θJA. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta JA = \theta JC + \theta CA$$

θCA is determined by the system environment of the part and is therefore application specific. θJC is determined by the construction of the part.

θJC Calculation

θJC = θ(silicon)

+ θ(die attach)

+ θ(paddle)

θJC = .072 °C / W + .61 °C/W + .006 °C/W

θJC = .688 °C/W

The calculation is based upon ideal assumptions and it should be treated as a best-case value.

The thermal resistance of any material is defined by the equation:

θ = (Intrinsic material resistivity) • Thickness / Area

or

θ = Thickness / (Intrinsic material conductivity • Area).

Intrinsic Thermal Conductivity

Die Attach Thermal Conductivity = 1.4 W / M °K

Silicon Thermal Conductivity = 141.2 W / M °K

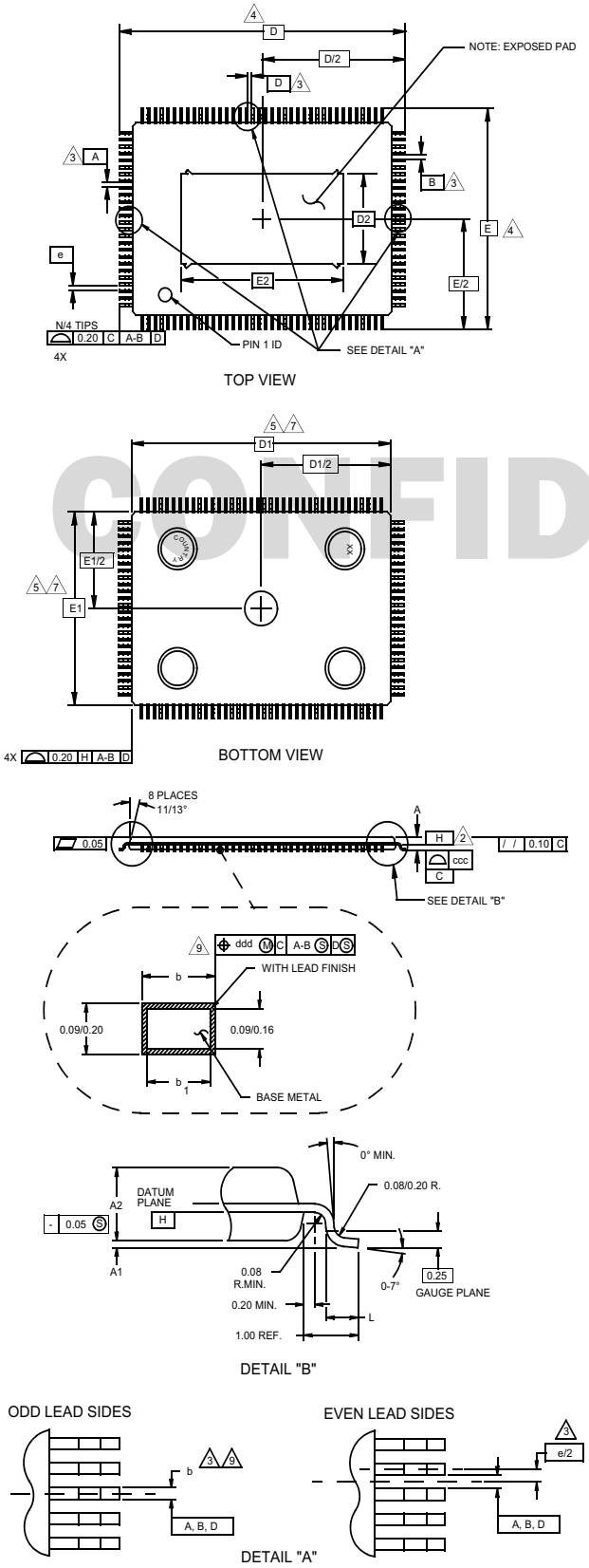
Paddle Thermal Conductivity = 263 W / M °K

Plastic Thermal Conductivity = 0.88 W / M °K

(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θJC through the paddle. The assumption is that all heat flow will go through the paddle and none through the surrounding plastic.)

Package Outline Drawing

Thin Plastic Quad Flatpack Package with Top Exposed Pad (TEP-LQFP)



Q128.14x20B

128 Lead Thin Quad Flatpack with Top Exposed Pad

SYMBOL	MILLIMETERS BHB MIN	NOM	MAX	NOTES
A	-	-	1.60	
A1	0.05	-	0.15	13
A2	1.35	1.40	1.45	
D	22 BSC			4
D1	20 BSC			7, 8
D2	12.20 BSC			14
E	16 BSC			4
E1	14 BSC			7, 8
E2	8.35 BSC			14
L	0.45	0.60	0.75	
N	128			
e	0.50 BSC			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

Rev. 0 3/09

NOTES:

1. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at center lines between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.254mm per side on D1 and E1 dimensions.
6. “N” is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. Package top dimensions are smaller than package bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located at the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 Registration MS-026, variations BHA & BHB.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimensions D2 and E2 represent the size of the exposed pad. The actual dimensions may be reduced up to 0.76mm due to mold flash.

Revision History

DATE	CHANGE
August 28, 2022	• Change Absolute Maximum of Digital Input Pins to VDD + 0.2 • Change Low Voltage Clamp Error VR0 to Spec # 14400 • Change Low Voltage Clamp Error VR2 to Spec # 14420 • Change High Voltage Clamp Error VR1 to Spec # 14550 • Change High Voltage Clamp Error VR2 to Spec # 14560
January 8, 2016	• Page 59: Power Supply Sequence Section - change power supply sequence
April 1, 2015	Change from Intersil to Elevate format.
July 31, 2013	Page 11: Spec 18110 - Change Test Conditions from PLL–ZA = 1; PLL–ZB = 0; PLL–ZA = 0; PLL–ZB =1 to (PLL–ZA = 1; PLL–ZB = 0) or (PLL–ZA = 0; PLL–ZB =1)
March 29, 2013	• Page 57 - Add “Transmission Line Inductors and Resistors Section • Page 57 - Figure 56 updated
February 7, 2013	• Page 8, Pin Descriptions: - Pins 2, 12, 22, 32: Change VOL_01 to VOH_01

Ordering Information

PART NUMBER (NOTE 1)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)
ISL55169CNEZ	ISL55161CNEZ	+25 to +100	128 Lead, 14x20mm MQFP w/top exposed heat slug
ISL55169-SYS	Evaluation Board		

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.