SOC Octal 500MHz Integrated Pin Electronics/DAC/PPMU/Deskew

Mystery is a highly integrated System-on-a-Chip (SoC) pin electronics solution that incorporates every analog function, along with digital support circuitry required to create 8 independent pin channels for Automated Test Equipment. Each channel is configured via a 100MHz SPI interface, and all real time data is programmed and read back through high-speed FLEX I/O pins that can be configured to interface directly to other devices using multiple single-ended and differential logic families.

Features

Pin Electronics Driver/Comparator

- Dual Mode 3-level Driver with Hi-Z Capability (DVH, DVL, VTT)
- HV (High Voltage) Driver Mode
- 25mV to 8V Swing Across –2V to +6V Range
- Programmable Driver Slew Rate
- HS (High Speed) Driver Mode
- 25mV to 4V Swing Across 0V to +4V Range
- Up to 8V Comparator Input Range
- 1GHz Comparator Equivalent Bandwidth
- Extremely Low Hi-Z Leakage over Entire I/O Range
- Short Circuit Protection

Per Pin PMU (PPMU)

- FV, FI, MV, MI
- 4 Quadrant Operation
- –2V to +6V FV/MV Range
- 5 Current Ranges (±2µA, ±20µA, ±200µA, ±2mA, ±50mA)
- Programmable Voltage and Current Clamps
- Resistive Load Function (12 Selectable Resistor Values)

Per Pin Active Load

- 2 Active Load Ranges (±24mA, ±1mA)
- Independently Programmable Current Source, Current Sink, and Commutating Voltage levels

Per Pin Timing Deskew

- Propagation Delay Adjustment
- 10ns Delay Adjustment Range
- 18ps Delay Adjustment Resolution

On-Chip DC Levels

- 17 Dedicated DAC levels per Channel
- 9 Dedicated DACs per Channel
- Per Level Offset Correction
- 16-bit Resolution/14-bit Accuracy
- DUT Ground Sensing and Correction (1 Per Chip)

100MHz SPI Interface

High Speed FLEX I/O

Analog Measure Bus

Extremely Small PCB Footprint: 2 package options

- 14mm x 14mm, 144 Ball fcBGA (1.0mm Pitch)
- 14mm x 14mm, 144 Ball fcCSP (1.0mm Pitch)

Pmax < 800mW per Channel

Applications

Automated Test Equipment (ATE)

Instrumentation and Characterization Equipment

ASIC Verifiers

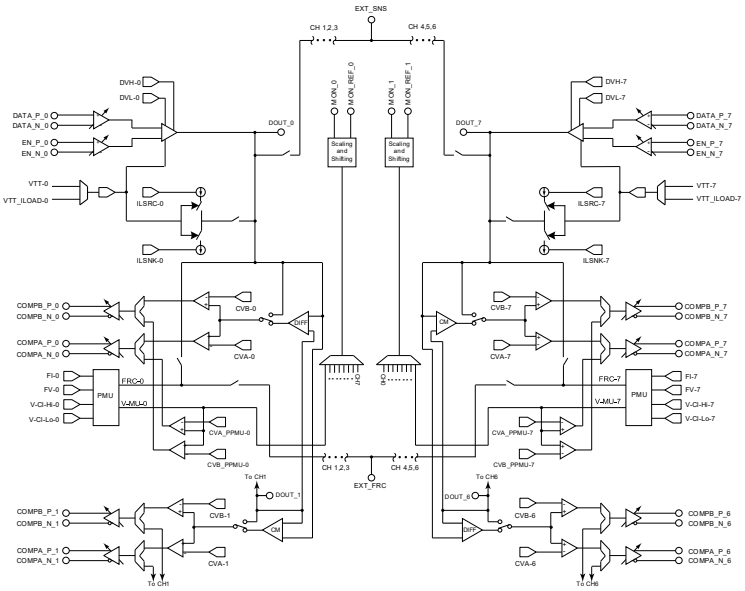

FIGURE 1: BLOCK DIAGRAM

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Pin Descriptions

TABLE 1: PIN DESCRIPTIONS

PIN #	PIN NAME	DESCRIPTION
Power Supplies		
E9	VHH	Positive analog power highest rail supply for gate drive bias.
B10, F10, H8, K10	VCC	Positive analog power supply for HV driver, PMU, and comparators, use clean supply.
B11, D11, F11, H11, K11, M11	VCCO	Positive HS driver output power supply, use clean supply.
D10, E8, H10, J9	VEE	Negative analog power supply for HV driver, PMU, comparator, use clean supply.
B12, D12, F12, H12, K12, M12	VEEO	Negative HS driver output power supply, use clean supply.
A11, B3, C10, C11, D3, E10, E11, F3, F6, F8, F9, G3, G6, G7, G8, G9, G10, G11, J3, J8, J10, J11, K9, L3, L10, L11	GND	Analog ground.
A3, M3	VDD	Digital power supply.
C3, E3, E6, H3, H6, K3	VDDA	Low voltage analog supply, should be clean.
Analog Pins		
F7	GND_REF	Accurate ground analog ground reference (sense only) for VREF.
E7	VREF	Precision external analog voltage reference connection.
H7	RREF	Precision external reference resistor connection (connect external resistor between RREF and GND).
A10, A12, C12, E12, G12, J12, L12, M10	DOUT_7, DOUT_6, DOUT_5, DOUT_4, DOUT_3, DOUT_2, DOUT_1, DOUT_0	Analog I/O that connects to device under test.
C8	EXT_SNS_HI	Unbuffered “measure high” DC calibration bus connection.
B8	EXT_SNS_LO	Unbuffered “measure low” DC calibration bus connection.
D8	EXT_FRC	External Force DC calibration bus connection.
L9, M9	MON_1, MON_0	Analog measurement output from PPMU.
L8, M8	MON_REF_1, MON_REF_0	Reference for analog measurement output from PPMU.
A8	DGS	DUT Ground Sense. Connect to Device Under Test Ground.
Digital Inputs		
M7, L7	DATA_P_0, DATA_N_0	Channel 0 driver data differential inputs.
M1, M2	DATA_P_1, DATA_N_1	Channel 1 driver data differential inputs.
K1, K2	DATA_P_2, DATA_N_2	Channel 2 driver data differential inputs.
H1, H2	DATA_P_3, DATA_N_3	Channel 3 driver data differential inputs.
E1, E2	DATA_P_4, DATA_N_4	Channel 4 driver data differential inputs.
C1, C2	DATA_P_5, DATA_N_5	Channel 5 driver data differential inputs.
A1, A2	DATA_P_6, DATA_N_6	Channel 6 driver data differential inputs.
A7, B7	DATA_P_7, DATA_N_7	Channel 7 driver data differential inputs.
M6, L6	ENA_P_0, ENA_N_0	Channel 0 driver enable differential inputs.
L1, L2	ENA_P_1, ENA_N_1	Channel 1 driver enable differential inputs.
J1, J2	ENA_P_2, ENA_N_2	Channel 2 driver enable differential inputs.
G1, G2	ENA_P_3, ENA_N_3	Channel 3 driver enable differential inputs.
F1, F2	ENA_P_4, ENA_N_4	Channel 4 driver enable differential inputs.
D1, D2	ENA_P_5, ENA_N_5	Channel 5 driver enable differential inputs.
B1, B2	ENA_P_6, ENA_N_6	Channel 6 driver enable differential inputs.

PIN #	PIN NAME	DESCRIPTION
A6, B6	ENA_P_7, ENA_N_7	Channel 7 driver enable differential inputs.
Digital Outputs		
K7, K6	COMPA_P_0, COMPA_N_0	Channel 0 comparator “A” differential outputs.
M4, L4	COMPA_P_1, COMPA_N_1	Channel 1 comparator “A” differential outputs.
K4, J4	COMPA_P_2, COMPA_N_2	Channel 2 comparator “A” differential outputs.
H4, G4	COMPA_P_3, COMPA_N_3	Channel 3 comparator “A” differential outputs.
E4, F4	COMPA_P_4, COMPA_N_4	Channel 4 comparator “A” differential outputs.
C4, D4	COMPA_P_5, COMPA_N_5	Channel 5 comparator “A” differential outputs.
A4, B4	COMPA_P_6, COMPA_N_6	Channel 6 comparator “A” differential outputs.
C7, C6	COMPA_P_7, COMPA_N_7	Channel 7 comparator “A” differential outputs.
J7, J6	COMPB_P_0, COMPB_N_0	Channel 0 comparator “B” differential outputs.
M5, L5	COMPB_P_1, COMPB_N_1	Channel 1 comparator “B” differential outputs.
K5, J5	COMPB_P_2, COMPB_N_2	Channel 2 comparator “B” differential outputs.
H5, G5	COMPB_P_3, COMPB_N_3	Channel 3 comparator “B” differential outputs.
E5, F5	COMPB_P_4, COMPB_N_4	Channel 4 comparator “B” differential outputs.
C5, D5	COMPB_P_5, COMPB_N_5	Channel 5 comparator “B” differential outputs.
A5, B5	COMPB_P_6, COMPB_N_6	Channel 6 comparator “B” differential outputs.
D7, D6	COMPB_P_7, COMPB_N_7	Channel 7 comparator “B” differential outputs.
SPI Interface		
C9	SPI_CLK	SPI serial bus clock input (selectable termination).
A9	SPI_SDI	SPI serial data input (selectable termination).
B9	SPI_SDO	SPI serial data output (50Ω output).
D9	SPI_CS	SPI chip selects input (selectable termination).
K8	RESET	Chip reset, active high (on chip 50kΩ pull up to VDD).
H9	ALARM	Alarm output pin. Open drain output that pulls high when an alarm has been triggered (connect a 10kΩ resistor between this ALARM and VDD). Active high.

Pin Configuration

14mm x 14mm
144 Ball fcBGA
(Top View, Balls Down)

	1	2	3	4	5	6	7	8	9	10	11	12
A	A1 DATA_P_6	A2 DATA_N_6	A3 VDD	A4 COMPA_P_6	A5 COMPB_P_6	A6 ENA_P_7	A7 DATA_P_7	A8 DGS	A9 SPI_SDI	A10 DOUT_7	A11 GND	A12 DOUT_6
B	B1 ENA_P_6	B2 ENA_N_6	B3 GND	B4 COMPA_N_6	B5 COMPB_N_6	B6 ENA_N_7	B7 DATA_N_7	B8 EXT_SNS_LO	B9 SPI_SDO	B10 VCC	B11 VCCO	B12 VEEO
C	C1 DATA_P_5	C2 DATA_N_5	C3 VDDA	C4 COMPA_P_5	C5 COMPB_P_5	C6 COMPA_N_7	C7 COMPA_P_7	C8 EXT_SNS_HI	C9 SPI_CLK	C10 GND	C11 GND	C12 DOUT_5
D	D1 ENA_P_5	D2 ENA_N_5	D3 GND	D4 COMPA_N_5	D5 COMPB_N_5	D6 COMPB_N_7	D7 COMPB_P_7	D8 EXT_FRC	D9 SPI_CS	D10 VEE	D11 VCCO	D12 VEEO
E	E1 DATA_P_4	E2 DATA_N_4	E3 VDDA	E4 COMPA_P_4	E5 COMPB_P_4	E6 VDDA	E7 VREF	E8 VEE	E9 VHH	E10 GND	E11 GND	E12 DOUT_4
F	F1 ENA_P_4	F2 ENA_N_4	F3 GND	F4 COMPA_N_4	F5 COMPB_N_4	F6 GND	F7 GND_REF	F8 GND	F9 GND	F10 VCC	F11 VCCO	F12 VEEO
G	G1 ENA_P_3	G2 ENA_N_3	G3 GND	G4 COMPA_N_3	G5 COMPB_N_3	G6 GND	G7 GND	G8 GND	G9 GND	G10 GND	G11 GND	G12 DOUT_3
H	H1 DATA_P_3	H2 DATA_N_3	H3 VDDA	H4 COMPA_P_3	H5 COMPB_P_3	H6 VDDA	H7 RREF	H8 VCC	H9 ALARM	H10 VEE	H11 VCCO	H12 VEEO
J	J1 ENA_P_2	J2 ENA_N_2	J3 GND	J4 COMPA_N_2	J5 COMPB_N_2	J6 COMPB_N_0	J7 COMPB_P_0	J8 GND	J9 VEE	J10 GND	J11 GND	J12 DOUT_2
K	K1 DATA_P_2	K2 DATA_N_2	K3 VDDA	K4 COMPA_P_2	K5 COMPB_P_2	K6 COMPA_N_0	K7 COMPA_P_0	K8 RESET	K9 GND	K10 VCC	K11 VCCO	K12 VEEO
L	L1 ENA_P_1	L2 ENA_N_1	L3 GND	L4 COMPA_N_1	L5 COMPB_N_1	L6 ENA_N_0	L7 DATA_N_0	L8 MON_REF_1	L9 MON_1	L10 GND	L11 GND	L12 DOUT_1
M	M1 DATA_P_1	M2 DATA_N_1	M3 VDD	M4 COMPA_P_1	M5 COMPB_P_1	M6 ENA_P_0	M7 DATA_P_0	M8 MON_REF_0	M9 MON_0	M10 DOUT_0	M11 VCCO	M12 VEEO

FIGURE 2: PIN CONFIGURATION - 144 BALL FCBGA (1.0MM PITCH)

14mm x 14mm
144 Ball fcCSP
(Top View, Balls Down)

	1	2	3	4	5	6	7	8	9	10	11	12
A	A1 DATA_P_6	A2 DATA_N_6	A3 VDD	A4 COMPA_P_6	A5 COMPB_P_6	A6 ENA_P_7	A7 DATA_P_7	A8 DGS	A9 SPI_SDI	A10 DOUT_7	A11 GND	A12 DOUT_6
B	B1 ENA_P_6	B2 ENA_N_6	B3 GND	B4 COMPA_N_6	B5 COMPB_N_6	B6 ENA_N_7	B7 DATA_N_7	B8 EXT_SNS_LO	B9 SPI_SDO	B10 VCC	B11 VCCO	B12 VEEO
C	C1 DATA_P_5	C2 DATA_N_5	C3 VDDA	C4 COMPA_P_5	C5 COMPB_P_5	C6 COMPA_N_7	C7 COMPA_P_7	C8 EXT_SNS_HI	C9 SPI_CLK	C10 GND	C11 GND	C12 DOUT_5
D	D1 ENA_P_5	D2 ENA_N_5	D3 GND	D4 COMPA_N_5	D5 COMPB_N_5	D6 COMPB_N_7	D7 COMPB_P_7	D8 EXT_FRC	D9 SPI_CS	D10 VEE	D11 VCCO	D12 VEEO
E	E1 DATA_P_4	E2 DATA_N_4	E3 VDDA	E4 COMPA_P_4	E5 COMPB_P_4	E6 VDDA	E7 VREF	E8 VEE	E9 VHH	E10 GND	E11 GND	E12 DOUT_4
F	F1 ENA_P_4	F2 ENA_N_4	F3 GND	F4 COMPA_N_4	F5 COMPB_N_4	F6 GND	F7 GND_REF	F8 GND	F9 GND	F10 VCC	F11 VCCO	F12 VEEO
G	G1 ENA_P_3	G2 ENA_N_3	G3 GND	G4 COMPA_N_3	G5 COMPB_N_3	G6 GND	G7 GND	G8 GND	G9 GND	G10 GND	G11 GND	G12 DOUT_3
H	H1 DATA_P_3	H2 DATA_N_3	H3 VDDA	H4 COMPA_P_3	H5 COMPB_P_3	H6 VDDA	H7 RREF	H8 VCC	H9 ALARM	H10 VEE	H11 VCCO	H12 VEEO
J	J1 ENA_P_2	J2 ENA_N_2	J3 GND	J4 COMPA_N_2	J5 COMPB_N_2	J6 COMPB_N_0	J7 COMPB_P_0	J8 GND	J9 VEE	J10 GND	J11 GND	J12 DOUT_2
K	K1 DATA_P_2	K2 DATA_N_2	K3 VDDA	K4 COMPA_P_2	K5 COMPB_P_2	K6 COMPA_N_0	K7 COMPA_P_0	K8 RESET	K9 GND	K10 VCC	K11 VCCO	K12 VEEO
L	L1 ENA_P_1	L2 ENA_N_1	L3 GND	L4 COMPA_N_1	L5 COMPB_N_1	L6 ENA_N_0	L7 DATA_N_0	L8 MON_REF_1	L9 MON_1	L10 GND	L11 GND	L12 DOUT_1
M	M1 DATA_P_1	M2 DATA_N_1	M3 VDD	M4 COMPA_P_1	M5 COMPB_P_1	M6 ENA_P_0	M7 DATA_P_0	M8 MON_REF_0	M9 MON_0	M10 DOUT_0	M11 VCCO	M12 VEEO

FIGURE 3: PIN CONFIGURATION - 144 BALL FCCSP (1.0MM PITCH)

Absolute Maximum Ratings

TABLE 2: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supplies					
Positive Analog Supply Voltage	V_{CC_ABS}	–0.5		8	V
Positive Analog Supply Voltage	V_{HH_ABS}	–0.5		16.5	V
Positive Driver Supply Voltage	V_{CCO_ABS}	–0.5		6	V
Digital Supply Voltage/Analog Supply Voltage	V_{DD}/V_{DDA_ABS}	–0.5		1.98	V
Negative Analog Supply Voltage	V_{EE_ABS}	–4.0		0.5	V
Negative Driver Supply Voltage	V_{EEO_ABS}	–2.0		0.5	V
Total Analog Supply [VCC-VEE]	$V_{DIF\_CE\_ABS}$	–0.5		11.5	V
Total Analog Supply [VHH-VEE]	$V_{DIF\_HE\_ABS}$	–0.5		20	V
Total Driver Supply Voltage [VCCO-VEEO]	$V_{DIF\_OUT\_ABS}$	–0.5		7.5	V
Driver Output Levels (High Voltage Mode)					
Driver Swing (|VDVH – VDVL|)	$V_{SWING\_HV\_ABS}$			8.2	V
DVH – Driver “High” Level Voltage Output Range	$V_{RNG\_HVH\_ABS}$	–2.1		6.1	V
DVL – Driver “Low” Level Voltage Output Range	$V_{RNG\_HVL\_ABS}$	–2.1		6.1	V
VTT – Driver “Termination” Level Voltage Output Range	$V_{RNG\_HVT\_ABS}$	–2.1		6.1	V
Driver Output Levels (High Speed Mode)					
Driver Swing (|VDVH – VDVL|)	$V_{SWING\_HS\_ABS}$			4.2	V
DVH – Driver “High” Level Voltage Output Range	$V_{RNG\_HSH\_ABS}$	–0.1		4.1	V
DVL – Driver “Low” Level Voltage Output Range	$V_{RNG\_HSL\_ABS}$	–0.1		4.1	V
VTT – Driver “Termination” Level Voltage Output Range	$V_{RNG\_HST\_ABS}$	–0.1		4.1	V
Differential Input Levels (for Differential Voltage Comparator Measurements)					
DOUTodd-DOUTeven (Absolute Value)	$V_{RNG\_DIFF\_EO}$	0		6.1	V
High Speed Comparator Threshold Levels					
CVA – Compare Voltage Threshold “A” Range	$V_{RNG\_CMPCVA\_ABS}$	–2.1		6.1	V
CVB – Compare Voltage Threshold “B” Range	$V_{RNG\_CMPCVB\_ABS}$	–2.1		6.1	V
Active Load					
VCOM_ILOAD Commutating Voltage Range	$V_{RNG\_VCOM\_ABS}$	–2.1		6.1	V
ISRC – Programmable Current Source Range	$I_{RNG\_ISRC\_ABS}$	0		25	mA
ISINK – Programmable Current Sink Range	$I_{RNG\_ISNK\_ABS}$	–25		0	mA
PPMU					
Force Voltage Output/Measure Voltage Input Range/Voltage Clamp Range	$V_{RNG\_FRC\_ABS}$	VEE		VCC	V
Force Current/Measure Current Range					
IR0 – Range 0	$I_{RNG\_FORCE0\_ABS}$	–3		3	µA
IR1 – Range 1	$I_{RNG\_FORCE1\_ABS}$	–30		30	µA
IR2 – Range 2	$I_{RNG\_FORCE2\_ABS}$	–300		300	µA
IR3 – Range 3	$I_{RNG\_FORCE3\_ABS}$	–3		3	mA
IR4 – Range 4	$I_{RNG\_FORCE4\_ABS}$	–55		55	mA
Force Current/Measure Current Compliance Range	$V_{RNG\_CMPL\_ABS}$	See Figure 42			V
CVA_PPMU – Go-no-Go Comparator Threshold “A”	$V_{RNG\_PMUCVA\_ABS}$	–2.1		6.1	V
CVB_PPMU – Go-no-Go Comparator Threshold “B”	$V_{RNG\_PMUCVB\_ABS}$	–2.1		6.1	V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
External References					
Reference Voltage (VREF)	$V_{RNG\_REF\_ABS}$	–0.5		1.8	V
GND_REF Voltage Range (relative to GND)	$V_{RNG\_GNDREF\_ABS}$	–0.5		0.5	V
RREF – External Reference Resistor Value	$R_{RNG\_RREF\_ABS}$	–1%		+1%	k□
DGS Voltage Range (Relative to GND)	$V_{RNG\_DGS\_ABS}$	–500		500	mV
EXT_FRC – External Force Voltage Range	$V_{RNG\_EXTFRC\_ABS}$	VEE – 0.5		VCC + 0.5	V
EXT_SNS – External Sense Voltage Range	$V_{RNG\_SNSLO\_ABS}$ $V_{RNG\_SNSHI\_ABS}$	VEE – 0.5		VCC + 0.5	V
Miscellaneous					
Maximum Junction Temperature Range	T_{JUNC_ABS}	0		125	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by the warranty.

Recommended Operating Conditions

TABLE 3: RECOMMENDED OPERATION CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Power Supplies					
Positive Analog Circuit Supply Voltage	V_{CC}	7.27	7.5	7.72	V
Positive Analog High (Bias) Supply Voltage	V_{HH}	15.05	15.5	15.95	V
Positive Driver Supply Voltage	V_{CCO}	5.34	5.5	5.66	V
Digital Supply Voltage/Analog Supply Voltage	V_{DD}/V_{DDA}	1.75	1.8	1.85	V
Negative Analog Supply Voltage	V_{EE}	–3.6	–3.5	–3.4	V
Negative Driver Supply Voltage	V_{EEO}	–1.55	–1.5	–1.46	V
Total Analog Supply |VCC – VEE|	V_{DIF_CE}	10.67	11	11.33	V
Total Analog Supply [VHH – VEE]	V_{DIF_HE}	17.95	19.0	19.5	V
Total Driver Supply [VCCO – VEEO]	V_{DIF_OUT}	6.79	7	7.21	V
Driver Output Levels (High Voltage Mode)					
Driver Swing (|DVH – DVL|)	V_{SWING_HV}	0.025		8	V
DVH – Driver "High" Level Voltage Output Range	V_{RNG_HVH}	–2		6	V
DVL – Driver "Low" Level Voltage Output Range	V_{RNG_HVL}	–2		6	V
VTT – Driver "Termination" Level Voltage Output Range	V_{RNG_HVT}	–2		6	V
Driver Output Levels (High Speed Mode)					
Driver Swing	V_{SWING_HS}	0.025		4	V
DVH – Driver "High" Level Voltage Output Range	V_{RNG_HSH}	0		4	V
DVL – Driver "Low" Level Voltage Output Range	V_{RNG_HSL}	0		4	V
VTT – Driver "Termination" Level Voltage Output Range	V_{RNG_HST}	0		4	V
Differential Input Levels (for Differential Voltage comparator measurements)					
DOUTodd-DOUTeven (Absolute Value)	$V_{RNG\_DIFF\_EO}$	0		6	V
High Speed Comparator Threshold Levels					
CVA – Compare Voltage Threshold "A"	V_{RNG_CMPCVA}	–2		6	V
CVB – Compare Voltage Threshold "B"	V_{RNG_CMPCVB}	–2		6	V
Active Load					
VCOM_ILOAD – Commutating Voltage Range	V_{RNG_VCOM}	–2		6	V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
ISRC – Programmable Current Source Range	I_{RNG_ISRC}	0		24	mA
ISINK – Programmable Current Sink Range	I_{RNG_ISNK}	–24		0	mA
PPMU					
Force Voltage Output/Measure Voltage Input Range/Voltage Clamp Range	V_{RNG_FRC}	–2		6	V
Force Current/Measure Current Range IR0 – Range 0 IR1 – Range 1 IR2 – Range 2 IR3 – Range 3 IR4 – Range 4	 I_{RNG_FORCE0} I_{RNG_FORCE1} I_{RNG_FORCE2} I_{RNG_FORCE3} I_{RNG_FORCE4}	 –2 –20 –200 –2 –50		 2 20 200 2 50	 µA µA µA mA mA
Force Current/Measure Current Compliance Range	V_{RNG_CMPL}	See Figure 42			V
CVA_PPMU – Go-no-Go Comparator Threshold "A"	V_{RNG_PMUCVA}	–2		6	V
CVB_PPMU – Go-no-Go Comparator Threshold "B"	V_{RNG_PMUCVB}	–2		6	V
External References					
Reference Voltage (VREF)	V_{RNG_REF}	1.2375	1.25	1.2625	V
GND_REF – Voltage Range (relative to GND)	V_{RNG_GNDREF}	–50		50	mV
RREF – External Reference Resistor Value	R_{RNG_RREF}	12.276	12.4	12.524	kΩ
DGS Voltage Range (Relative to GND)	V_{RNG_DGS}	–300		300	mV
EXT_FRC – External Force Voltage Range	V_{RNG_EXTFRC}	VEE		VCC	V
EXT_SNS_LO, EXT_SNS_HI - External Sense Voltage Range	V_{RNG_SNSLO} V_{RNG_SNSHI}	VEE		VCC	V
MON_0, MON_1 – Voltage Range	V_{RNG_MH}			6.1	V
MON_REF_0, MON_REF_1 – Voltage Range	V_{RNG_ML}	-2.1			V
MON_0, MON_1, MON_REF_0, MON_REF_1 – Output load	I_{RNG_MHL}	-5		5	µA
Miscellaneous					
Junction Operating Temperature Range	T_{JUNC}	25		100	°C

DC Characteristics

NOTE: For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supplies

VHH = 15.5V, VCC =7.5V, VCCO = 5.5V, VEE = -3.5V, VEEO = -1.5V, VDD = 1.8V, VDDA = 1.8V, VDGS=0V for all tests.

TABLE 4: DC ELECTRICAL SPECIFICATIONS – POWER SUPPLIES

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
POWER Setup A: Reset Condition							
C200	VCC Current Setup A	Chip Reset condition.	I_{CC_A}		230		mA
C201	VHH Current Setup A		I_{HH_A}		7		mA
C202	VCCO Current Setup A		I_{CCO_A}		28		mA
C203	VDD/A Current Setup A		I_{DD_A}		840		mA
C204	VEE Current Setup A		I_{EE_A}		275		mA
C205	VEEO Current Setup A		I_{EEO_A}		10		mA
POWER Setup B: DC3							
C210	VCC Current Setup B	All drivers set to HS mode. All comparators are set to differential mode. DVH_DAC, DVL_DAC and COMP DACs enabled. All other DACs disabled. DVH_DAC = 4.0V / DVL_DAC = 0.0V. CVA_DAC = 2.0V / CVB_DAC = 2.0V. Drive, Enable, and Comparator deskews enabled. PMU disconnected. No data toggling. All other register values are set to default reset conditions. No load output.	I_{CC_B}		375		mA
C212	VHH Current Setup B		I_{HH_B}		7		mA
C213	VCCO Current Setup B		I_{CCO_B}		28		mA
C214	VDD/A Current Setup B		I_{DD_B}		1380		mA
C215	VEE Current Setup B		I_{EE_B}		440		mA
C216	VEEO Current Setup B		I_{EEO_B}		10		mA
POWER Setup C: DC2							
C220	VCC Current Setup C	All drivers set to HS mode. All comparators are set to differential mode. DVH_DAC, DVL_DAC and COMP DACs enabled. All other DACs disabled. DVH_DAC = 4.0V / DVL_DAC = 0.0V. CVA_DAC = 2.0V / CVB_DAC = 2.0V. PMU disconnected. No data toggling. All other register values are set to default reset conditions. No load on output.	$I_{CC\_C\_Q}$		375		mA
C221	VHH Current Setup C		$I_{HH\_C\_Q}$		7		mA
C222	VCCO Current Setup C		$I_{CCO\_C\_Q}$		28		mA
C223	VDD/A Current Setup C		$I_{DD\_C\_Q}$		1030		mA
C224	VEE Current Setup C		$I_{EE\_C\_Q}$		440		mA
C225	VEEO Current Setup C		$I_{EEO\_C\_Q}$		10		mA
POWER Setup D: PMU2							
C240	VCC Current Setup D	All channels are set to Force Voltage mode. FV_DAC and PMU enabled. All other DACs disabled. FV_DAC = 2.0V. PMU_IRNG = 50mA range. All other register values are set to default reset conditions. No load on output.	$I_{CC\_D\_Q}$		260		mA
C241	VHH Current Setup D		$I_{HH\_D\_Q}$		7		mA
C242	VCCO Current Setup D		$I_{CCO\_D\_Q}$		28		mA
C243	VDD/A Current Setup D		$I_{DD\_D\_Q}$		840		mA
C244	VEE Current Setup D		$I_{EE\_D\_Q}$		260		mA
C245	VEEO Current Setup D		$I_{EEO\_D\_Q}$		10		mA
POWER Setup E: LD2							
C250	VCC Current Setup E	All DVH_DAC, DVL_DAC, COMP DAC's, VTT_DAC, ILSRC_DAC and ILSNK_DACs enabled. All channel drivers are set to HS mode. ILSRC_DAC and ILSNK_DAC set to maximum. VTT = 2.0V. PMU disconnected. All other register values are set to default reset conditions. No load on output.	$I_{CC\_E\_Q}$		270		mA
C251	VHH Current Setup E		$I_{HH\_E\_Q}$		7		mA
C252	VCCO Current Setup E		$I_{CCO\_E\_Q}$		28		mA
C253	VDD/A Current Setup E		$I_{DD\_E\_Q}$		880		mA
C254	VEE Current Setup E		$I_{EE\_E\_Q}$		340		mA
C255	VEEO Current Setup E		$I_{EEO\_E\_Q}$		10		mA

DC Electrical Specifications – Calibration Buses

TABLE 5: DC ELECTRICAL SPECIFICATIONS – CALIBRATION BUSES

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C168	EXT_FRC Voltage Range (Voltage measured at DOUT)	Measured at each DOUT pin	$V_{RNG\_EXTFRC\_20}$	V_{EE}+0.3		V_{CC}-0.4	V
C163	EXT_SNS_HI Voltage Range (Connected to each DOUT pin)	FV every DOUT, measure at pin	$V_{RNG\_EXTSNS\_HI}$	V_{EE}		V_{CC}	V
C388	EXT_SNS_LO Voltage Range (Connected to internal VEE, VCC)	FV every DOUT, measure at pin	$V_{RNG\_EXTSNS\_LO}$	-3		7	V
C164	EXT_FRC Resistance (all 8 channels). Note 1.	Force -2/6V at pin, measure at each DOUT pulling 1µA	R_{IN_EXTFRC}	50		95	Ω
C165	EXT_SNS_HI Resistance EXT_SNSE_LO Resistance	Force -2/6V at DOUT, measure at EXT_SNS_HI/LO by pulling 1µA	R_{OUT_EXTSNS}	18k		28k	Ω
C166	EXT_FRC Leakage Current (100mV from rails)	All switches open	I_{LEAK_EXTFRC}		±25		nA
C167	EXT_SNS_HI, EXT_SNS_LO Leakage Current	All switches open	I_{LEAK_EXTSNS}	-5		5	nA

Notes:

The EXT_FRC resistance is a combination of the FORCE_ENA and one of the FORCE[7:0] switches in series. The individual resistance of each switch is listed in Table 99 of this datasheet. The PMU CONNECT switch resistance is listed in Table 65.

DC Electrical Specifications – DUT Connection Pin

TABLE 6: DC ELECTRICAL SPECIFICATIONS – DUT CONNECTION PIN

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C177	DOUT Hi-Z Leakage Current (–2V ≤ DOUT ≤ 6V)		I_{LEAK_DOUT}	-5		5	nA
C185	DOUT Hi-Z Leakage Current (DOUT within 100mV of the VEE or 400mV VCC rail)	High temperature dependance	$I_{LEAK\_DOUT\_RAIL}$		±20		µA
C19	DOUT Hi-Z Capacitance	Measured at output to ground	C_{PIN_DOUT}		7		pF

DC Electrical Specifications – Pin Driver

TABLE 7: DC ELECTRICAL SPECIFICATIONS - PIN DRIVER

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C21	Driver Output Continuous DC Current Capability, Note 1	After settling time, Note 2	I_{OH_DRV}	-50		50	mA
C25	Driver Output Short Circuit Current, Note 1	Tested < 1µS	I_{SHORT_DRV}		70		mA
C207	Driver Output Impedance, Note 7	Drift BC to WC post calibration	R_{OUT_DRV}	47.5	50	52.5	Ω
C162	Driver output impedance trim resolution	Average change each code tested	R_{OUT_RES}		0.5		Ω/bit
High Voltage Mode							
C22	Driver Full Swing (|DVH – DVL|)	Tested, Note 3 Into High Impedance	V_{SWING_HV}	8			V
C23	Driver Level Max Output6 (DVL / DVH = 0xFFFF)	Into High Impedance	$V_{OH\_DRV\_HV}$	6			V
C24	Driver Level Min Output6 (DVL / DVH = 0x0000)	Into High Impedance	$V_{OL\_DRV\_HV}$			-2	V
C29	Driver Termination Max Output, Note 6 (VTT =0xFFFF)	VTT Mode, Note 5	V_{VTTH_HV}	6			V
C30	Driver Termination Min Output, Note 6 (VTT =0x0000)	VTT Mode	V_{VTTL_HV}			-2	V
	Driver Output Level DC Accuracy, Note 6						
C33	Pre-Calibration Accuracy (DVH, DVL, VTT)	(Post Offset adjust 2V)	$V_{ERR\_HV\_PRE}$		±200		mV
	Post-Calibration Accuracy (DVH, DVL, VTT)		$V_{ERR\_HV\_CAL}$	-5		5	mV
	Accuracy Temperature Error (DVH, DVL, VTT)	Measured 50-90C Char only					
C341	0V to 2V output.		$TE_{DRV\_HV\_2}$		0.3		mV/C
C342	2V to 4V output		$TE_{DRV\_HV\_4}$		0.4		mV/C
C343	-2V to 0V / 4 to 6V output		$TE_{DRV\_HV\_6}$		2		mV/C
High Speed Mode							
C26	Driver Full Swing (|DVH – DVL|)	Tested, Note 3 Into High Impedance	V_{SWING_HS}	4			
C27	Driver Level Max Output, Note 6 (DVL / DVH = 0xFFFF)	Into High Impedance	$V_{OH\_DRV\_HS}$	4			
C28	Driver Level Min Output, Note 6 (DVL / DVH = 0x0000)	Into High Impedance	$V_{OL\_DRV\_HS}$			0	V
C31	Driver Termination Max, Note 6 Output (VTT =0xFFFF)	VTT Mode, Note 5	V_{VTTH_HS}	4			V
C32	Driver Termination Min, Note 6 Output (VTT =0x0000)	VTT Mode	V_{VTTL_HS}			0	
C35	Driver Output Level DC Accuracy, Note 6. Pre-Calibration Accuracy (All Levels - DVH, DVL, VTT).		$V_{ERR\_HS\_PRE}$		±200		mV
	Post-Calibration Accuracy, Note 4. (All Levels - DVH, DVL, VTT)		$V_{ERR\_HS\_CAL}$	-5		5	mV
	Accuracy Temperature Error (DVH, DVL, VTT).	Measured 50-90C Char Only					
C361	0V to 2V output		$TE_{DRV\_HS\_2}$		.5		mV/C
C362	2 to 4V output		$TE_{DRV\_HS\_4}$		1		mV/C

NOTES:
1. Same spec for High Speed and High Voltage, but tested separately at high bias, low Rout. This is the minimum guaranteed output current before the driver clamp will start to limit the output.
2. Includes current for DVL, DVH, and VTT. Settling time will vary by load.
3. DOUT Vswing 50% = 2V only for testing.
4. Using 113-point calibration as described in white paper (reference)
5. VTT mode: Driver disabled; voltage set into high impedance.
6. Using offset value of 0x03. Full -2V to 6V range can be reached by using low HV_BIAS settings (0x00), but AC performance may not meet specifications if that setting is used.
7. System difference may cause up to 4Ω inaccuracy in ATE pre-shipped fuse map. One-time customer calibration in-system is recommended if

greater accuracy is required.

DC Electrical Specifications – High Speed Window Comparator

TABLE 8: DC ELECTRICAL SPECIFICATIONS – HIGH SPEED WINDOW COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	CVA/CVB DAC Accuracy Error.						
C89	Pre-Calibration	(Post Offset adjust at 2V)	$V_{ERR\_CMP\_PRE}$		±200		mV
C90	Post-Calibration		$V_{ERR\_CMP\_CAL}$	–5		5	mV
C91	Accuracy Temperature Error (CVA, CVB DACs)	Measured over 40C, char only. High codes measured; small codes have less drift	TE_{CMP_DAC}		250		µV/°C
	Compare Threshold offset, uncalibrated (can be calibrated out).						
C180	0V to 5V		$V_{ERR\_CMP\_THRSH\_5}$		5		mV
C181	-2V to 6V		$V_{ERR\_CMP\_THRSH\_6}$		30		mV
C182	Temperature Error of offset	Measured over 50C, proportional to voltage	TC_{CMP_THRSH}		±150		µV/°C

DC Electrical Specifications – Digital Pins

TABLE 9: DC ELECTRICAL SPECIFICATIONS – DIGITAL PINS

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Comparator Outputs (COMP_A_P_#, COMP_B_P_#, COMP_A_N_#, COMP_B_N_#) for both LVDS and CML Modes							
C92	Differential Voltage Full Swing	100Ω Differential Load	V_{SWING_CMP}		500		mV
C93	Common Mode Voltage Range	100Ω Diff Load (LVDS) VTT = VDDA (CML)	V_{CM_CMP}		V_{DD} -250m		V
Pin Driver Inputs (DATA_P_#, ENA_P_#, DATA_N_#, ENA_N_#)							
C105	Input Current	Hi-Z input termination mode	I_{LEAK_IN}			10	nA
C107	Differential Input Voltage Swing	All Termination Levels tested Vcm from 0.6V to 1.8. Swing must be below VDD rail.	V_{SWING_IN}	0.2		1.8	V
C104	Common Mode Voltage Range	Max swing cannot exceed VDD Rail	V_{CM_IN}	0.8	1.4	1.7	V
C106	Programmable Input Termination	100Ω Differential Setting	R_{IN_DE100}	80	100	120	Ω
		50Ω Single Ended Setting	R_{IN_DE50}	40	50	60	Ω
Serial Interface (SPI_SDI, SPI_SDO, SPI_CLK, CPI_CS) (SSTL18 only when termination is enabled)							
C1	SSTL Leakage Current	Terminations and outputs Disabled, tested VDD/GND	I_{LEAK_SSTL}		<10		µA
C2	SSTL Input High Voltage (DC)		V_{IH_SSTL}	$V_{DD}/2 + 0.150$		$V_{DD}+0.3$	V
C3	SSTL Input Low Voltage (DC)		V_{IL_SSTL}	-0.3		$V_{DD}/2 - 0.150$	V
C4	SSTL Output High Voltage (DC)	IOH=5	V_{OH_SSTL}	$V_{DD}/2 + 0.5$			V
C5	SSTL Output Low Voltage (DC)	IOL=-5	V_{OL_SSTL}			$V_{DD}/2 – 0.5$	V
Reset Pin (LVCMOS) and Alarm output (Open Drain)							
C6	Leakage Current	Inputs tested at VDD/GND	I_{LEAK_CMOS}		<10		µA
C7	Input High Voltage		V_{IH_CMOS}	$0.7*V_{DD}$		$V_{DD}+0.3$	V
C8	Input Low Voltage		V_{OH_CMOS}	-0.3		$0.2*V_{DD}$	V
C9	Output High Voltage	OD: Connect to 10KΩ pullup Tested with IOH=200µA	V_{OH_ALARM}	V_{DD} -0.2			V
C10	Output Low Voltage	IOL=-200µA	V_{OL_ALARM}			0.2	V

DC Electrical Specifications – Differential Mode Comparator

TABLE 10: DC ELECTRICAL SPECIFICATIONS – DIFFERENTIAL MODE COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C170	Common Mode Input Voltage Range	Channel A or Channel B	V_{RNG_DIF}	–1.5		+4.5	V
C171	Minimum Differential Swing	Channel A – Channel B	V_{MIN_DIF}	±0.05			V
C172	Maximum Differential Swing	Channel A – Channel B, max useful range	V_{SWING_DIF}			±1.1	V
C173	Input Offset Voltage	Offset measured at calibrated code for –0.5V and 0.5V with VCM = 1.5V	V_{OFS_DIF}	–400		+400	mV
C174	Input Offset Temperature Error		TE_{OFS_DIF}		±150		µV/°C
C175	Gain	Gain measured at calibrated code for –1.0V and 1.0V with VCM = 0.0V. Based on an ideal DAC transfer function	GM_{AMP_DIF}	1.0		1.2	V/V
C176	Gain Temperature Coefficient		TC_{AMP_DIF}		±850		ppm/°C
C275	Common Mode Error	Δ Offset measured at VCM = –1.5V and +4.5V, VDM = 0.0V	$\lvert CMR_{OFS\_DIF} \rvert$		1.0		mV/V
C276	DC PSR	Δ Offset measured at VCM = 0.0V	PSR_{OFS_DIF}		±5		mV/V
C270	CVA/CVB DAC Accuracy Error. Pre-Calibration	For both CM and Amplitude measurement DACs	$V_{ERR\_DCMP\_PRE}$		±200		mV
C271	CVA/CVB DAC Accuracy Error. Post-Calibration	For both CM and Amplitude measurement DACs	$V_{ERR\_DCMP\_CAL}$	–5		5	mV
C272	Accuracy Temperature Error (CVA, CVB DACs)	For both CM and Amplitude DACs. Measured over 40°C, char only. High codes largest, low codes have smaller error	TE_{DCMP_DAC}		10		mV
C273	CM Compare Threshold offset, uncalibrated (Can be calibrated out)	Offset on Common Mode output valid up to 1.1V differential input	$V_{ERR\_DCMP\_THRSH}$		±50		mV
C274	CM Temperature Error of offset	Offset tempco on common mode output over 50°C, proportional to CM voltage	TC_{DCMP_THRSH}		±800		µV/°C

DC Electrical Specifications – PPMU Force Voltage

TABLE 11: DC ELECTRICAL SPECIFICATIONS – PPMU FORCE VOLTAGE

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C108	Force Voltage Error	Measured after calibration. Valid for all min/max current in ranges	V_{ERR_FV}	–5		+5	mV
C120	Force Voltage Temperature Error	Based on worst case code shifting over 50°C	TE_{FV}		300		µV/°C
C300	DGS Tracking Range	Force offset on DGS, measure change on PMU FV (ATE)		-100		100	mV

DC Electrical Specifications – PPMU Force Current

TABLE 12: DC ELECTRICAL SPECIFICATIONS – PPMU FORCE CURRENT

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Force Current Error	Measured at 2V, no Common Mode Error. Measured after calibration.					
	IR0 (±2µA Range), IR1(±20µA Range)	Untested					
C111	IR2 (±200µA Range)		$I_{ERR\_FI\_200u}$	-1		+1	µA
C112	IR3 (±2mA Range)		$I_{ERR\_FI\_2m}$	-10		+10	µA
C113	IR4 (±50mA Range)		$I_{ERR\_FI\_50m}$	-250		+250	µA
	FI Temperature Error						
C121	IR2 (±200µA Range)		TE_{FI_200u}		±40		nA/°C
C151	IR3 (±2mA Range)		TE_{FI_2m}		±400		nA/°C
C152	IR4 (±50mA Range)		TE_{FI_50m}		±10		µA/°C
C387	Common Mode Error	Measured as a %FS	$I_{ERR\_FI\_CM}$		1		%

DC Electrical Specifications – PPMU Measure Voltage

TABLE 13: DC ELECTRICAL SPECIFICATIONS – PPMU MEASURE VOLTAGE

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C119	Measure Voltage Error	Measured at MON_0 and MON_1	V_{ERR_MV}	–5		+5	mV
C122	Measure Voltage Temperature Error	Change proportional to forced voltage	TE_{MV}		±40		µV/°C

DC Electrical Specifications – PPMU Measure Current

TABLE 14: DC ELECTRICAL SPECIFICATIONS – PPMU MEASURE CURRENT

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
	Measure Current Error	Tested 2V only. Measured after calibration.					
C114	IR0 (±2µA Range)		$I_{ERR\_MI\_2u}$	-10		+10	nA
C115	IR1 (±20µA Range)		$I_{ERR\_MI\_20u}$	-100		+100	nA
C116	IR2 (±200µA Range)		$I_{ERR\_MI\_200u}$	-1		+1	µA
C117	IR3 (±2mA Range)		$I_{ERR\_MI\_2m}$	-10		+10	µA
C118	IR4 (±50mA Range)		$I_{ERR\_MI\_50m}$	-250		+250	µA
	MI Temperature Error						
C123	IR4 (±50mA Range)		$TE_{MI\_50m\ I}$		±5		µA/°C
C153	IR3 (±2mA Range)		TE_{MI_2m}		±150		nA/°C
C154	IR2 (±200µA Range)		TE_{MI_200u}		±15		nA/°C
C155	IR1 (±20µA Range)		TE_{MI20u}		±1.5		nA/°C
C156	IR0 (±2µA Range)		TE_{MI_2u}		±0.5		nA/°C
C157	Common Mode Error		$I_{ERR\_MI\_CM}$		1		%

DC Electrical Specifications – PPMU Go-No-Go Comparator

TABLE 15: DC ELECTRICAL SPECIFICATIONS – PPMU GO-NO-GO COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C143	Threshold Error, Post Cal		V_{ERR_PMUCV}	–5		+5	mV
C144	Threshold Temperature Error	Over 50°C	T_{EPMUCV}		±150		µV/°C

DC Electrical Specifications – Voltage Clamp

TABLE 16: DC ELECTRICAL SPECIFICATIONS - VOLTAGE CLAMP

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C124	Voltage Clamp Error, Calibrated	Measured through 50Ω	V_{ERR_VCLAMP}		±100		mV
C125	Voltage Clamp Temperature Error	Varies Per Code	TE_{VCLAMP}		600		µV/°C
C126	Voltage Clamp Low Range		$V_{RNG\_VCLAMP\_LO}$	–1.8		2.4	V
C127	Voltage Clamp High Range		$V_{RNG\_VCLAMP\_HI}$	0.5		5	V
C128	Voltage Clamp DAC Resolution		V_{RES_VCLAMP}		80		mV

DC Electrical Specifications – Current Clamp

Current clamps are only for device gross protection, not precision control.

TABLE 17: DC ELECTRICAL SPECIFICATIONS - CURRENT CLAMP

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C129	50mA Current Clamp Error	Measured through 50Ω	$I_{ERR\_ICLAMP50}$		±5		mA
C130	50mA Current Clamp Temperature Error	Decreases with lower codes	$TE_{ICLAMP50}$		600		µA/°C
C131	50mA Positive Current Clamp Maximum	Measured with code 0xFF	$I_{MAX\_PICLAMP50}$	55	80	98	mA
C132	50mA Negative Current Clamp Maximum	Measured with code 0xFF	$I_{MAX\_NICLAMP50}$	–85	–70	–52	mA
C385	50mA Positive Current Clamp Minimum	Measured with code 0x01	$I_{MIN\_PICLAMP50}$			5	mA
C386	50mA Negative Current Clamp Minimum	Measured with code 0x01	$I_{MIN\_NICLAMP50}$	-10			mA
C133	50mA Voltage Clamp DAC Resolution		$I_{RES\_ICLAMP50}$		0.55		mA
C134	2mA Current Clamp Error	Measured through 50Ω	$I_{ERR\_ICLAMP2}$		±1		mA
C135	2mA Current Clamp Temperature Error		$TE_{ICLAMP2}$		5		µA/°C
C136	2mA Positive Current Clamp Threshold		$I_{MAX\_ICLAMP2}$	3			mA
C137	2mA Negative Current Clamp Threshold		$I_{MIN\_ICLAMP2}$			-3	mA
C138	2mA Voltage Clamp DAC Resolution		$I_{RES\_ICLAMP2}$		500		µA

DC Electrical Specifications – Active Load

TABLE 18: DC ELECTRICAL SPECIFICATIONS - ACTIVE LOAD

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C145	Source/Sink Post Cal Error (1/24mA)	Tested into 50Ω	I_{ERR_ILOAD}	–1		+1	%FS
C160	VCOM keep out for FS current (1/24mA), Note 1		$V_{COM\_KEEPOUT}$	±200			mV
C146	Low Current (1/24mA)	0x0000 code (abs value)	I_{MIN_ILAOD}		10/270		µA
C147	High Current Sink/Source (24mA)	0xFFFF code	$I_{MAX\_ISNK/ISRC}$	–24/24		-35/37	mA
C148	High Current Sink/Source (1mA)	0xFFFF code	$I_{MAX\_ISNK/ISRC}$	–1/1		-1.3/1.3	mA
C149	Source Current Temperature Error	Measured 50-100C at high code. Lower code drift smaller.	TE_{ISRC}		12		µA/°C
C150	Sink Current Temperature Error	Measured 50-100C at high code. Lower code drift smaller.	TE_{ISNK}		5		µA/°C
C161	VCOM Temperature Error	Measured 50-100C	TE_{VCOM}		3		mV/°C

NOTES:

1. Minimum voltage above or below VCOM where current is guaranteed to be within spec. May require calibration.

AC Characteristics

NOTE: For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications – Pin Driver

Slew Rate = Fastest Setting, Deskew = Bypassed, 1KΩ Far End termination unless noted

TABLE 19: AC ELECTRICAL SPECIFICATIONS - PIN DRIVER:

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High Voltage Mode							
	Maximum Operating Frequency – Fmax 10% Amplitude Reduction	See Figure 12					
C46	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)	Mid bias level	$F_{MAX\_HV0.5}$	150			MHz
C47	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)	Fastest slew rate	$F_{MAX\_HV1.0}$	145			MHz
C48	3.0V Programmed Swing (DVL = 0V, DVH = 3.0V)	Rout calibrated	$F_{MAX\_HV3.0}$	115			MHz
C49	6.0V Programmed Swing (DVL = -1V, DVH = 5.0V)		$FM_{AX\_HV6.0}$	70			MHz
	Minimum Pulse Width measured at 50% amplitude point when waveform amplitude drops to 90% of programmed value	See Figure 7 10MHz tested fastest SLEW, ROUT calibrated					
C50	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)	Measured 50-100C at high code. Lower code drift smaller.	$T_{PWM\_HV0.5}$		3		ns
C51	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)	Measured 50-100°C	$T_{PWM\_HV1.0}$		3		ns
C52	3.0V Programmed Swing (DVL = 0V, DVH = 3.0V)		$T_{PWM\_HV3.0}$		3.2		ns
C53	6.0V Programmed Swing (DVL = -1V, DVH = 5.0V)		$T_{PWM\_HV6.0}$		4.5		ns
C62	Driver Pulse Width Dispersion (abs value of the Δ|Tpwin – Tpwout|as pw changes from 25ns down to the pwmin, 1.0V swing, 1ns MPW, 1MHz tested)	See Figure 7	T_{PWD_HV}		20		ps
	Driver Overshoot/Undershoot/Pre-Shoot	See Figure 13 Worst case value reported, max slew used					
C79	0.5V to 1V Programmed Swing		$V_{SHOOT\_HV\_LO}$		1		%
C82	3.0V to 6V Programmed Swing		$V_{SHOOT\_HV\_HI}$		4		%
	Driver Crosstalk (Any Channel to Any Other Channel)	7 toggles with 1 victim channel. See test setup in characterization.					
C310	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)		0.5V Xtalk_HV		25		mVpp
C311	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)		1.0V Xtalk _HV		40		mVpp
C312	3.0V Programmed Swing (DVL = 0V, DVH = 3.0V)		3.0V Xtalk _HV		75		mVpp
C313	6.0V Programmed Swing (DVL = -1V, DVH = 5.0V)		5.0V Xtalk _HV		85		mVpp
C72	Driver Propagation Delay (DVL = 0V, DVH = 0.8V) DATA to DOUT_FORCE (Deskews bypassed)	See Figure 10	T_{PDR_HV}, T_{PDF_HV}		3.5		ns
C75	Output Active to Hi-Z	See Figure 9	T_{DIS_HV}		7		ns
C77	Output HiZ to Active	See Figure 9	T_{EN_HV}		4		ns
C88	Delay Tempco		TC_{DLY_HV}		3		ps/°C
	Driver Programmable Slew Rate	10/90 R/F tested HVBias=8					
C383	Range		SR_{RNG_HV}	0.25		1.8	V/ns
C384	Resolution (4 bits)		SR_{RES_HV}		0.1		V/ns

AC Electrical Specifications – Pin Driver

Deskew = Bypassed, 50Ω Far End termination unless noted. Output swings will be about ½ voltage of programmed swings.

TABLE 20: AC ELECTRICAL SPECIFICATIONS - PIN DRIVER

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High Speed Mode							
	Maximum Operating Frequency – Fmax 10% Amplitude Reduction	See Figure 12 Mid Bias level					
C400	Absolute FMAX, Note 1	See Note 1	F_{MAX_ABS}		500		MHz
C54	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)	No pre-emphasis	$F_{MAX\_HS0.5}$	400			MHz
C55	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)	Rout calibrated	$F_{MAX\_HS1.0}$		370		MHz
C56	2.0V Programmed Swing (DVL = 0V, DVH = 2.0V)		$F_{MAX\_HS2.0}$		320		MHz
C57	4.0V Programmed Swing (DVL = 0V, DVH = 4.0V)		$F_{MAX\_HS4.0}$		250		MHz
	Minimum Pulse Width measured at 50% point when waveform amplitude drops to 90% of programmed value ()	See Figure 11					
C58	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)	Measured 50-100°C	$T_{PWM\_HS0.5}$		1.2		ns
C59	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)		$T_{PWM\_HS1.0}$		1.2		ns
C60	2.0V Programmed Swing (DVL = 0V, DVH = 2.0V)		$T_{PWM\_HS2.0}$		1.2		ns
C61	4.0V Programmed Swing (DVL = 0V, DVH = 4.0V)	See Figure 7	$T_{PWM\_HS4.0}$		1.2		ns
	Driver Rise/Fall Time	See Figure 11 Load dependent, 50Ω to ground used, all levels 20/80%					
C64	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)		$T_{R\_0.5}/T_{F\_0.5}$		500		ps
C65	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)		$T_{R\_1.0}/T_{F\_1.0}$		500		ps
C66	2.0V Programmed Swing (DVL = 0V, DVH = 2.0V)	7 toggles with 1 victim channel. See test setup in characterization.	$T_{R\_2.0}/T_{F\_2.0}$		500		ps
C67	4.0V Programmed Swing (DVL = 0V, DVH = 4.0V)		$T_{R\_4.0}/T_{F\_4.0}$		550		ps
	Driver Rise/Fall Time Matching (50Ω terminated)	See Figure 11 Load dependent, 50Ω to ground used, all levels 20/80%					
C68	0.5V Programmed Swing (DVL = 0V, DVH = 0.5V)		$T_{\Delta RF\_0.5}$		±5		%
C69	1.0V Programmed Swing (DVL = 0V, DVH = 1.0V)		$T_{\Delta RF\_1.0}$		±3		%
C70	2.0V Programmed Swing (DVL = 0V, DVH = 2.0V)	See Figure 10	$T_{\Delta RF\_2.0}$		±5		%
C71	4.0V Programmed Swing (DVL = 0V, DVH = 4.0V)		$T_{\Delta RF\_4.0}$		±5		%
C63	Driver Pulse Width Dispersion (abs value of the Δ|Tpwin – Tpwout| as pw changes from 25ns down to the pwmin, 1.0V swing, 1ns MPW)	See Figure 7	T_{PWD_HS}		20		ps
	Driver Overshoot/Undershoot/Pre-shoot	See Figure 13					
C86	0.5V to 4V Programmed Swing	Output 0.25-2V	V_{SHOOT_HS}		±1		%
C74	Output Active to Hi-Z	See Figure 9	T_{DIS_HS}		3		ns
C76	Output HiZ to Active	See Figure 9	T_{EN_HS}		3		ns
C87	Drive Path Propagation Delay Tempco		TC_{DLY_HS}		3		ps/°C

NOTES:

1. Parts need tuning for 500MHz. This includes a higher DRV_BIAS_HS setting (0xA-F) which will consume more power, and a custom ROUT setting down to ~48Ω. The FMAX (90% output-point) will vary with programmed amplitude, normally about 1V.

AC Electrical Specifications – High Speed Window Comparator

Deskew = Bypassed

TABLE 21: AC ELECTRICAL SPECIFICATIONS – HIGH SPEED WINDOW COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C97	Comparator Path Propagation Delay Tempco		TC_{DLY_CV}		5		ps/°C
C98	Comparator Minimum Pulse Width	90% output height	T_{PWM_CV}		1		ns
C94	Comparator Output Rise/Fall Time (20% to 80% Amplitude)	Tested as LVDS	T_{R_CV}/T_{F_CV}		330		ps
C99	Comparator Equivalent Bandwidth	Calculated from difference between fast edge (<100pS) and output edge	F_{BW_CV}		1		GHz
C100	Comparator Input Waveform Tracking (0-2V step, 100ps rise, 0.4, 1, 1.6V)	See Figure 6	$\Delta T_{PDR\_CV/V}$ $\Delta T_{PDF\_CV/V}$		1.8		Δns/V
C101	Common Mode Dispersion (DOUT_X Common Mode Voltage = –1V to 5V, DOUT_X Signal = 10MHz, 1Vpp square wave w/50% duty cycle, Tr/Tf = 1ns, CVA/CVB = 50% of square wave amplitude)	See Figure 3	$\Delta T_{PDR\_CV/CMV}$ $\Delta T_{PDF\_CV/CMV}$		18		Δps/V
C103	Overdrive Dispersion (Overdrive = 200mV to 1V, 1V/ns input slew rate)	See Figure 5	$\Delta T_{PDR\_CV/ODV}$ $\Delta T_{PDF\_CV/ODV}$		4		Δps/V
C102	Pulse Width Dispersion (Sweep input PW from 50ns to MPW for 1Vpp swing and monitor TPDR_CV, TPDF_CV	See Figure 4 in linear region	$\Delta T_{PDR\_CV/TPW}$ $\Delta T_{PDF\_CV/TPW}$		26		Δps/ns

AC Electrical Specifications – Differential Mode Comparator

All AC tests performed after DC levels calibration; 1MHz, input transition time = 50ps, 20-80%; outputs terminated 50Ω to GND (LVDS)

TABLE 22: AC ELECTRICAL SPECIFICATIONS - DIFFERENTIAL MODE COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C193	Compare path Propagation Delay Tempco		TC_{DLY_DF}		7		ps/°C
C194	Comparator Minimum Pulse Width	90% output height with 0/1V inputs compared at 0.5V Amp	T_{PWM_DF}		1		ns
C195	Comparator	Calculated from difference between fast edge (50pS) and output edge	F_{BW_DF}		1		GHz

AC Electrical Specifications – PPMU Comparator

TABLE 23: AC ELECTRICAL SPECIFICATIONS - PPMU COMPARATOR

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C322	Compare Path Delay Tempco	Mean shift over time	TC_{DLY_PMU}		100		ps/°C
C323	FMAX, Note 1	0.4-0.8V input, CVA/B 600mV	T_{FMAX_PMU}		1		MHz

NOTES:

1. It is not recommended to use the PPMU Comparator with AC signals, but it will reliably toggle with this input.

AC Electrical Specifications – Timing Deskew

These specifications apply to all delay lines in Driver, Comparator, and PMU paths for all channels. Full delay measured from bypassed.

TABLE 24: AC ELECTRICAL SPECIFICATIONS - TIMING DESKEW

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C37	Coarse LSB Delay	Room Temp, Char Only	T_{DLY_CRS}		700		pS
C38	Medium LSB Delay	Room Temp, Char Only	T_{DLY_MED}		150		pS
C39	Fine LSB Delay	Room Temp, Char Only	T_{DLY_FINE}		18		pS
C40	Rising edge adjustment unit delay	Room Temp, Char Only	T_{DLY_REA}		80		pS
C41	Falling edge adjustment unit delay	Room Temp, Char Only	T_{DLY_FEA}		15		pS
C42	Maximum delay line achievable delay	50C, Max code, Note 1	T_{DLY_MAX}	10			nS
C45	Delay line drift, factory compensated	Char only, Tj 50 to 100, delay set to 10nS, Note 2	TC_{DLY_COMP}		±2		pS/°C per nS

NOTES:

1. See deskew section for maximum code definition.
2. Better drift can be achieved with manual calibration of PTAT, but 0x1C is coded for typical production parts. Drift from all channels from characterization.

AC Electrical Specifications – Serial Interface

TABLE 25: AC ELECTRICAL SPECIFICATIONS - SERIAL INTERFACE

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C11	SPI Clock Frequency		F_{MAX_SCLK}			100	MHz
C12	Chip Select Setup Time	Max assert time after pos-edge of 1st cycle clock.	T_{SU_CS}			800	ps
C13	Chip Select Hold Time	De-assert in 31st cycle, measured from neg-edge of 32nd clock	T_{HO_CS}			-200	ps
C14	Serial Clock High Time		T_{PWH_SCLK}	2			ns
C15	Serial Clock Low Time		T_{PWL_SCLK}	2			ns
C16	Data In Setup Time		T_{SU_DIN}	2			ns
C17	Data In Hold Time		T_{HO_DIN}	2			ns
C18	Data Out Valid Time	Clk neg-edge to SDO Valid	T_{VAL_DOUT}			4	ns
C20	Data Out Tri-State	CS rise to SDO undriven, not measured, by design	T_{TS_DOUT}		4		ns
C206	Data Out Enable	CS fall to SDO driven	T_{EN_DOUT}	2			nS

AC Electrical Specifications – PPMU

TABLE 26: AC ELECTRICAL SPECIFICATIONS – PPMU

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C139	PMU Settling Time, High Step (0 to +.5V, High Cload = 10nF, IR4)	PMU FV into pure Cload to ground. 10% to last ring > 5mV	$T_{STL\_HSTP/HC}$		100		µs
C140	PMU Settling Time, High Step (0 to 5V, Low Cload = 100pF, IR4)		$T_{STL\_HSTP/LC}$		70		µs
C141	PMU Settling Time, Low Step (100mV step, High Cload = 10nF, IR4)		$T_{STL\_LSTP/HC}$		60		µs
C142	PMU Settling Time, Low Step (100mV step, Low Cload = 100pF, IR4)		$T_{STL\_LSTP/LC}$		50		µs

AC Electrical Specifications – Active Load

TABLE 27: AC ELECTRICAL SPECIFICATIONS - ACTIVE LOAD

SPEC #	PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
C280	Iload Output Active to HiZ Time (Real Time Control)	50% rise of EN to Iload (24mA) dropping measurable current	T_{DIS_ILOAD}		3		ns
C281	Iload Output HiZ to Active (Real Time Control)	50% fall of EN to Iload sourcing measurable current (24mA)	T_{EN_ILOAD}		5		ns

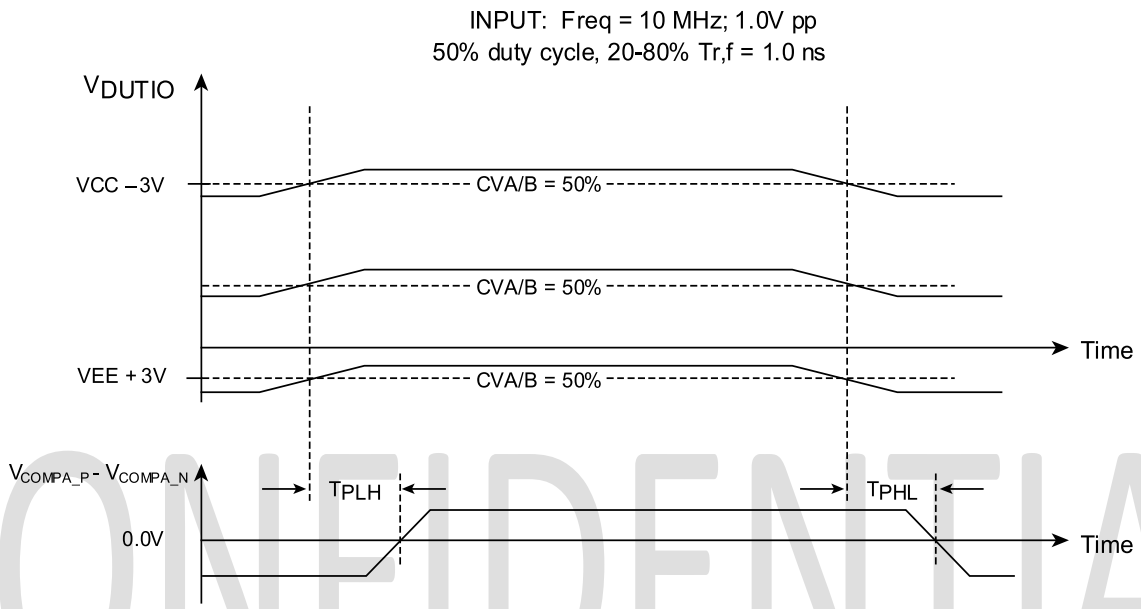


FIGURE 4: COMPARATOR DISPERSION: COOMMON MODE MEASUREMENT DEFINITION

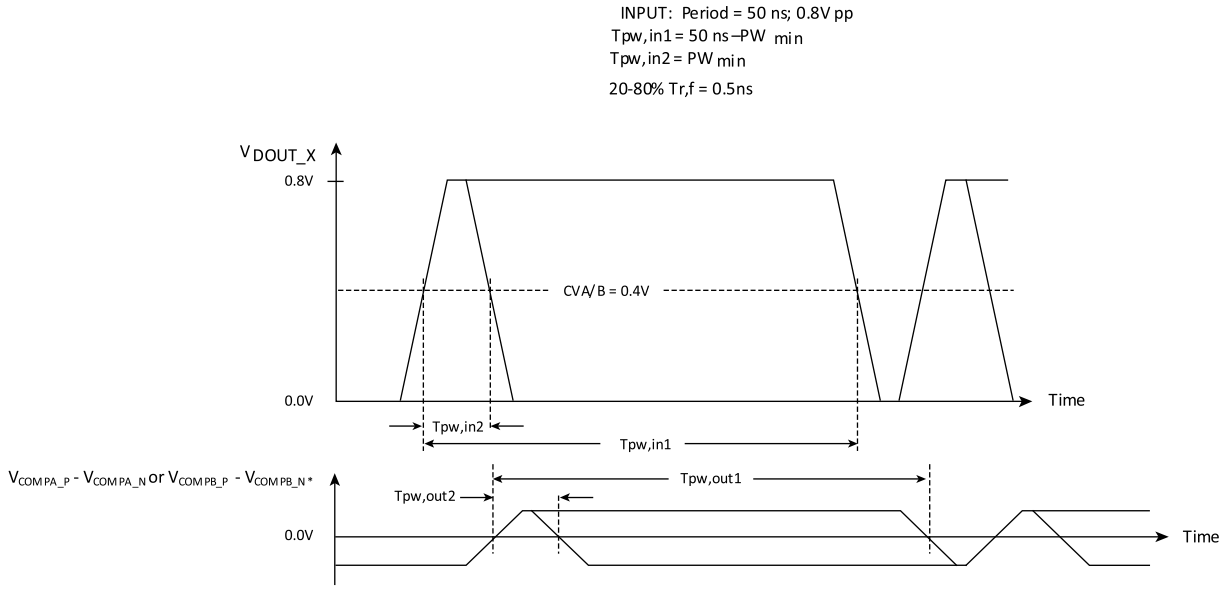


FIGURE 5: COMPARATOR DISPERSION: PULSE WIDTH MEASUREMENT DEFINITION

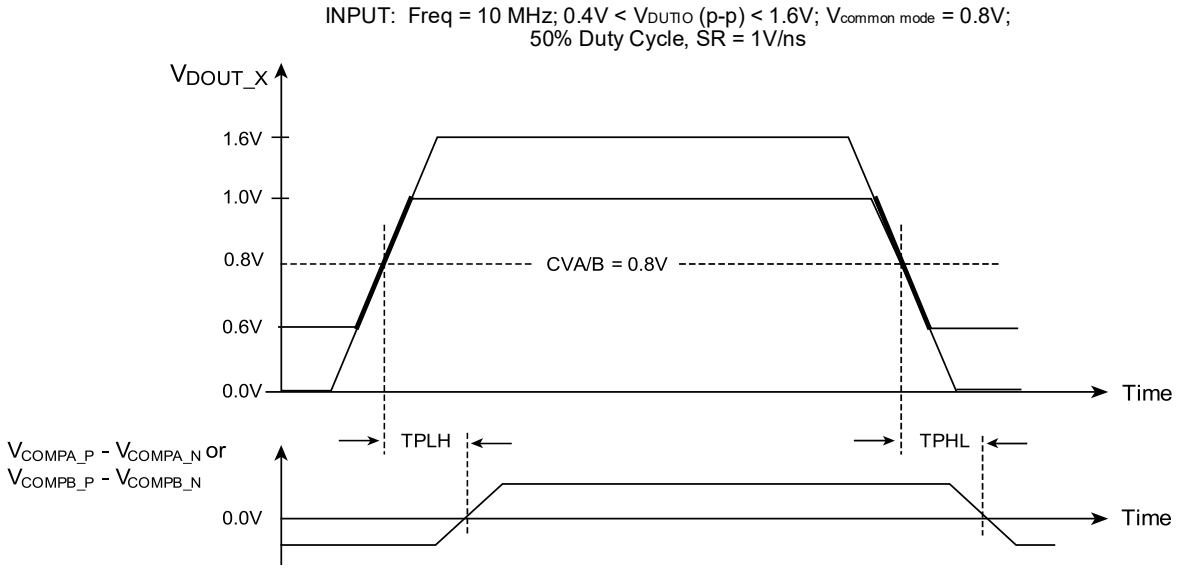


FIGURE 6: COMPARATOR DISPERSION: OVERDRIVE MEASUREMENT DEFINITION

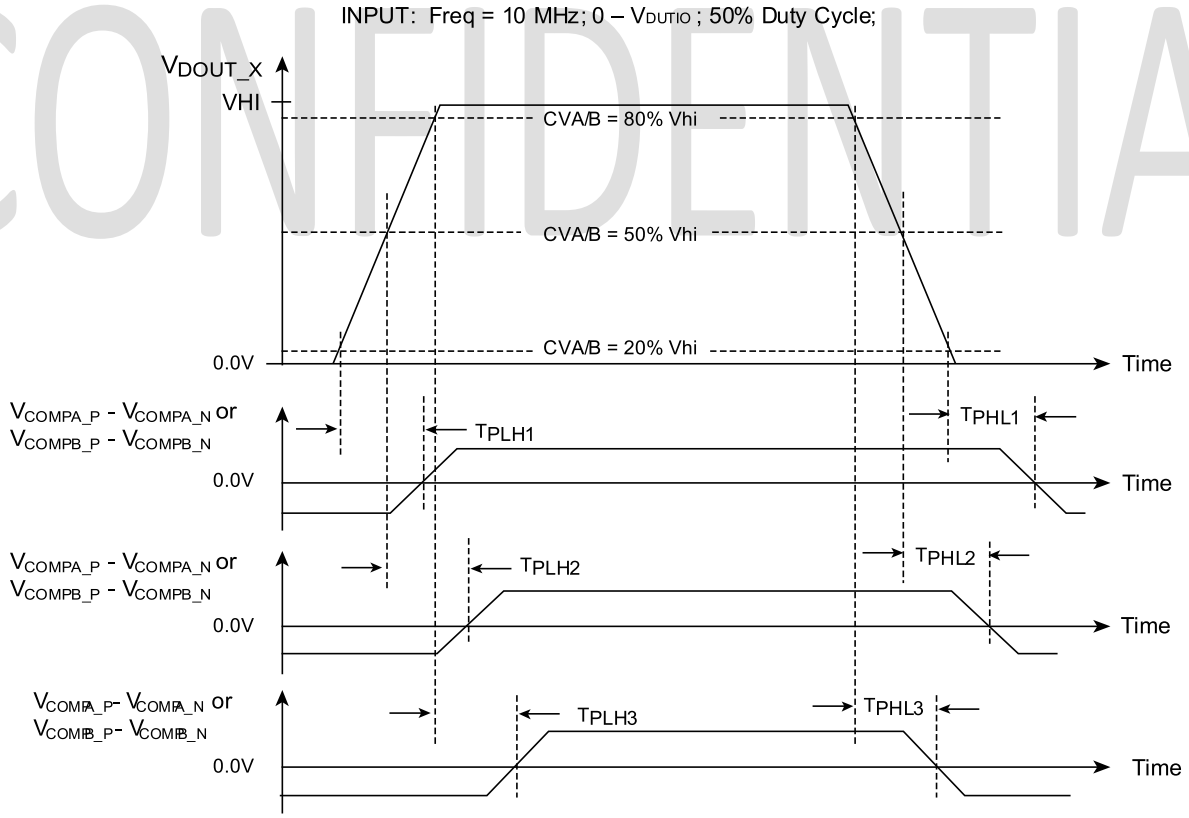
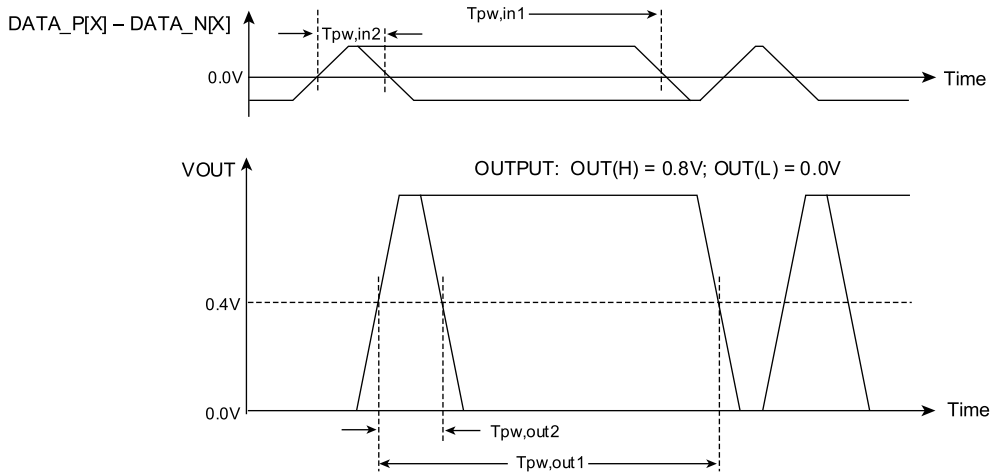


FIGURE 7: COMPARATOR DISPERSION: WAVEFORM TRACKING MEASUREMENT DEFINITION

Period = 50 ns
Tpw, in1 = 50 ns – Pwmin
Tpw, in2 = PW_{min}



Δ Tpw = |(Tpw, in1 – Tpw, out1)– (Tpw, in2– Tpw, out2)|

The measured result is the maximum absolute value of the change in [Tpw,in-Tpw,out] as the P.W. changes from 25ns to the endpoints of PW_{MIN} and [50ns-PW_{MIN}]

FIGURE 8: DRIVER DISPERSION: PULSE WIDTH MEASUREMENT DEFINITION

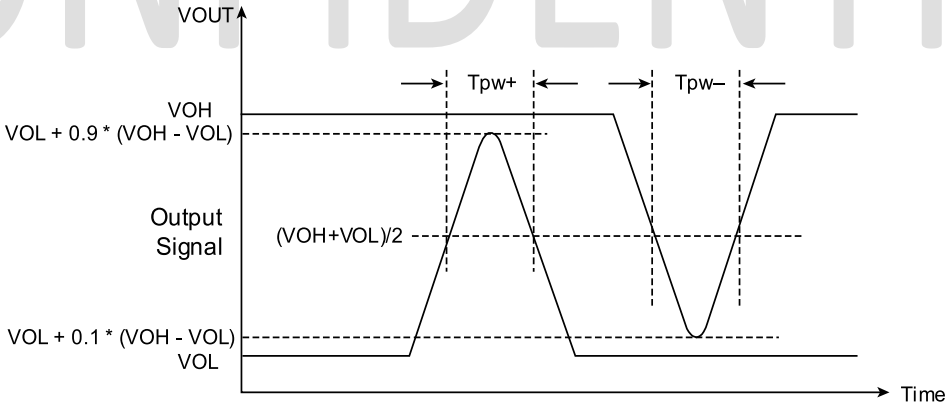
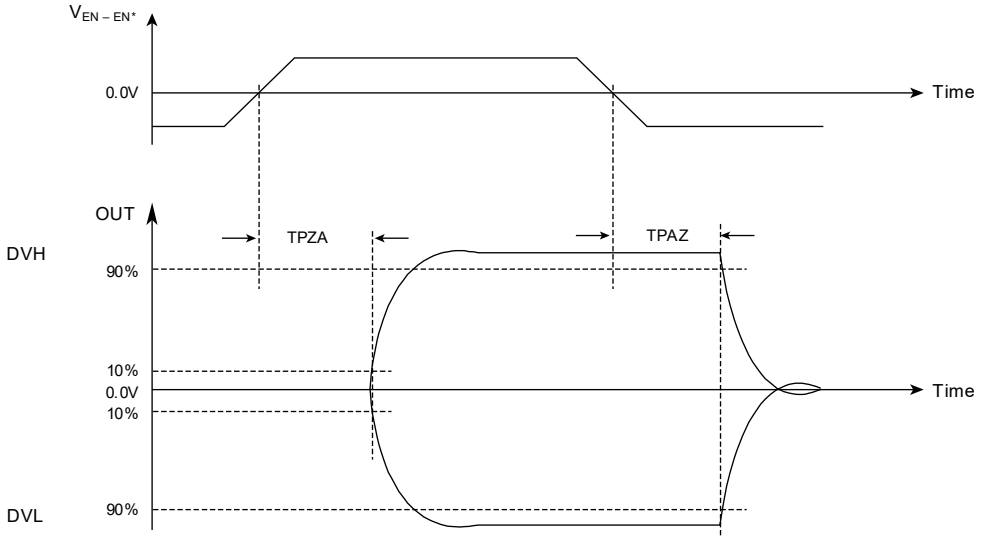


FIGURE 9: DRIVER MINIMUM PULSE WIDTH MEASUREMENT DEFINITION



(R LOAD at OUT = 50Ω to GND; DVH = +800mV, DVL = -800mV programmed)

Data is taken for testing with VTT enabled at 0V

FIGURE 10: DRIVER HIZ ENABLE/DISABLE MEASUREMENT DEFINITION

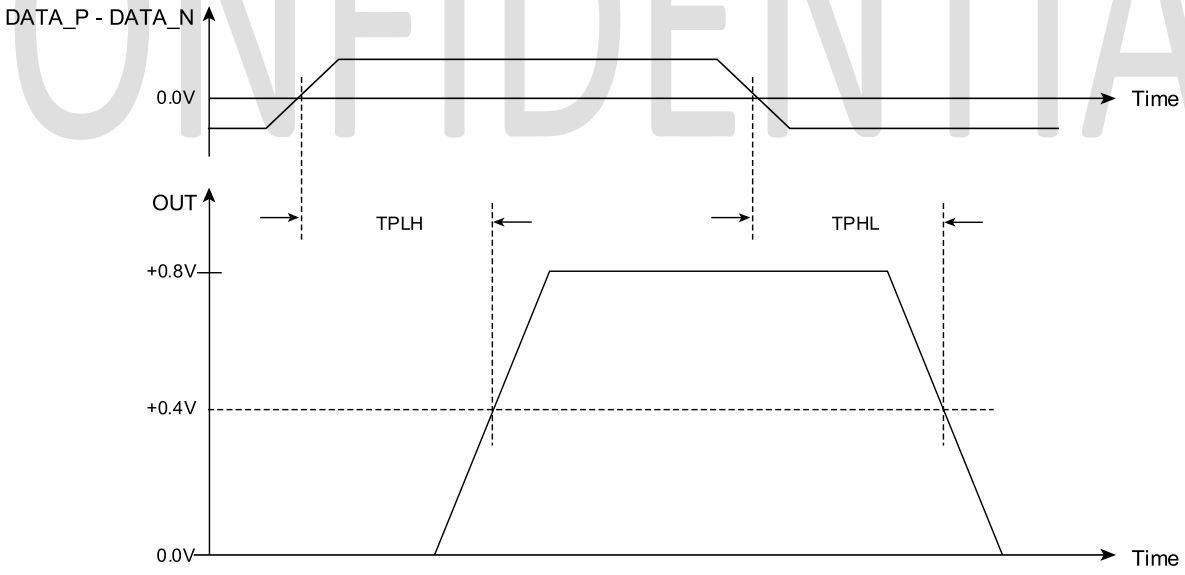
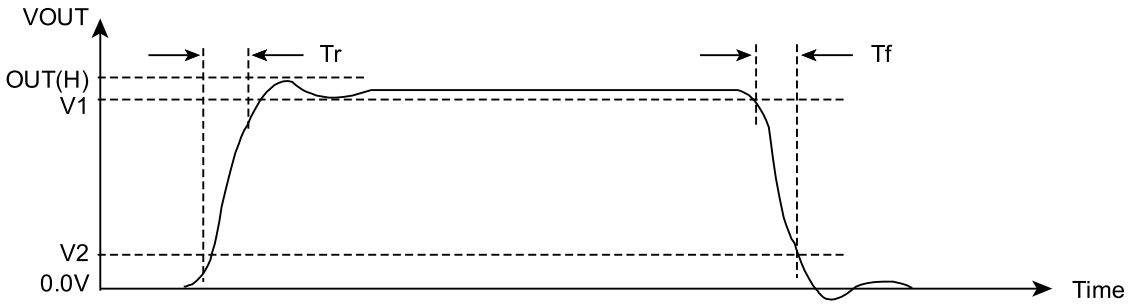


FIGURE 11: DRIVER PROPAGATION DELAY: DHI TO OUT, SYMMETRY AND TRACKING SKEW MEASUREMENT DEFINITION



V1 is 0.9* OUT(H) for 3V and higher, 0.8* OUT(H) for 1V and lower
V2 is 0.1* OUT(H) for 3V and higher, 0.2* OUT(H) for 1V and lower

FIGURE 12: TR/TF

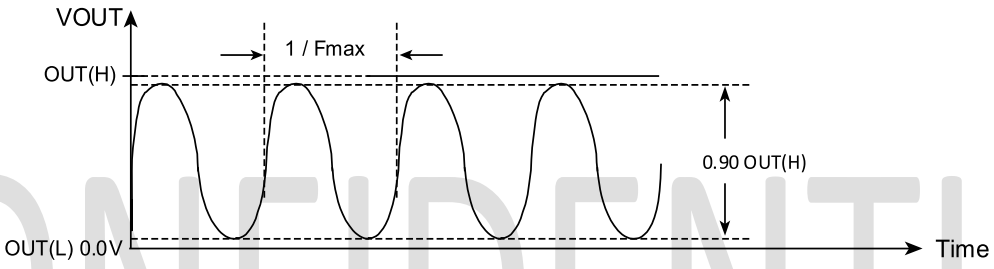
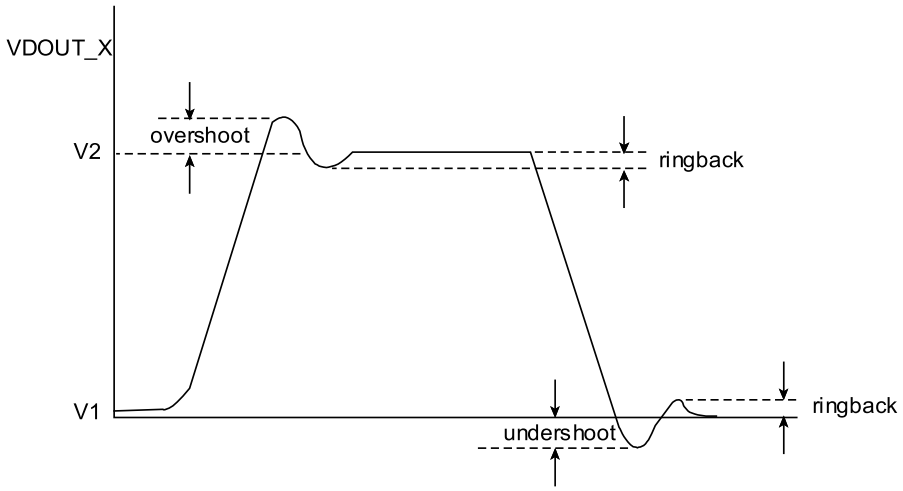


FIGURE 13: DRIVER FMAX MEASUREMENT DEFINITION



Test Cases: V1:V2 = DVL:DVH or DVT:DVH or DVL:DVT

FIGURE 14: DRIVER OVERSHOOT, UNDERSHOOT AND RINGBACK

Datasheet Nomenclature

External Signal Nomenclature

All input and output pins, when referred to in the datasheet or in any circuit diagram, use the following conventions:

- All capital letters (i.e., DATA_P_0),
- Underscores for clarity (i.e., EXT_FRC),
- Shown next to an I/O circle in any figure,
- Pound sign used to signify that the signal name applies to all channels (i.e., DATA_P_#).

High Speed Control

All real-time control and observations are accomplished via the real-time input and output signals.

- DATA_P_#, DATA_N_# (Differential Inputs)
- ENA_P_#, ENA_N_# (Differential Inputs)
- COMPA_P_#, COMPA_N_# (Differential Outputs)
- COMPB_P_#, COMPB_N_# (Differential Outputs)

Analog Reference

All on-chip analog functions are related to one of several off-chip precision reference inputs:

- VREF
- RREF

These external references are used to provide accurate and stable analog circuit performance that does not vary over time, temperature, supply voltage, or process changes.

SPI Programmed Control Line

All chip setup, configuration control, and writing to and reading back of the internal registers is controlled through the 4-bit serial SPI port. The SPI port is typically used to setup the operating mode of the chip prior to executing a test, or to change modes during a test.

An internal register chart in this datasheet documents all programmable control signals and their addresses and shows how to program each internal signal.

Any internal signal, DAC level, or control signal that is programmed via the SPI port uses a different nomenclature:

- All letters in the word are capitalized.
- Underscores are used for clarity.
- Shown with a Register square in any figure.

Control lines, internal registers, and other inputs are defined in the Host Serial Bus Data section and listed in the Register Map section of this datasheet.

Datasheet Symbols

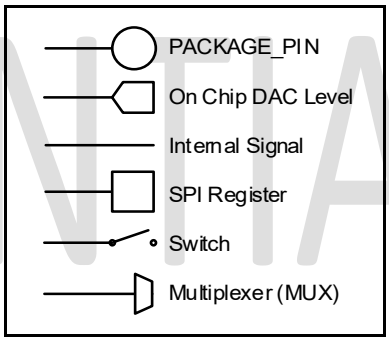


FIGURE 15: DATASHEET SYMBOLS

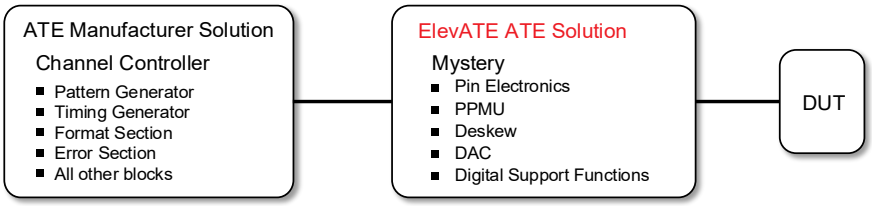


FIGURE 16: ELEVATE ATE SOLUTION

Driver/VTT/Load Block Diagram

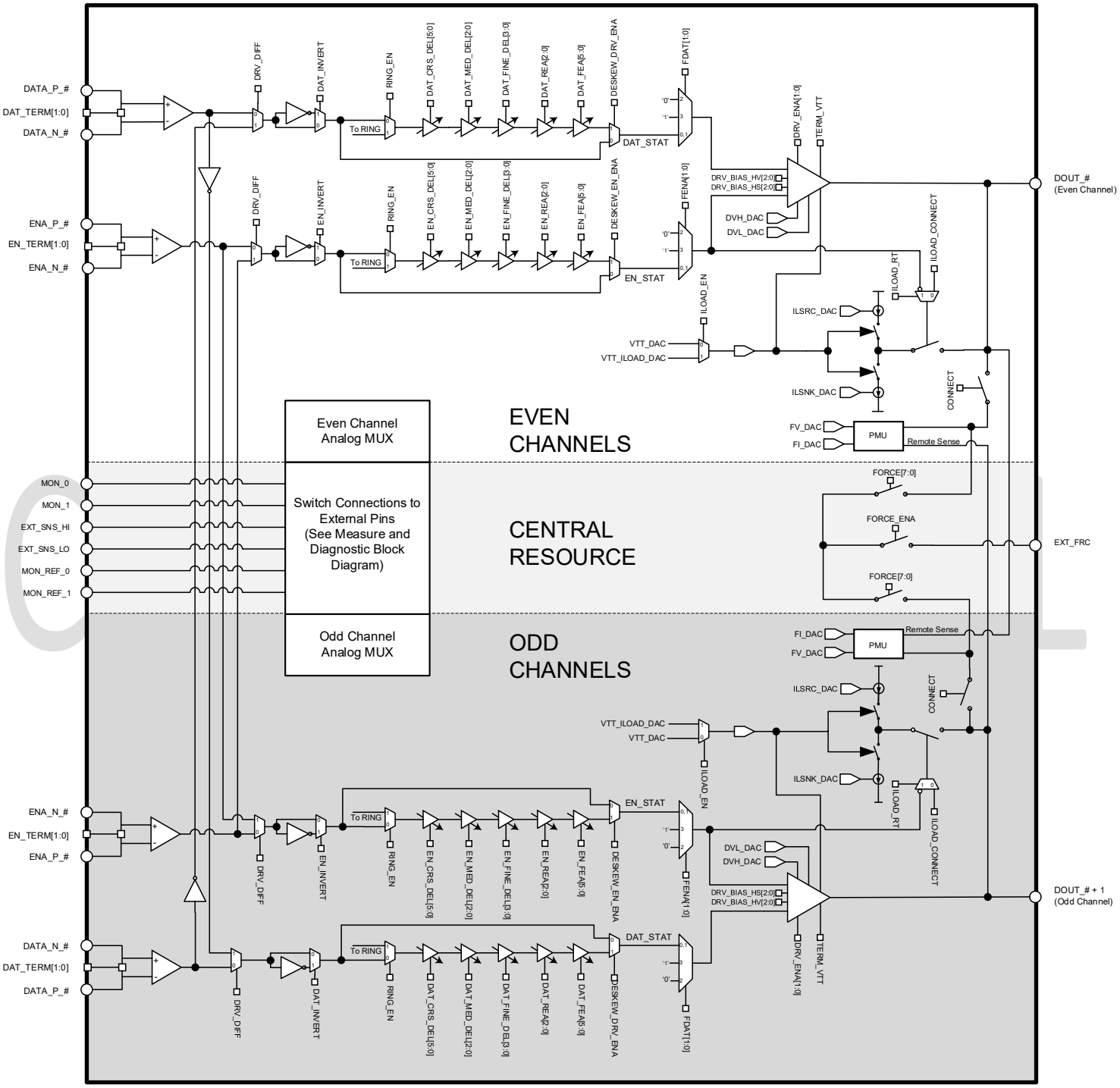


FIGURE 17: DRIVER/LOAD BLOCK DIAGRAM

Comparator Block Diagram

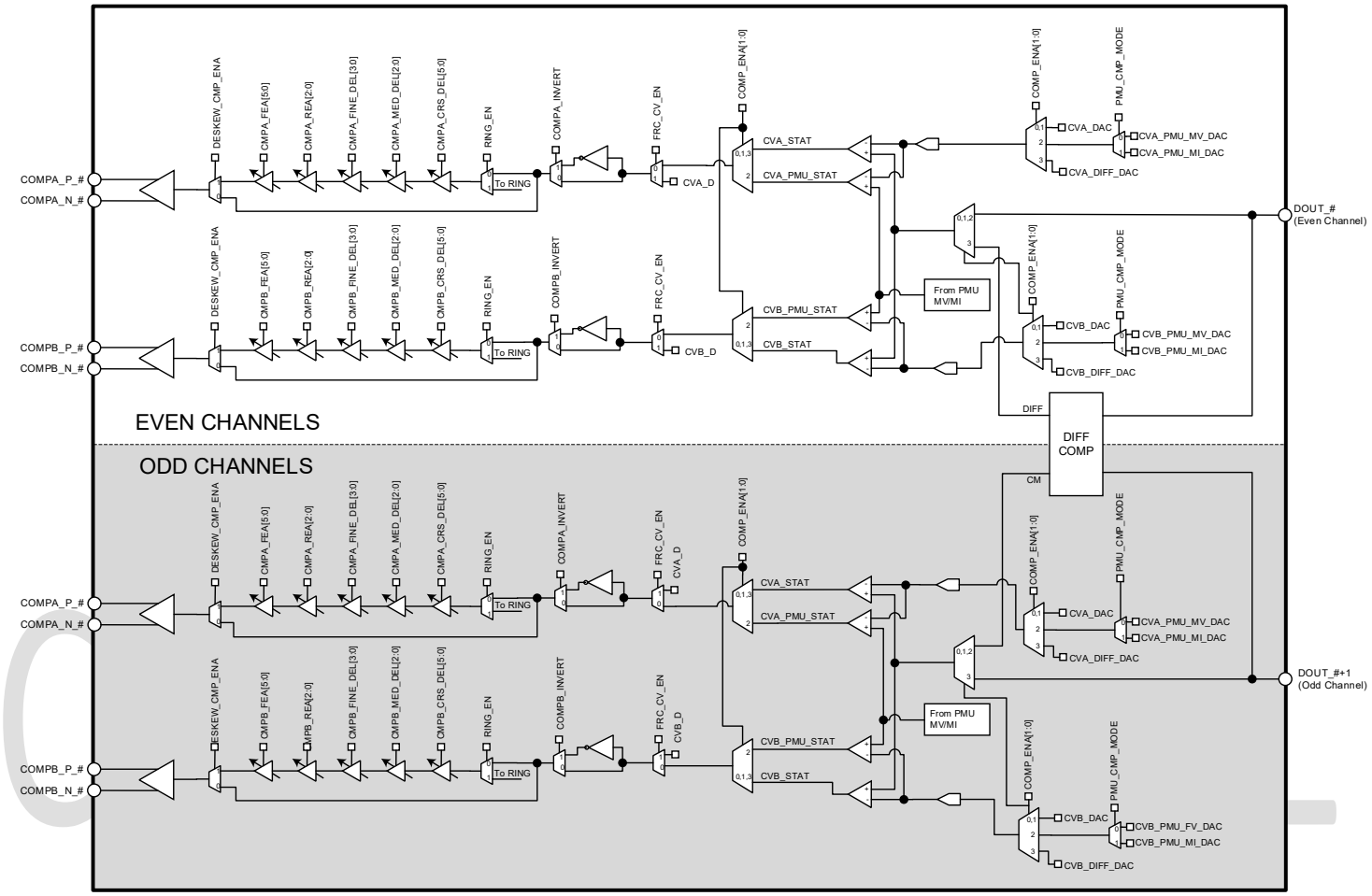


FIGURE 18: COMPARATOR BLOCK DIAGRAM

PPMU Block Diagram

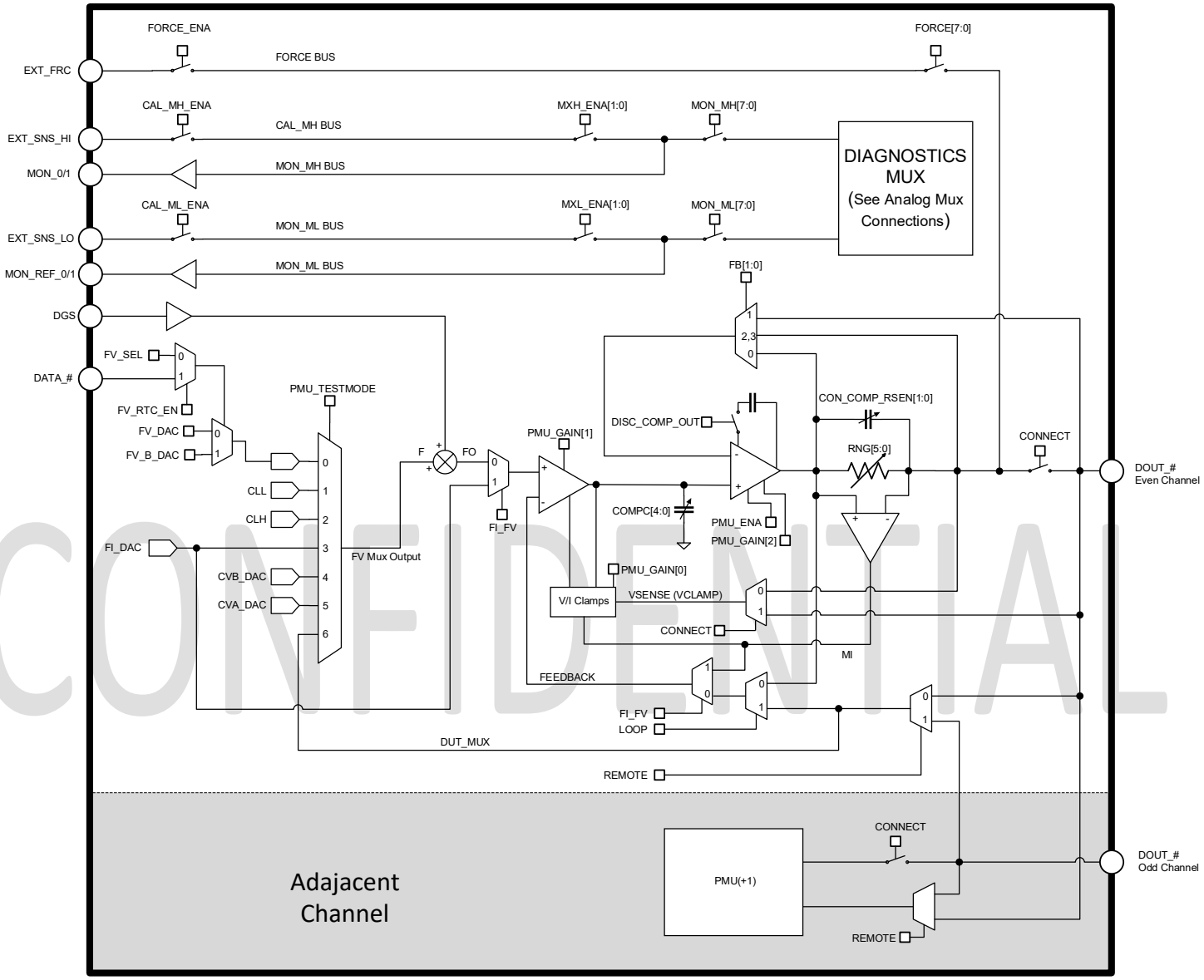


FIGURE 19: PMU BLOCK DIAGRAM

Measure and Diagnostic Block Diagram

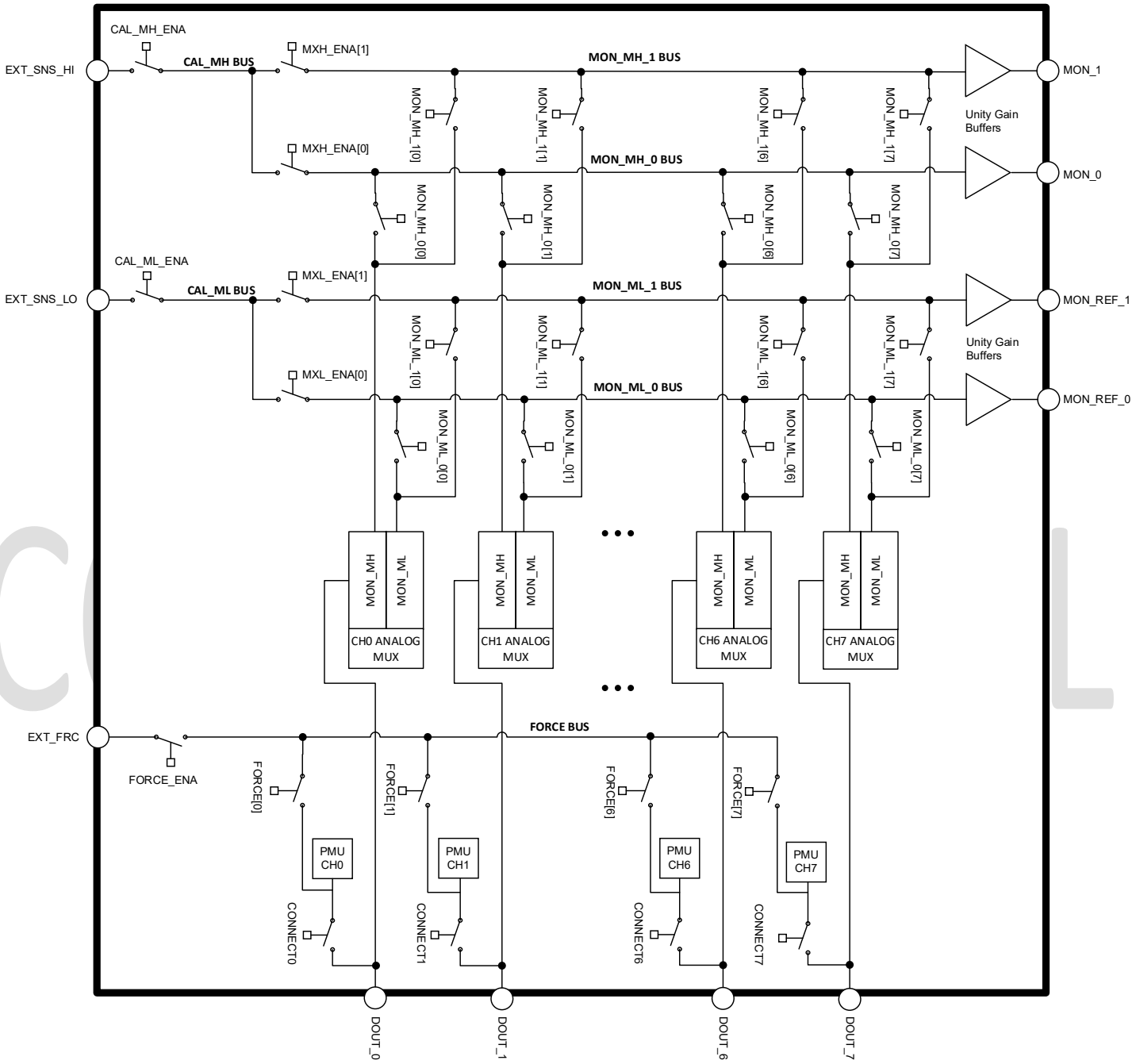


FIGURE 20: MEASURE AND DIAGNOSTIC MUX DIAGRAM

Alarm Block Diagram

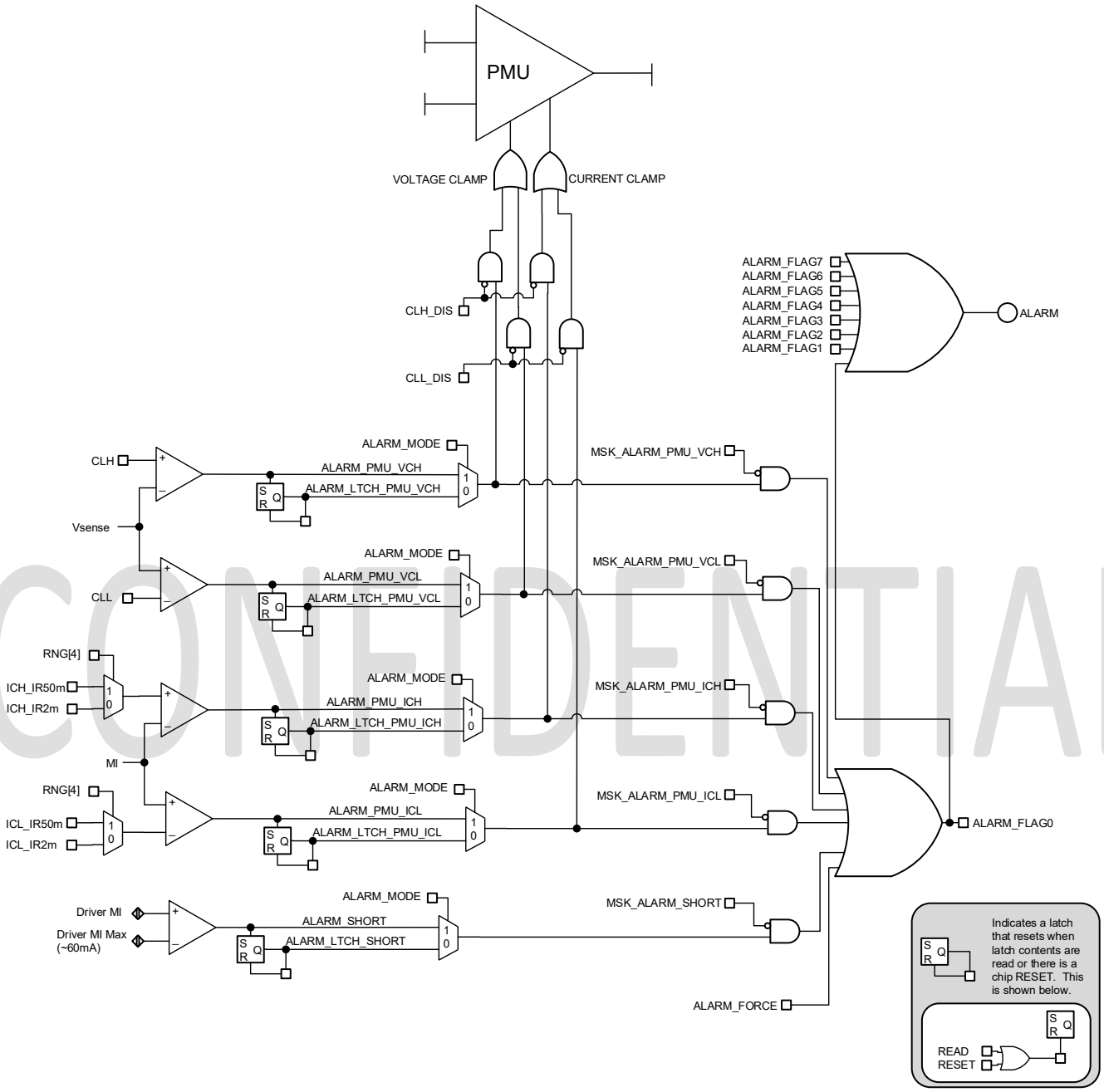


FIGURE 21: ALARMS

Real-time Digital Inputs

Each channel has real-time digital inputs, DATA and ENA, which control the real-time operation of the driver. Universal Inputs DATA_P_#/DATA_N_# and ENA_P_#/ENA_N_# are differential inputs that directly accept most standard technologies which operate between VDD (+1.8V) and ground, without requiring any external translation. The DATA and ENA inputs are optimized for LVDS inputs.

On-Chip Terminations

Each channel's DATA and ENA inputs have independent on-chip termination options which support three different termination schemes:

- No termination (open circuit)
- 100Ω across the differential input
- 50Ω single-ended termination

These termination schemes may be realized without requiring any external resistors. Access and control of these termination resistors is accomplished via the SPI port, through which the individual enable bits can be set or cleared.

TABLE 28: ON-CHIP TERMINATIONS

DAT_TERM [1:0] EN_TERM [1:0]	INPUT TERMINATION
00	No Termination
01	100Ω Differential
10	100Ω Differential
11	50Ω Single-Ended

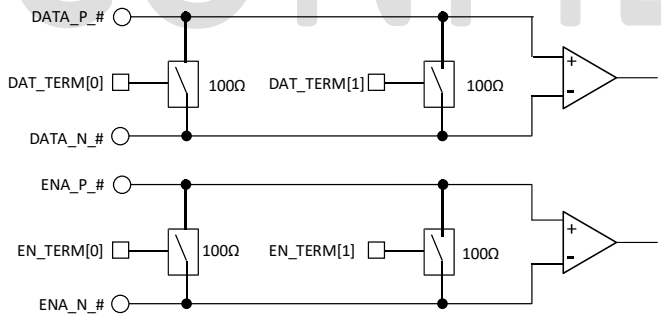


FIGURE 22: ON-CHIP TERMINATION FOR DATA AND ENABLE

50Ω Single-Ended Termination

Selecting this option creates a single-ended 50Ω termination. The inverting input then becomes the termination voltage for the input signal and the appropriate termination voltage level must be applied to this pin. Vterm must be able to handle any current flow required for proper termination.

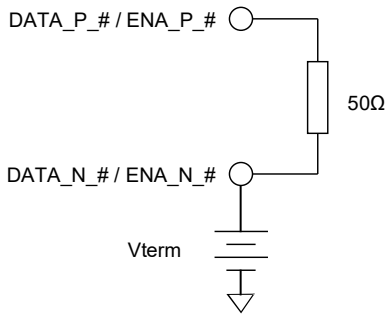


FIGURE 23: SINGLE ENDED TERMINATION

100Ω Differential Termination

By selecting this option, a 100Ω resistance is connected between the differential inputs, thus cleanly terminating differential inputs connected by 50Ω transmission lines on the PCB.

Digital Signal Processing Options

Deskew

Each channel's high-speed DATA, ENA, COMPA and COMPB inputs have timing adjustment capability with the following characteristics:

- Separate and independent delay circuitry for the DATA, ENA, COMPA, and COMPB paths.
- Separate and independent delay circuitry for all channels.
- Propagation delay adjust (both rising (Tpd+) and falling (Tpd−) edge are delayed equally).
- Falling edge adjust (FEA) (falling edge may be adjusted, rising edge Tpd remains constant).
- Rising edge adjust (REA) (rising edge may be adjusted, falling edge Tpd remains constant).
- Delay elements can be bypassed to reduce power consumption.

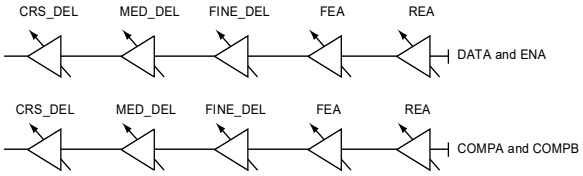


FIGURE 24: DRIVER AND COMPARATOR DESKEW

Deskew Temperature Compensation

The on-chip deskews have circuitry controlled by register bits which help negate the effects of temperature change on the performance of the deskew elements. There are two sets of registers which are used to perform this function.

- The first register is stored in FUSE memory on chip. The Deskew Temperature Compensation is calibrated during ATE test and the calibration values are burned into FUSE memory. These values can be used with no further input from the user. By default, the calibrated values from ATE test will be used for deskew temperature calibration. This value cannot be read but will automatically be used following a reset of the chip.
- The second register for deskew temperature compensation is located within the normal channel registers. This register can be accessed using the SPI port and is shown in Table 29.

TABLE 29: DESKEW TEMPCO

DSKW_TEMPCO [4:0]	AMOUNT OF TEMPERATURE COMPENSATION
00000	Negative Temperature compensation
10000	No Temperature compensation
11111	Positive Temperature Compensation

The selection on whether to use the calibrated value stored in fuse memory or override the compensation with the value in the DSKW_TEMPCO [4:0] register is made using the DSK_TEMPCO_FUSE_OVRD bit.

TABLE 30: DESKEW TEMPCO OVERRIDE

DSKW_TEMPCO_FUSE_OVRD	DESKEW TEMPERATURE COMPENSATION VALUES TO USE
0	FUSE Memory
1	DSKW_TEMPCO [4:0]

While the DSKW_TEMPCO_FUSE_OVRD bit is set to ‘0’, writing any value to the DSKW_TEMPCO [4:0] register will have no effect on the deskew temperature compensation. The DSKW_TEMPCO [4:0] register can be read or written to whether the DSK_TEMPCO_FUSE_OVRD bit is set to ‘0’ or ‘1’.

During ATE test the best Deskew Temperature Compensation value for all 8 channels is measured and then averaged. This one averaged value is then burned into Fuse Memory. The deskew calibration compensation factors burned into fuse memory are expected to meet the needs of most applications.

Propagation Delay Adjust

The propagation delay circuitry adds timing delay to the rising edge (Tpd+) and the falling edge (Tpd–) in equal amounts.

Propagation delay adjustment is typically used for aligning the timing of multiple channels inside a tester.

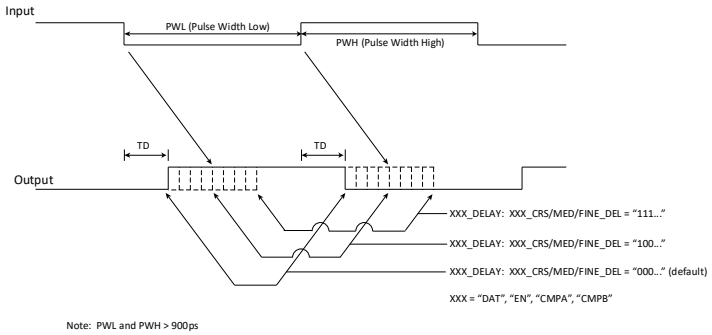


FIGURE 25: PROPAGATION DELAY ADJUST

The propagation delay circuitry is divided into three separate blocks:

- Coarse Delay (CRS_DEL)
- Medium Delay (MED_DEL)
- Fine Delay (FINE_DEL)

Coarse Delay (CRS_DEL)

Coarse delay divides the overall delay range into equal segments and then selects one of those delays. Coarse delay has a 6-bit control.

- Tspan (CRS_DEL) = ~12ns
- Resolution = ~700ps
- “000000” = min delay,
- “100111” = max delay,
- “100111” = codes not allowed above this value

There are 4 sets of coarse delay deskew paths on chip.

- DAT_CRS_DEL [5:0]: Delay for driver path deskew.
- EN_CRS_DEL [5:0]: Delay for enable path deskew.
- CMPA_CRS_DEL [5:0]: Delay for COMPA path deskew.
- CMPB_CRS_DEL [5:0]: Delay for COMPB path deskew.

Medium Delay (MED_DEL)

Medium Delay allows edge placement between coarse delay LSB steps. Medium delay has a 3-bit control.

- Tspan (MED_DEL) = ~1050ps
- Resolution = ~150ps
- “000” = min delay, “111” = max delay

There are 4 sets of medium delay deskew paths on chip.

- DAT_MED_DEL [2:0]: Delay for driver path deskew.
- EN_ MED _DEL [2:0]: Delay for enable path deskew.
- CMPA_ MED_DEL [2:0]: Delay for COMPA path deskew.
- CMPB_ MED_DEL [2:0]: Delay for COMPB path deskew.

Fine Delay (FINE_DEL)

Fine delay adjust makes very small corrections to Tpd+ and Tpd– and affects both rising and falling edges equally. Fine Delay allows edge placement between medium delay LSB steps. Fine delay has a 4-bit control.

- Tspan (FINE_DEL) = ~270ps
- Resolution = ~18ps
- “0000” = min delay, “1111” = max delay

There are 4 sets of fine delay deskew paths on chip.

- DAT_FINE_DEL [3:0]: Delay for driver path deskew.
- EN_ FINE _DEL [3:0]: Delay for enable path deskew.
- CMPA_ FINE_DEL [3:0]: Delay for COMPA path deskew.
- CMPB_ FINE_DEL [3:0]: Delay for COMPB path deskew.

Falling Edge Adjust (FEA)

The falling edge delay circuitry adds or subtracts timing delay to or from the falling edge (Tpd–) while having no effect on the rising edge (Tpd+). Falling edge adjustment is typically used for removing any pulse width distortion inside a tester.

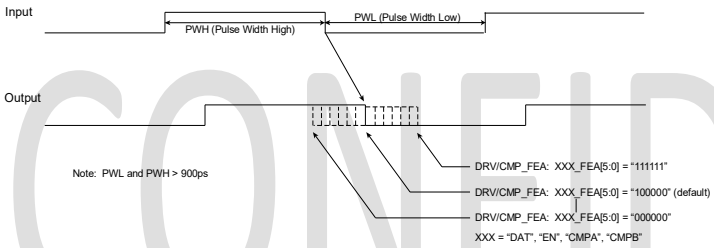


FIGURE 26: FALLING EDGE ADJUST

FEA offers a range of falling edge adjustments as selected by the SPI port. FEA has a 6-bit control.

- Tspan (FEA) 500 ps from –250ps to 250ps
- Resolution = ~15ps
- “010100” = min FEA, “111111” = max FEA

FEA code values below 20 can be non-monotonic.

There are 4 sets of falling edge adjust deskew paths on chip.

- DAT_FEA [5:0]: Delay for driver path deskew.
- EN_FEA [5:0]: Delay for enable path deskew.
- CMPA_FEA [5:0] Delay for COMPA path deskew.
- CMPB_FEA [5:0]: Delay for COMPB path deskew.

Rising Edge Adjust (REA)

The rising edge delay circuitry adds or subtracts timing delay to or from the rising edge (Tpd+) while having no effect on the falling edge (Tpd–). Edge adjustment is typically used for removing any pulse width distortion inside a tester.

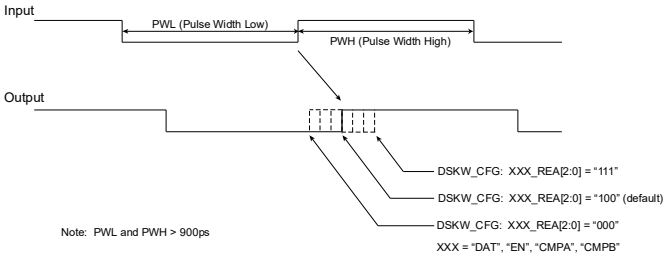


FIGURE 27: RISING EDGE ADJUST

REA offers a range of rising edge adjustments as selected by the SPI port. REA has a 3-bit control.

- Tspan (REA) 500 ps from –250ps to 250ps
- Resolution = ~80ps.
- “000” = min REA, “111” = max REA.

There are 4 sets of rising edge adjust deskew paths on chip.

- DAT_REA [2:0]: Delay for driver path deskew.
- EN_REA [2:0]: Delay for enable path deskew.
- CMPA_REA [2:0]: Delay for COMPA path deskew.
- CMPB_REA [2:0]: Delay for COMPB path deskew.

Bypass Mode

All digital processing and deskew options may be bypassed completely by having DATA, ENA, and CMP paths have direct control over the output. Bypass mode results in the shortest Tpd across the chip and is useful in applications where the digital features and channel deskew are performed in an external IC.

- DESKEW_DRV_ENA: Power up enable for the drive path deskew.
- DESKEW_EN_ENA: Power up enable for the enable path deskew.
- DESKEW_CMP_ENA: Power up enable for the comparator path deskew.

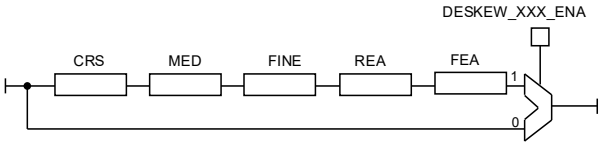


FIGURE 28: DESKEW ENABLE

TABLE 31: BYPASS MODE

DESKEW_DRV_ENA, DESKEW_ENA_ENA, DESKEW_CMP_ENA	DESKEW
1	Deskew Elements Included in the Signal Path
0	Deskew Elements Bypassed and Deskew Elements placed in a lower power standby mode.

Driver Output Modes

There are 2 driver output modes:

Driver High Speed Mode (HS). The HS driver produces an output that has a constant rise time. The rise/fall time is independent of amplitude. The HS driver can swing across a range of 0V to +4V.

Driver High Voltage Mode (HV). The HV driver is slew rate controlled. The slew rate control is via a DAC setting in the channel registers using the SPI port and produces an output that has constant slew rate over a range of settings. The HV driver can swing across a range of –2V to +6V. The slew rate control is discussed later in this datasheet and uses the SLEW_HV_N and SLEW_HV_P registers.

TABLE 32: DRIVER OUTPUT MODE

DRV_ENA [1:0]	MODE
00	Reduced power standby state (both driver modes disabled)
01	HS Driver mode enabled
10	HV Driver Mode enabled
11	Reduced power standby state (both driver modes disabled)

Driver Output Control

The driver has a nominal 50Ω output impedance when not in Hi-Z and supports four output states:

- High level (DVH)
- Low level (DVL)
- Termination voltage (VTT)
- High impedance (Hi-Z)

Data and Enable Sources

There are multiple sources for the driver data and enable inputs:

- Real time data and enable input pins
- Differential data and enable signals
- SPI port control

SPI Port Control

The SPI port can take control over the driver DATA and ENA signals and override any real-time inputs.

TABLE 33: FDAT

FDAT [1:0]	DATA PATH
0X	Real-time inputs from DAT pins
10	Force Data “0”
11	Force Data “1”

TABLE 34: FENA

FENA [1:0]	ENABLE PATH
0X	Real-time inputs from EN pins
10	Disable Driver
11	Enable Driver

Internal Driver State Readback

The internal nodes DAT_STAT and EN_STAT may be read back via the SPI Port. These bits are read only.

- EN_STAT: Internal state of the driver enable at the ENA pins.
- DAT_STAT: Internal state of the driver data at the DATA pins.

Driver Termination and Hi-Z Mode

When disabled, the driver can either assume one of two modes which are determined by the TERM_VTT bit. The driver can be disabled by using the real-time ENA_P_#/ENA_N_# inputs or via the SPI port. This is shown in the Driver Termination Table 35.

TABLE 35: DRIVER TERMINATION

TERM_VTT	DRIVER ENABLE	DRIVER OUTPUT
0	0	Hi-Z Mode
1	0	VTT Mode. Driver terminated through 50Ω to a programmed voltage value on VTT

TABLE 36: DRIVER TRUTH TABLE

	DRV_EN [1:0]	TERM_VTT	FENA [1:0]	FDAT [1:0]	Real Time Data	Real Time Enable	Driver State	Driver Output
Driver Standby	00	X	XX	XX	X	X	Disabled	Hi-Z
	11	X	XX	XX	X	X	Disabled	Hi-Z
Driver HS Mode	01	0	0X	00	X	0	Disabled	Hi-Z
	01	X	0X	00	1	1	Enabled	DVH
	01	X	0X	00	0	1	Enabled	DVL
	01	1	0X	00	X	0	Enabled	VTT
	01	0	10	XX	X	X	Disabled	Hi-Z
	01	1	10	XX	X	X	Enabled	VTT
	01	0	11	00	1	X	Enabled	DVH
	01	0	11	00	0	X	Enabled	DVL
	01	0	11	10	X	X	Enabled	DVL
	01	0	11	11	X	X	Enabled	DVH
	01	0	0X	XX	X	0	Disabled	Hi-Z
	01	0	0X	10	X	1	Enabled	DVL
	01	0	0X	11	X	1	Enabled	DVH
Driver HV Mode	10	0	0X	00	X	0	Disabled	Hi-Z
	10	X	0X	00	1	1	Enabled	DVH
	10	X	0X	00	0	1	Enabled	DVL
	10	1	0X	00	X	0	Enabled	VTT
	10	0	10	XX	X	X	Disabled	Hi-Z
	10	1	10	XX	X	X	Enabled	VTT
	10	0	11	00	1	X	Enabled	DVH
	10	0	11	00	0	X	Enabled	DVL
	10	0	11	10	X	X	Enabled	DVL
	10	0	11	11	X	X	Enabled	DVH
	10	0	0X	XX	X	0	Disabled	Hi-Z
	10	0	0X	10	X	1	Enabled	DVL
	10	0	0X	11	X	1	Enabled	DVH

Differential Driver Mode

Adjacent channels may be combined into one differential channel using the DRV_DIFF register bit. Adjacent channels are grouped in the following pairs: 0/1, 2/3, 4/5, 6/7. The adjacent channels are grouped for both the Data and Enable paths. This mode produces complementary DATA outputs on adjacent channels.

Either channel of the pair may be selected to control the differential data and enable paths. Set the DRV_DIFF bit as follows:

1. DRV_DIFF = "0" for Master Channel.
2. DRV_DIFF = "1" for Slave Channel. For the DATA path, this channel will take the inverted data from the Master Channel. The ENABLE path uses the same signal for both the Master and Slave channels.

TABLE 37: DIFFERENTIAL DRIVER

DRV_DIFF	DIFFERENTIAL DRIVER PATH
0	Master Channel in differential driver mode. (This mode is also used for normal single ended driver mode)
1	Slave Channel. This enables differential driver mode

Driver Data and Enable Inversion

The SPI port can invert the polarity of the DATA and ENABLE signals. This inversion is useful to allow one single DATA input to drive adjacent channels to the same logic level.

TABLE 38: DAT_INVERT/EN_INVERT

DAT_INVERT EN_INVERT	SIGNAL
0	True signal
1	Inverted signal

High Voltage Driver Slew Rate Adjust

The HV driver has independent adjustments for the rising and falling edge slew rates via the SPI port.

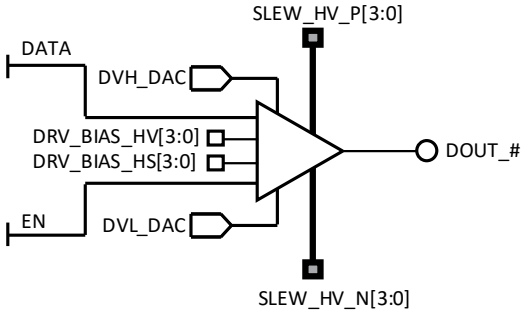


FIGURE 29: SLEW AND BIAS CONTROL

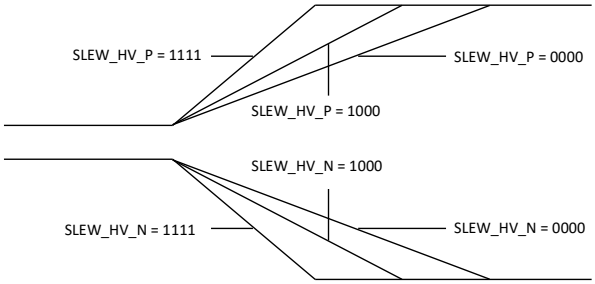


FIGURE 30: SLEW RATE ADJUST

TABLE 39: DRIVER SLEW RATE

SLEW_HV_P [3:0] SLEW_HV_N [3:0]	DRIVER SLEW RATE
0000	Minimum Slew Rate
•	•
1000	Recommended Slew Rate Setting
•	•
1111	Maximum Slew Rate

Driver Bias

The HV and HS driver output stages have a programmable bias current to allow applications that require slower edge rates to consume less power.

- DRV_BIAS_HV: Sets High Voltage Driver Bias Current
- DRV_BIAS_HS: Sets High Speed Driver Bias Current

TABLE 40: DRIVER BIAS

DRV_BIAS_HV [3:0] DRV_BIAS_HS [3:0]	DRIVER BIAS
0000	Minimum Driver Bias
•	•
1000	Recommended Driver Bias Setting
•	•
1111	Maximum Driver Bias

Driver Bias and Slew Rate Settings

The bias settings have a significant impact on rise and fall time when operating at maximum slew rate.

The bias settings will also impact the output impedance and driver levels. Therefore, bias settings should be chosen prior to calibrating Rout and calibrating all driver levels.

Driver Pre-Emphasis

A Pre-Emphasis circuit in the driver aids to overcome and compensate for primarily on-chip parasitic effects. At maximum setting there may be some peaking observable at the output that could help compensate for line loss. This peaking can help compensate for roll off due to capacitive loads at the end of the transmission line. The compensation circuit is only applied to the High-Speed Driver.

TABLE 41: DRIVER PRE-EMPHASIS

HS_PRE [3:0]	PRE-EMPHASIS
0000	Minimum Pre-Emphasis
1111	Maximum Pre-Emphasis

Adjustable Output Impedance

The HS and HV drivers are designed to maintain constant output impedance regardless of changes due to:

- Ambient Temperature
- Part to Part variation

Nominal ROUT (Output Impedance) for the HS and HV drivers is 50Ω.

Output Impedance Adjustments

The driver output has circuitry controlled by the SPI port that can set the output impedance of the driver to 50Ω. There are two sets of registers that perform this function.

- The first set of registers are stored in FUSE memory on chip. The output impedance registers are calibrated during ATE test and the calibration values are burned into FUSE memory and can be used with no further input from the user. By default, the calibrated values from the ATE test will be used for the output impedance calibration values. These values can be read and will automatically be used following a reset of the chip. Refer to the FUSE section of this datasheet for information on reading the calibrated values.
- The second set of registers for output impedance adjustments are stored in the normal channel registers. These registers can be accessed using the SPI port and are shown in Table 42 and explained here:
- It is possible to make fine adjustments to the driver ROUT for sourcing and sinking resistances. These adjustments are accomplished through independent registers. The ROUT has an adjustment range that can move the impedance slightly up and down and is guaranteed to calibrate to 50Ω. This can be used to accommodate transmission line impedance errors on a PCB board, as well as to adjust a characteristic in a waveform's performance.
- RO_SRC_HS [3:0]: HS Driver output sourcing resistance.
- RO_SRC_HV [3:0]: HV Driver output sourcing resistance.
- RO_SINK_HS [3:0]: HS Driver output sinking resistance.
- RO_SINK_HV [3:0]: HV Driver output sinking resistance.

TABLE 42: ROUT ADJUSTMENT

RO_SRC_HV [3:0] RO_SINK_HV [3:0] RO_SRC_HS [3:0] RO_SINK_HS [3:0]	ROUT ADJUSTMENT
0000	Maximum ROUT
•	•
0111	Nominal ROUT
•	•
1111	Minimum ROUT

The selection on whether to use the calibrated values stored in FUSE memory or override the output impedance adjustment values in the channel registers is made using the RO_SRC_SNK_FUSE_OVRD bit.

TABLE 43: DRIVER OUTPUT IMPEDANCE OVERRIDE

RO_SRC_SNK_FUSE_OVRD	DRIVER OUTPUT IMPEDANCE VALUES TO USE
0	Fuse Memory
1	RO_SRC_HV [3:0] RO_SINK_HV [3:0] RO_SRC_HS [3:0] RO_SINK_HS [3:0]

While the RO_SRC_SNK_FUSE_OVRD bit is set to '0', writing any value to the RO_SRC_HV, RO_SINK_HV, RO_SRC_HS, and RO_SINK_HS registers will have no effect on the driver output impedance. The RO_SRC_HV, RO_SINK_HV, RO_SRC_HS, and RO_SINK_HS registers can be read whether the RO_SRC_SNK_FUSE_OVRD bit is set to '0' or '1'.

Ring Oscillator Mode

Each channel may be placed into a ring oscillator mode configuration where the DAT, COMPA, COMPB, and ENA paths are fed back to each other to form a loop. This loop is primarily used for test and characterization of the deskew paths, and it may also be used for calibrating each of the deskew elements. The frequency of two or more generated signals with different settings can be measured and compared to observe the deskew vernier linearity and resolution. The deskew elements for DAT, COMPA, COMPB, and ENA paths must all be enabled while in ring oscillator mode.

Ring Oscillator Mode - Enable

The ring oscillator function is enabled using the RING_EN register bit.

TABLE 44: RING_EN DATA/ENABLE PATH

RING_EN	DATA PATH SOURCE ENABLE PATH SOURCE
0	DATA_P_#/DATA_N_#, ENA_P_#/ENA_N_#
1	RING_#

TABLE 45: RING_EN COMPARATOR PATH

RING_EN	COMPARATOR PATH
0	COMPA_P_#/ COMPA_N_#, COMPB_P_#/COMPB_N_#
1	RING_#

Ring Oscillator – Start Up

The ring starts up by the SPI port executing a RING_PULSE transaction. This write-only function fires off a one-shot pulse that initiates the ring oscillation. In most cases however, the RING_PULSE is not needed, and the ring oscillator will start when the part is configured in the ring oscillator mode.

Only one SPI transaction is needed to start-up the ring oscillator. The deskew path for the DATA, COMPA, COMPB, and ENA paths must all be enabled while in Ring Oscillator Mode.

Ring Oscillator Mode:

- Select Drive Mode (HS or HV)
- Set DVH and DVL to desired levels
- DESKEW_DRV_ENA = 1
- DESKEW_CMP_ENA = 1
- DESKEW_EN_ENA = 1
- FENA [1:0] = 0 (The FENA mux is bypassed in the ring oscillator configuration. When RING_EN = 1. The Driver is automatically enabled.)
- FDAT [1:0] = 0
- RING_EN = 1
- RING_PULSE = 1 (Usually not necessary)

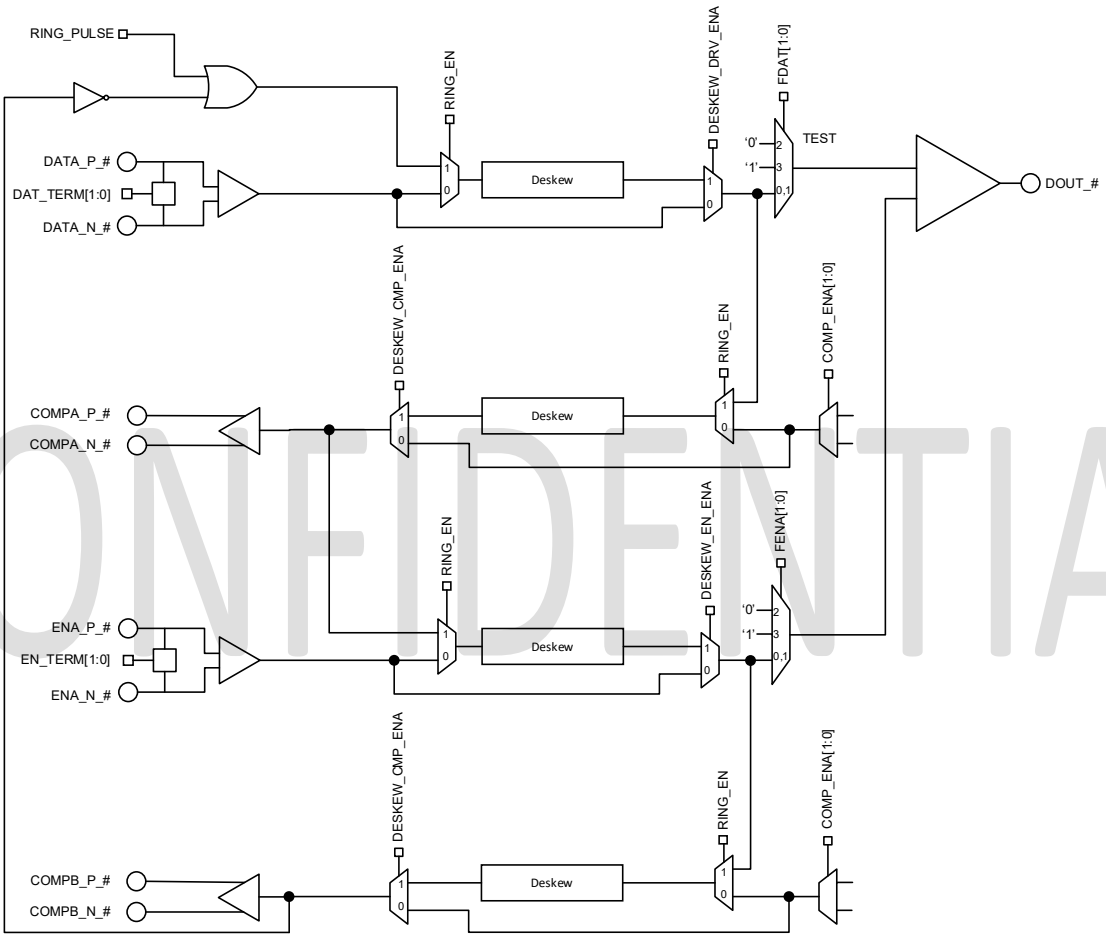


FIGURE 31: RING OSCILLATOR

Active Load

The active load consists of source and sink current sources, and a commutation buffer. The circuitry emulates an actual diode bridge but is built with current mirrors and steering circuitry. Each channel's active load may:

- Switch between 2 active load ranges (24mA and 1mA)
- Source up to 24mA
- Sink up to 24mA
- Be placed in a high impedance state

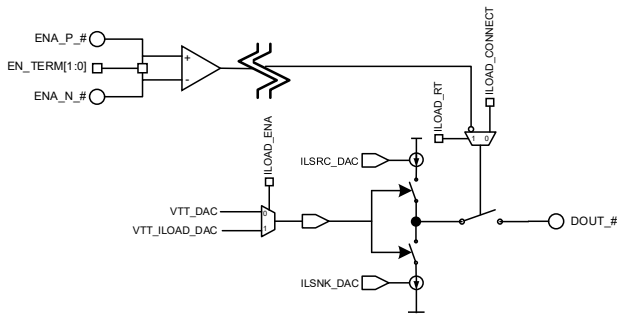


FIGURE 32: ACTIVE LOAD

Commutating Voltage

The active load commutating buffer and the VTT termination functions are mutually exclusive in that the SPI port sets up which resource is active when the driver goes into HiZ.

The on-chip DC level VTT_ILOAD is used to set the commutating voltage of the active load.

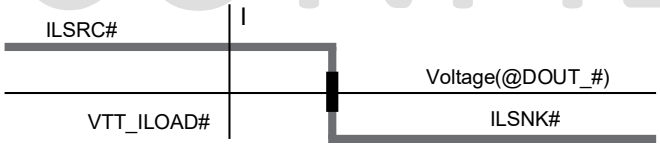


FIGURE 33: COMMUTATING VOLTAGE

The programmed ILSRC# current loads the device under test when (V-DOUT < VTT_ILOAD). The programmed ILSNK# current loads the device under test when: (V-DOUT > VTT_ILOAD).

Note: V-DOUT: Voltage at the DOUT pin.

Load Enable Sources

The active load may be activated by:

- SPI port
- ENA_P_#/ENA_N_# input pins

Active Load Enable

The active load block can be powered down using the ILOAD_ENA bit. This bit powers down the ILSNK and ILSRC currents and switches the commutating voltage between VTT and VTT_ILOAD.

TABLE 46: ILOAD_ENA

ILOAD_ENA	ACTIVE LOAD BLOCK
0	Active load block powered down. VTT level selected for input to DAC
1	Active load block powered up. VTT_ILOAD level selected for input to DAC

TABLE 47: ACTIVE LOAD ENABLE

EN	ILOAD_RT	ILOAD_CONNECT	ILOAD_ENA	CHANNEL ACTIVE LOAD
X	X	X	0	HiZ
1	1	X	1	HiZ
0	1	X	1	Active
X	0	1	1	Active
X	0	0	1	HiZ

Source and Sink Currents

The source and sink current levels are independent and supplied by on-chip programmable current sources and may be programmed to different values.

The active load has the ability to switch between 2 active load current ranges using the ILOAD_RANGE [4:0] bits: 1mA and 24mA.

TABLE 48: ACTIVE LOAD RANGE

ILOAD_RANGE [4:0]	ACTIVE LOAD RANGE
0	24mA Range
1	1mA Range

TABLE 49: ILSRC_DAC REGISTER

ILSRC_DAC [15:0]	ILOAD_RANGE = 0 SOURCE CURRENT	ILOAD_RANGE = 1 SOURCE CURRENT
0000 Hex	0mA	0mA
FFFF Hex	24mA	1mA

TABLE 50: ILSNK_DAC REGISTER

ILSNK_DAC [15:0]	ILOAD_RANGE = 0 SINK CURRENT	ILOAD_RANGE = 1 SINK CURRENT
0000 Hex	0mA	0mA
FFFF Hex	24mA	1mA

The active load contains compensation for stability. There are 5 bits of compensation for the active load loop.

TABLE 51: ACTIVE LOAD COMPENSATION

ILOAD_COMP_MODE[4:0] (Bits[4:1] = Unused)	COMPENSATION
0	Default Compensation. Recommended for most use cases.
1	Use Register ILOAD_COMP[4:0] register bits listed in Table 52 for compensation settings.

TABLE 52: ACTIVE LOAD COMPENSATION SETTINGS

ILOAD_COMP[4:0]	ACTIVE LOAD COMPENSATION SETTINGS
0x00	Minimum Compensation.
0x1F	Maximum Compensation.

Comparator Overview

Each channel supports two sets of differential comparator output signals, COMPA_P_#/COMPA_N_# and COMPB_P_#/ COMPB_N_#, that may be driven by a variety of signal sources:

- Functional comparators
- PMU comparators
- SPI port
- Differential common-mode comparators
- Differential differential-mode comparators

Threshold Generation

The following per channel comparator threshold reference levels are independent on-chip DC levels programmed through the SPI port.

- CVA_DAC, CVB_DAC
- CVA_PMU_MV_ DAC, CVB_PMU_MV_ DAC
- CVA_PMU_MI_ DAC, CVB_PMU_MI_ DAC
- CVA_DIFF_ DAC, CVB_DIFF_ DAC

Internal State Readback

The internal nodes CVA_STAT, CVB_STAT, CVA_PMU_STAT, and CVB_PMU_STAT may be read back via the SPI port.

TABLE 53: COMPARATOR READBACK REGISTERS

COMPARATOR READBACK REGISTER	DESCRIPTION
CVA_STAT	State of Comparator A Output (Single Ended or Differential: Depends on state of COMP_ENA [1:0])
CVB_STAT	State of Comparator B Output (Single Ended or Differential: Depends on state of COMP_ENA [1:0])
CVA_PMU_STAT	State of PPMU Comparator A
CVB_PMU_STAT	State of PPMU Comparator B

Comparator Inversion

The SPI port can invert the polarity of the comparator signal.

TABLE 54: COMPARATOR INVERSION

COMPA_INVERT COMPB_INVERT	COMPARATOR SIGNAL
0	True Comparator Signal
1	Inverted Comparator Signal

Comparator Source Selection

The SPI port defines the comparator operating mode.

TABLE 55: COMPARATOR SOURCE SELECTION

COMP_ENA [1:0]	REAL-TIME WINDOW COMPARATOR
00	All comparators disabled
01	Single-ended compare
10	PPMU compare enabled
11	Differential compare enabled

All Comparators Disabled

The SPI port can disable the comparators to save power in applications where the window comparators are not used. When the real-time comparators are powered down, the SPI port must be selected as the comparator signal path source (FRC_CV_EN=1) in order for the comparator outputs to be in a defined state. Disable the comparators using the following setting: COMP_ENA [1:0]='00'.

Single Ended Compare

The single-ended functional comparator is a high-speed window comparator with extremely low input leakage current when DOUT is between the power supply rails VEE and VCC. It is normally selected for real-time functional testing of the Device Under Test. DAC voltage levels CVA_DAC and CVB_DAC control the comparator thresholds. Enable single ended compare mode using the following setting COMP_ENA [1:0]='01'.

TABLE 56: COMPARATOR TRUTH TABLE

CONDITION		COMPA	COMPB
DOUT < CVA_DAC	DOUT < CVB_DAC	0	0
DOUT < CVA_DAC	DOUT > CVB_DAC	0	1
DOUT > CVA_DAC	DOUT < CVB_DAC	1	0
DOUT > CVA_DAC	DOUT > CVB_DAC	1	1

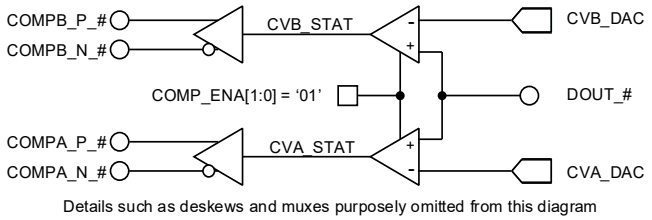


FIGURE 34: SINGLE ENDED COMPARE

PPMU Compare

The parametric measurement unit comparator is a window comparator with its input generated by the PPMU and is normally selected for parametric testing of the Device Under Test. The PPMU inputs for the comparator are generated by the PPMU MI (measure current) or the PPMU MV (measure voltage) circuitry. Enable PPMU compare mode using the following setting: COMP_ENA [1:0] = '10'.

This circuitry translates the current or voltage being sensed into an output voltage that can be compared against an upper and lower limit. This can create a 2-bit "go/no-go" window comparator test. The "go/no-go" comparator is useful for production testing when data logged values are not necessary.

When in PPMU compare mode, the PMU_CMP_MODE bit must also be set. This bit selects between MV and MI. DAC voltage levels CVA_PMU_MV, CVA_PMU_MI, CVB_PMU_MV, and CVB_PMU_MI control the PMU comparator thresholds.

TABLE 57: PPMU COMPARE MODE

PMU_CMP_MODE	COMPARE TYPE
0	Measure Voltage (MV)
1	Measure Current (MI)

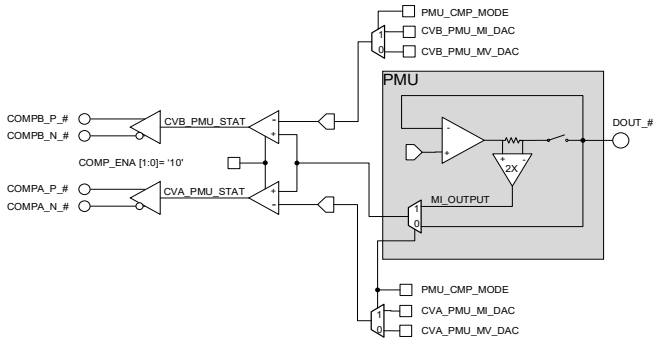


FIGURE 35: PPMU COMPARE

Differential Compare

Two adjacent channels may be combined into one differential comparator that tracks both the common mode voltage and differential voltage of the input signal:

- Common mode voltage between DOUT_#(Even) and DOUT_#(Odd): In common mode operation, the comparators track the sum of the two input signals divided by 2.
- Differential voltage between DOUT_#(Even) and DOUT_#(Odd): In differential mode operation, the comparators track the difference between the two inputs.

Common mode detection is output on the odd numbered channel and differential mode detection is output on the even numbered channel.

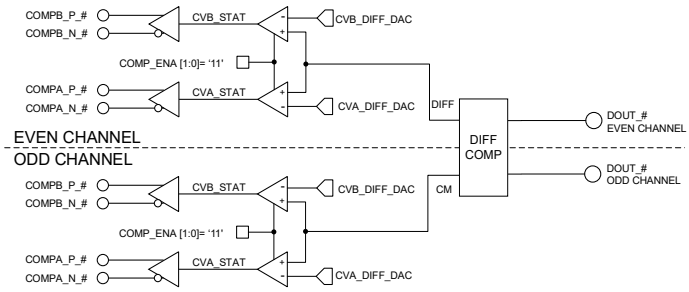


FIGURE 36: DIFFERENTIAL COMPARE

TABLE 58: DIFFERENTIAL MODE COMPARATOR

CONDITION		COMPA	COMPB
(DOUT Even – DOUT Odd) < (CVA_DIFF_DAC)	(DOUT Even – DOUT Odd) < (CVB_DIFF_DAC)	0	0
(DOUT Even – DOUT Odd) < (CVA_DIFF_DAC)	(DOUT Even – DOUT Odd) > (CVB_DIFF_DAC)	0	1
(DOUT Even – DOUT Odd) > (CVA_DIFF_DAC)	(DOUT Even – DOUT Odd) < (CVB_DIFF_DAC)	1	0
(DOUT Even – DOUT Odd) > (CVA_DIFF_DAC)	(DOUT Even – DOUT Odd) > (CVB_DIFF_DAC)	1	1

TABLE 59: COMMON MODE COMPARATORS

CONDITION		COMPA	COMPB
(DOUT Even + DOUT Odd)/2< (CVA_DIFF_DAC)	(DOUT Even + DOUT Odd < (CVB_DIFF_DAC)	0	0
(DOUT Even + DOUT Odd)/2< (CVA_DIFF_DAC)	(DOUT Even + DOUT Odd) > (CVB_DIFF_DAC)	0	1
(DOUT Even + DOUT Odd)/2> (CVA_DIFF_DAC)	(DOUT Even + DOUT Odd) < (CVB_DIFF_DAC)	1	0
(DOUT Even + DOUT Odd)/2> (CVA_DIFF_DAC)	(DOUT Even + DOUT Odd) > (CVB_DIFF_DAC)	1	1

SPI Comparator Control

The SPI port can set the Comparator A and B status and override any real-time status from the measurement unit. This SPI control allows the comparator outputs to be placed in a known state, typically for calibration, diagnostics, and debugging purposes within a tester. This is also useful when the comparator is powered down to ensure the comparator outputs are in a known state.

This override is accomplished using the FRC_CV_EN register bit. This bit forces the output value of the comparators to the values programmed into the CVA_D and CVB_D bits.

TABLE 60: FRC_CV_EN

FRC_CV_EN	COMPARATOR OUTPUT
0	Comparator operates normally and responds to normal input signals.
1	Comparator output states forced to the value stored in the CVA_D and CVB_D registers.

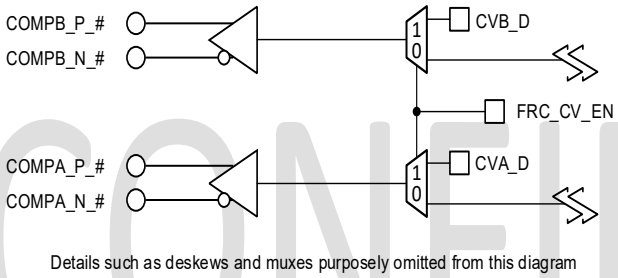


FIGURE 37: SPI COMPARATOR CONTROL

Comparator Output Stage

Each channel has CML differential output pins which can be connected to several types of interfaces. The FlexIO_LS register bits can be used to level shift the common mode output voltage to support different types of interfaces such as LVDS and CML.

TABLE 61: FLEXIO_LS UNTERMINATED

FlexIO_LS [1:0]	VOLTAGE OUTPUT DIFFERENTIAL	VOLTAGE COMMON MODE
00	0.5V	1.25
01	0.5V	1.10
10	0.5V	0.95
11	0.5V	0.80

TABLE 62: FLEXIO_LS TERMINATED TO 100Ω DIFFERENTIAL

FlexIO_LS [1:0]	VOLTAGE OUTPUT DIFFERENTIAL	VOLTAGE COMMON MODE
00	0.25V	1.25
01	0.25V	1.10
10	0.25V	0.95
11	0.25V	0.80

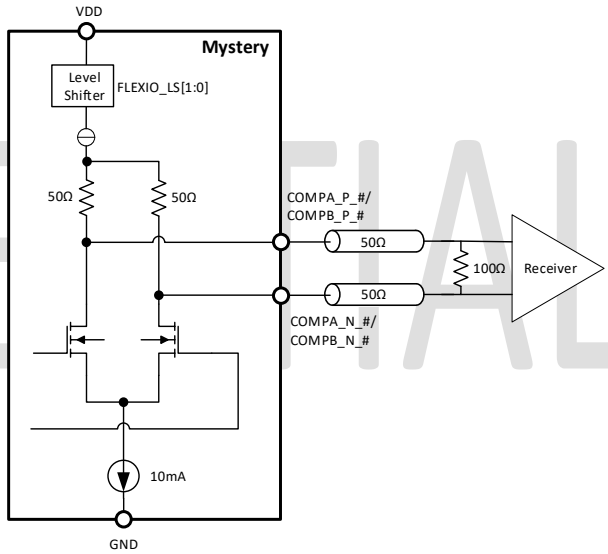


FIGURE 38: INTERFACING TO LVDS 100Ω DIFFERENTIAL

PPMU Overview

Each channel has a PPMU (Per-Pin Parametric Measurement Unit) with the ability to:

- Force Current (FI)
- Force Voltage (FV)
- Measure Current (MI)
- Measure Voltage (MV)

The current and voltage measured by the PPMU may be tested via two separate mechanisms:

- On-board PPMU window comparator (This is shown in the PPMU Compare section above).
- An analog output voltage is available on the analog test and calibration buses.

Power Saving Mode

The forcing op amp may be placed into a power saving mode.

TABLE 63: PMU_ENA

PMU_ENA	FORCING OP AMP STATUS
0	Power saving mode with reduced bandwidth and slew.
1	Active

Setting PMU_ENA to 0 reduces quiescent power consumption by lowering the PMU bias current by 75%. The PMU will continue to operate while in power saving mode, but accuracy and functionality are not guaranteed.

High Impedance

The PMU can be placed into a high impedance state using the CONNECT switch. Care should be exercised when doing this due to the large transient response possible when switching out of this mode.

TABLE 64: CONNECT

CONNECT	SWITCH
0	Open
1	Closed

TABLE 65: CONNECT RESISTANCE

SWITCH	RESISTANCE
Connect	15Ω

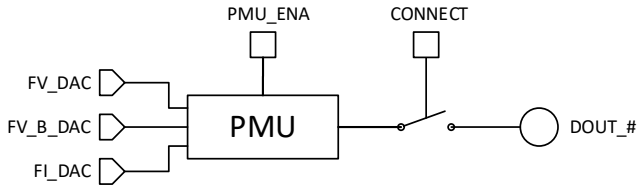


FIGURE 39: PMU ENABLE AND CONNECT

When disabled through the CONNECT switch, the PMU maintains an extremely low leakage current when DOUT remains between the two analog supply levels, VCC and VEE.

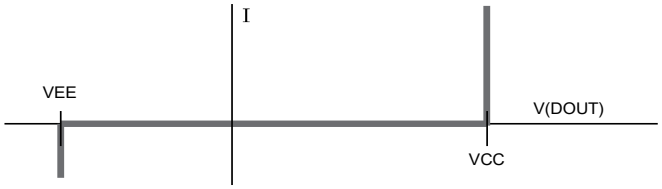


FIGURE 40: HIGH IMPEDANCE

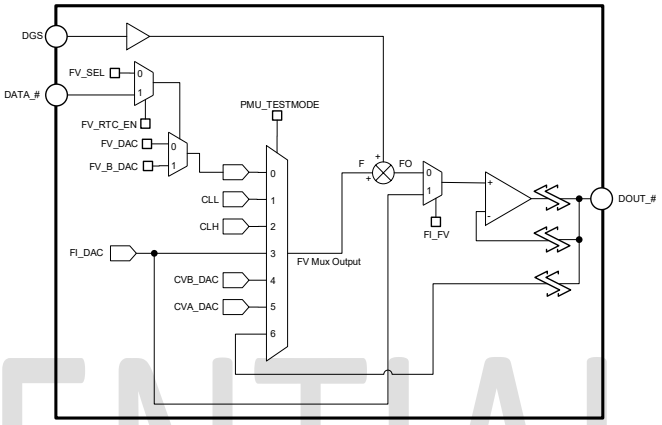


FIGURE 41: PPMU FV/FI

PPMU Operating Mode

The decision whether to force current or voltage, or to measure current or voltage, is controlled by the SPI port. There are no restrictions between Force Voltage and Force Current and Measure Voltage and Measure Current in that all combinations are legal modes.

TABLE 66: PPMU FORCE FUNCTION

FI_FV	PPMU FORCE FUNCTION
0	FV
1	FI

PMU Test Mode

The PMU may be set to a test mode that connects one of several internal DAC voltages to the PMU output. This mode is used during production tests and DAC calibration. Under most normal cases, PMU_TESTMODE should be set to '0'.

To view the raw internal DAC voltage, form the PMU_TESTMODE mux output, the MON_MH bus (see Table 100) must be selected to connect to the "FV Mux Output". Please review the Diagnostic and Monitor section of this datasheet for more detail on the MON_MH analog bus.

TABLE 67: PMU_TESTMODE

PMU_TESTMODE	FV MUX OUTPUT DAC SELECTION
0	FV_DAC
1	CCL (Voltage Clamp Low DAC)
2	CCH (Voltage Clamp High DAC)
3	FI_DAC
4	CVB _DAC
5	CVA_DAC
6	DUT_MUX*
7-15	Not Used

*DUT_mux is the output of the MUX that selects between DUT feedback and remote sense (adjacent DUT) feedback. This feedback path is not gated by the connect switch so the user can use this input to reduce glitching on connection. If the PMU is in a tight loop and disconnected with the PMU_TESTMODE mux set to DUT_MUX, the user can set the PMU up to force the same voltage is present on the DUT pin. This enables the user to be able to connect at the same voltage as the DUT.

Force Voltage (FV)

In FV mode, the voltage at DOUT is offset and will track any voltage changes on the DGS pin. The DGS pin should be connected to the ground of the device under test.

The resulting forcing voltage is FO = F + DGS. This is shown in Figure 40.

Force Voltage Input Source

The Force Voltage input to the main forcing op amp can be sourced from either the FV_DAC or FV_B_DAC register level inputs. This selection is made using the SPI port or by use of the external DATA pins. By using the DATA pins, the Force Voltage op amp can be switched between the FV_DAC and FV_B_DAC levels without writing any registers.

TABLE 68: FV_RTC_EN

FV_RTC_EN	FV_SEL	DATA	F
0	0	X	FV_DAC
0	1	X	FV_B_DAC
1	X	0	FV_DAC
1	X	1	FV_B_DAC

Current Ranges

The PMU can force current over 50mA. In order to achieve maximum accuracy while still being able to measure smaller currents, five current ranges are supported.

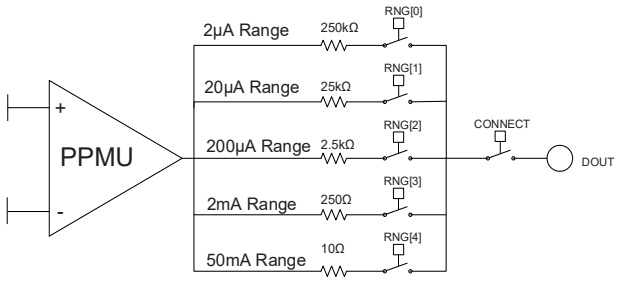


FIGURE 42: CURRENT RANGES

TABLE 69: PMU CURRENT RANGES

PMU_TERM_ENA	RNG [5:0]	CURRENT RANGE	IMAX*	RSENSE
0	000001	IR0	±2µA	250kΩ
0	000010	IR1	±20µA	25kΩ
0	000100	IR2	±200µA	2.5kΩ
0	001000	IR3	±2mA	250Ω
0	010000	IR4	±50mA	10Ω
0	100000	N/A	NA	NA

*Imax of a current range is defined as the current that creates a 500mV drop across the current range resistors. There is no hard limit, except for the current clamps, within the part to exceed IMAX for each current range. The currents that exceed Imax will simply continue to create a large voltage drop across the current range resistors until a headroom condition is reached.

The PMU_TERM_ENA bit must be set to ‘0’ for the RNG bits to have any effect on the range switches. This bit, when set to ‘1’, puts the PPMU into termination mode and is discussed later in this datasheet.

The SPI selects the current range by setting the range select bit high. Each range select bit has independent control, allowing a wide variety of “make before break” options when changing current ranges.

It is possible to select more than one range simultaneously. However, this option should be used only when changing ranges as a means of controlling the transient response associated with changing ranges or changing modes.

Activating more than one range simultaneously will have the effect of placing the current range resistors in parallel thus altering the transfer function. Activating more than one range at a time is not recommended for taking measurements.

Measure Current

The current across the sense resistor will create an analog voltage that is proportional to the current flowing through DOUT. Imax is determined by the current range selection. There is a transfer function between the current at the DOUT pin and the voltage measuring the current at the MON_# pins.

TABLE 70. MEASURE CURRENT TRANSFER FUNCTION

VOLTAGE ACROSS SENSE RESISTOR	I_{OUT}
–500mV	–Imax (Sinking current)
0V	0
+500mV	+Imax (Sourcing current)

There are three options for measuring current in the Mystery chip. Each of these options use the Monitor and Diagnostics buses discussed later in this datasheet.

- MI Output – The MI Output has a voltage reference of 2.25V. When no current is measured, the output voltage is 2.25V. For each selected current range, the voltage can vary ±1.25V from the reference voltage of +2.25V. The voltage corresponds to ±Imax and whether the PMU is sourcing current or sinking current. The MI output measuring instrumentation amplifier has a gain of 2.5, therefore the ±500mV across the sense resistor is gained up to ±1.25V.
- MI Output 2X – This option is the same as the MI Output above except the voltage swing for ±Imax is double to ±2.5V. The MI output 2X measuring instrumentation amplifier has a gain of 5.0.
- MI Input+/MI Input – This is a differential voltage measured between MI Input+ and MI Input-. A differential measurement between MI Input+ and MI Input- will vary from +500mV to -500mV. A differential voltage of 0V indicates 0 current.

These three options can be chosen using the MON_MH and MON_ML analog test buses. Please see Table 100 and Table 101 for selecting each option.

The PPMU current vs output voltage for the 50mA range is shown below. Please see Table 101 for selecting each option.

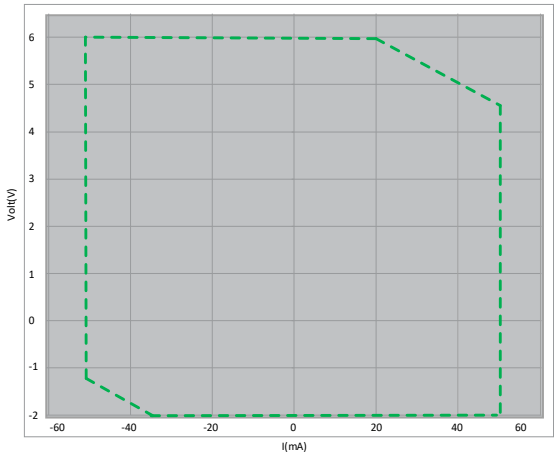


FIGURE 43: PPMU COMPLIANCE CURRENT

PPMU Architecture

The PPMU is made up of a two op-amp output stage architecture. The two stages are: Input op-amp and the output op-amp:

- The output op-amp is low gain so it can respond quickly to changes in the output.
- The input op-amp is high gain to provide a more accurate voltage.

With this architecture, there are feedback options for:

- Total PPMU including both output stages.
- The output op-amp stage.

Total PPMU Voltage Feedback

There are multiple voltage feedback nodes to the inverting input of the forcing op amp. The forcing op amp is automatically protected against going open loop when the PPMU goes into HiZ.

TABLE 71: VOLTAGE FEEDBACK OPTIONS

LOOP	PMU_ENA	FI_FV	CONNECT	REMOTE	MODE
0	X	X	X	X	Tight Loop
X	0	X	X	X	HiZ
X	1	1	1	X	FI
1	1	0	1	0	Local Sense
1	1	0	1	1	Remote Sense – Using adjacent channel
1	1	0	0	X	Open Loop Not Suggested

Tight Loop Feedback

With Loop = 0, the forcing op amp will be configured as a unity gain amplifier tracking FV. Tight loop is the default condition upon reset or power-up.

The tight loop configuration is NOT used for any traditional PMU FI or FV function. It is used mainly for:

- Stable default conditions
- Resistive load applications

Local Sense Feedback

The inverting feedback to the main forcing op-amp is at the DOUT pin. This will normally be the Feedback option used.

Remote Sense Feedback

Adjacent channels can be arranged in pairs to support a PMU remote sense mode. In remote sense mode, the output of one channel is used to force voltage while the DOUT pin of the other adjacent channel is used as a remote voltage sense input. Either channel in the adjacent pair can be used to as the forcing pin while the other channel's pin is used for remote sense. This option ensures the most accurate voltage at the load by eliminating IR (current * resistance) drops caused by trace resistance. This option uses two DOUT pins to accomplish this greater accuracy.

TABLE 72: REMOTE FEEDBACK

REMOTE	FEEDBACK
0	Local sense will be selected at DOUT pin.
1	Sense is connected to the adjacent channel DUT pin. Adjacent odd/even channels can be used to sense voltage at the DUT.

Output Op-Amp Voltage Feedback

There are three voltage feedback nodes to the inverting input of the output op-amp. The output op-amp is located just after the internal PPMU compensation caps.

TABLE 73: FB OPTIONS

FB [1:0]	FEEDBACK
00	Feedback from the amplifier output. This is the internal side of the sense resistor.
01	Feedback is from DOUT pin. If this option is used, the CONNECT switch is included in the feedback path. With this option, the CONNECT switch should always be closed.
1X	Feedback is from just inside the CONNECT switch. This is the recommended FB for all PPMU use and is the default connection. This option does not depend on the CONNECT switch being opened or closed.

FB [1:0] = 1X is the default setting for the FB register and is recommended for all use. It has been observed when changing this option during use, a glitch can be seen on the output.

Force Current (FI)

In FI Mode, the transfer function in Table 72 translates the current measured across a chosen RNG[5:0] resistor into an output current. The output of the MI instrumentation amplifier is used as the feedback to the forcing output amplifier. The DAC level voltages in FI mode match the voltages across the RNG[5:0] resistors. The FI_FV bit must be set to '1' for Force Current Mode.

The PMU FI loop uses the same DAC voltage range as used for FV (-2V to +6V nominal). The MI amplifier has a nominal output range of 1.00V to 3.50V (Full Scale Range) with 2.25V corresponding to 0mA, so FI uses only about 1/3 the available DAC range over Mystery's specified current range. Use care when programming the FI DAC to avoid forcing excess current by using the FV Current clamps.

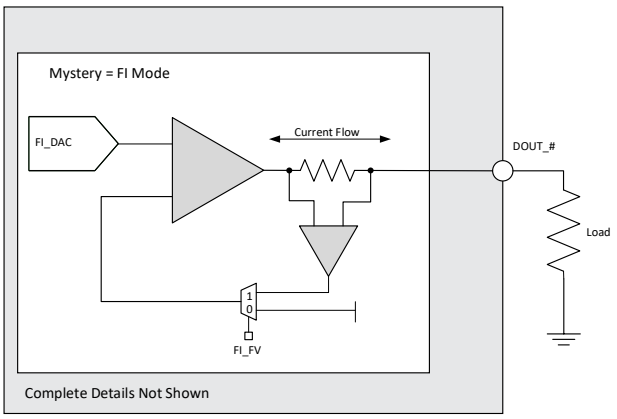


FIGURE 44: FORCE CURRENT MODE

TABLE 74: FORCE CURRENT DAC CODES TRANSFER FUNCTION

FI_DAC CODE	IOUT
B000	+Imax (Sourcing) Nominal
8000	0
5000	–Imax (Sinking) Nominal

Note: The values Table 74 are approximate values used for the FI_DAC codes.

FI Voltage Clamps

Each PMU has a set of programmable voltage clamps that limit the voltage output when the PMU is forcing current. The voltage clamps protect the DUT when current is being forced into a high impedance node. There are independent clamps for both High Voltage and Low Voltage. The voltage clamps are only available in Force Current mode.

The internal voltage clamps override the PPMU to reduce output current from the internal PPMU but do not limit any external current sources.

The clamps may be turned off by setting CLL_DIS = 1 and CLH_DIS = 1, in which case the clamps have no effect while DOUT varies between the supply voltages VCC and VEE. CLL_DIS disables the low voltage clamp, CLH_DIS disables the high voltage clamp. The CLH_DIS/CLL_DIS register bits are shared with both voltage clamps and current clamps.

TABLE 75: CLL/CLH_DIS

CLL/CLH_DIS	V_{SENSE}	VOLTAGE CLAMPS
1	X	Not Active
0	Vsense > CLH	DOUT = CLH
0	Vsense < CLL	DOUT = CLL
0	CLL < Vsense < CLH	Not Active

When active, if the sensed voltage exceeds the high or low voltage clamp, the PMU reduces the output current until the output voltage does not exceed the clamp. If the voltage subsequently returns to within the clamp thresholds, the PMU resumes forcing the programmed current.

The PMU voltage clamps are programmable with an 8-bit DAC. These can be set anywhere within the operable range of the PPMU.

TABLE 76: PMU VOLTAGE CLAMP LOW

CLL [7:0] Bit [7] UNUSED	PMU VOLTAGE CLAMP LOW
00000000	-2.2V
•	•
•	•
01111111	4.0V

TABLE 77: PMU VOLTAGE CLAMP HIGH

CLH [7:0] Bit [7] UNUSED	PMU VOLTAGE CLAMP HIGH
00000000	0.0V
•	•
•	•
01111111	6.2V

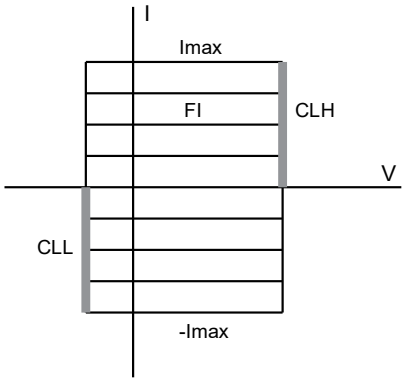


FIGURE 45: PMU VOLTAGE CLAMPS

FV Current Clamps

Each PPMU has two ranges of programmable current clamps which limit the amount of current flow when the PMU is forcing voltage. These clamps are useful in protecting the DUT from an over current situation. There are independent clamps for both sourcing and sinking. The Current Clamps are only available when the PMU is in Force Voltage mode.

The 2 current clamp ranges correspond to the 2 upper PPMU current ranges:

- 50mA range (8-bit setting)
- 2mA range (3-bit setting)

The current clamps ranges are automatically set by the Measure Current ranges. The 50mA current clamp range is automatically set when the IR4 range is enabled (RNG=0x10). The 2mA current clamp range is used for all other Measure Current ranges selected.

In the current ranges less than 2mA, the current is normally self-limited to the voltage drop caused by the output current and sense resistor (RSENSE).

The clamps may be turned off by setting CLL_DIS = 1 and CLH_DIS = 1, in which case the clamps have no effect while DOUT varies between the supply voltages VCC and VEE. CLL_DIS disables the sinking clamp, CLH_DIS disables the sourcing clamp. The CLH_DIS/CLL_DIS register bits are shared with both the voltage clamps and current clamps.

TABLE 78: CURRENT CLAMPS

CLL_DIS CLH_DIS	CURRENT	CURRENT CLAMPS
1	X	Not Active
0	Current > *ICH	DOUT = *ICH
0	Current < *ICL	DOUT = *ICL
0	*ICL < Current < *ICH	Not Active

*ICH/*ICL can be either the 50mA range or the 2mA range.

When active, the Current Clamps sense the current supplied by the PMU. If the current is within the boundaries set by the clamps, no action is taken. If the measured current exceeds the upper or lower current clamp, the PMU reduces the output voltage until the output current does not exceed the clamp. If the current subsequently drops back to within the clamp levels, the PMU resumes forcing its programmed voltage.

The internal current clamps override the PMU current only and does not limit external sources.

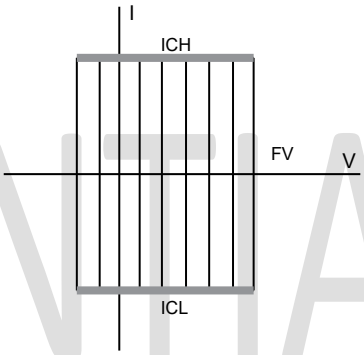


FIGURE 46: CURRENT CLAMPS

The 2 current clamp ranges are separated into sourcing and sinking registers.

TABLE 79: CURRENT CLAMP REGISTER SETTING

REGISTER	CURRENT	CURRENT CLAMP RANGE
ICH_IR50m [7:0]	50mA Sourcing	~ 2mA to 70mA
ICL_IR50m [7:0]	50mA Sinking	~-2mA to -70mA
ICH_IR2m [2:0]	2mA Sourcing	~ 3mA
ICL_IR2m [2:0]	2mA Sinking	~-3mA

The 50mA clamp allows the user to set the clamp levels from ±70mA down to about ±2mA.

The 2mA clamp is a coarse clamp that is intended to be calibrated to 3mA and left there just for gross DUT protection.

PPMU Termination Mode/Resistive Load

The PPMU may be connected and disconnected through the SPI port in order to provide a resistive load. This gives the user options for terminations resistances with different values other than the 50Ω termination available from the PE driver. The PPMU terminations are not intended to provide good RF termination. Connections available for "Termination Only" are not allowed when measuring current.

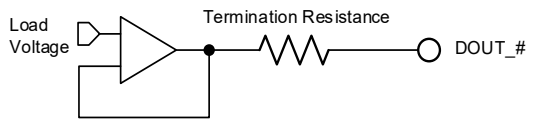


FIGURE 47: PPMU TERMINATION

Load Voltage

To establish the load voltage source, the following is recommended.

- FI_FV = 0 (FV mode)
- FV/FV_B = Desired Termination Voltage
- Loop = 0 (Tight Loop)
- PMU_ENA = 1
- CONNECT = 1

The forcing op amp will now be a low impedance voltage source.

PPMU Termination Mode

The resistance between the load voltage and DOUT will be the series combination of the resistors, switch resistances, and termination mode resistors. The combination of resistances depends on which termination mode is used and how much resistance is needed.

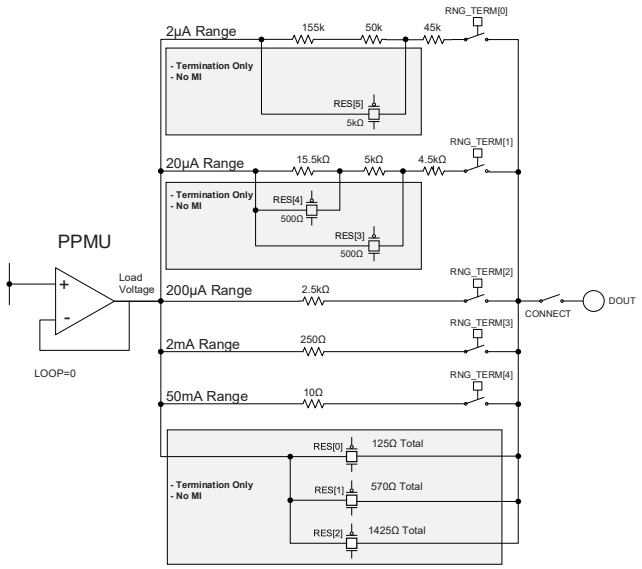


FIGURE 48: PPMU TERMINATION MODE

To enable Termination Mode, PMU_TERM_ENA must be set to '1'.

TABLE 80: PMU_TERM_ENA

PMU_TERM_ENA	PMU# TO DOUT_#
0	Normal PMU operation. PPMU resistors set by RNG [5:0] bits.
1	PPMU Termination Mode enabled. Termination resistors set by RNG_TRM [5:0] bits.

When PPMU Termination Mode is enabled (PMU_TERM_ENA = 1), range control for the PMU resistors switches over to the RNG_TRM [5:0] register bits. When PMU_TERM_ENA is disabled (PMU_TERM_ENA = 0), all the RNG_TRM bits are forced to '0' and control of the PPMU resistors is set by the RES [5:0] bits.

TABLE 81: PMU TERMINATION RESISTORS

PMU_TERM_ENA	RNG_TRM [5:0]	CURRENT RANGE	IMAX*	RSENSE
1	000001	IR0	±2μA	250kΩ
1	000010	IR1	±20μA	25kΩ
1	000100	IR2	±200μA	2.5kΩ
1	001000	IR3	±2mA	250Ω
1	010000	IR4	±50mA	10Ω
1	100000	NA	NA	NA

Additional termination resistances can be added using the RES [5:0] bits. These bits can only be used in PPMU Termination Mode (PMU_TERM_EN = '1'). When PMU_TERM_ENA is disabled (PMU_TERM_ENA = 0), the RE [5:0] bits are ignored.

TABLE 82: RES [6:0] BITS

PMU_TERM_ENA	RES[5:0]	RESISTANCE	TERMINATION RESISTANCE
1	RES [0]	125Ω	125Ω
1	RES [1]	570Ω	570Ω
1	RES [2]	1425Ω	1425Ω
1	RES [3]	500Ω	5KΩ When used in Conjunction with RNG_TRM [1]
1	RES [4]	500Ω	10KΩ Used in Conjunction with RNG_TRM [1]
1	RES [5]	5KΩ	50KΩ Used in Conjunction with RNG_TRM [0]

PMU Compensation

The PMU has variable compensation capacitor settings which can be changed to:

1. Be more stable under large capacitive loads.
2. Have a faster settling transient response when the DUT undergoes a change in load currents.

These settings will allow the adjustment of the internal dominant pole for optimal stability. This must be lower than the pole created by the sense resistor and load capacitor. Switching in the compensation can cause glitches, therefore it is best to do this when the PMU is disconnected (CONNECT = 0). There is a trade-off between stability and transient response performance. The larger the compensation capacitor, the more stable the PMU will be. However, the response settling times will be slower.

TABLE 83: COMPC

COMPC [4:0]	VALUE
00001	10pF
00010	20pF
00100	40pF
01000	70pF
10000	150pF

The compensation capacitors are in parallel and can be used in any combination. When 2 or more are selected, the compensation capacitance is additive.

Recommended settings:

For Cload ≤ 150pF use 0b11000

For Cload ≤ 0.1 µF use 0b11111

Output Op-Amp Compensation

The PPMU has an internal loop compensation capacitor for feedback loop stability. This capacitor can be disconnected to trade response time for stability. Under heavy capacitive load conditions, this compensation can be disconnected to speed up the output. The internal compensation can be connected or disconnected as follows:

TABLE 84: DISCONNECT OUPUT COMPENSATION

DISC_COMP_OUT	COMPENSATION
0	Connected (Recommended setting for most cases)
1	Disconnected

Rsense Compensation

Compensation capacitors can be connected across the Rsense range resistors to further fine tune settling response. It is recommended that both bits be set to “1”.

TABLE 85: RSENSE COMPENSATION

CON_COMP_RSEN [1:0]	OUTPUT COMPENSATION
11	Recommended Setting

PMU Gain Control

Gain control within the PMU can be fined tuned to aid in stability and settling times. The PMU_GAIN [3:0] register bits can change the gm (open loop gain) of several operational amplifiers within the PMU.

TABLE 86: PMU GAIN CONTROL

PMU_GAIN [3:0]	GM SETTINGS
Bit 0	Selects lower clamp gm
Bit 1	Selects lower input gm to the PMU
Bit 2	Selects higher output gm of the PMU
Bit 3	Unused

TABLE 87: RECOMMENDED PMU GAIN CONTROL SETTINGS

PMU_GAIN [3:0]	GM SETTINGS
0000	For all current ranges.

Channel Alarms

Each channel has the ability to detect a fault for the following conditions that will cause an alarm.

1. FV Current Clamp High
2. FV Current Clamp Low
3. FI Voltage Clamp High
4. FI Voltage Clamp Low
5. Driver short
6. Manually force an alarm for testing

Each of the alarms can be real time or latched and can be read back using the SPI port. Once the latched version of each alarm is set, it will remain high until cleared by an SPI port read or a chip level reset. The latched values are read only and are cleared when read. The real time Alarm can also be read back through the SPI port but are not cleared on a read.

Each channel has an ALARM_FLAG which is the logical ‘or’ of all the alarm bits of each channel. Each of the alarms can be masked from setting the ALARM_FLAG for each channel. The ALARM_FLAG is either derived from the latched alarm bits or the real time alarm bits based on the ALARM_MODE bit. The state of the ALARM_FLAG may also be read back using the SPI port.

The ALARM_MODE bit sets the alarm mode for all the alarms of each individual channel.

TABLE 88: ALARM MODE

ALARM_MODE	MODE
0	Latched mode with clear on read
1	Real time mode (unlatched)

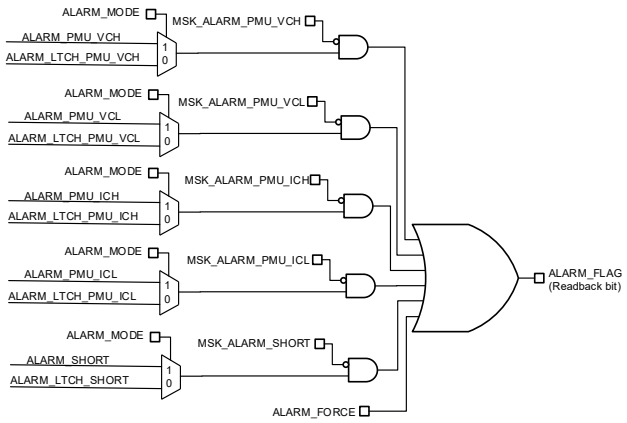


FIGURE 49: ALARM FLAG

FV Current Clamp Alarm

The Force Voltage current clamps alarms are enabled when the current clamps are enabled. There is a high current alarm and a low current alarm. These are enabled/disabled using the CLH_DIS/CLL_DIS bits. These bits are discussed in the Current Clamp section of this datasheet.

Current clamps are used to identify an overcurrent situation and raise a flag.

TABLE 89: CURRENT CLAMP ALARMS

ALARM_MODE	MODE	ALARM
0	Latched	ALARM_LTCH_PMU_ICH ALARM_LTCH_PMU_ICL
1	Unlatched	ALARM_PMU_ICH ALARM_PMU_ICL

The Current Clamp Alarms can be masked from setting the ALARM_FLAG for each channel.

TABLE 90: MSK_ALARM

MSK_ALARM_PMU_ICL MSK_ALARM_PMU_ICH	ALARM
0	Alarm Enabled
1	Alarm Masked

FI Voltage Clamp Alarm

The voltage clamps alarms are enabled when the current clamps are enabled. There is a high voltage alarm and a low voltage alarm. These are enabled/disabled using the CLH_DIS/CLL_DIS bits. These bits have been discussed in the Voltage Clamp section of this datasheet.

Current clamps are used to identify an overcurrent situation and raise a flag.

TABLE 91: VOLTAGE CLAMP ALARM

ALARM_MODE	MODE	ALARM
0	Latched	ALARM_LTCH_PMU_VCH ALARM_LTCH_PMU_VCL
1	Unlatched	ALARM_PMU_VCH ALARM_PMU_VCL

The Current Clamp Alarms can be masked from setting the ALARM_FLAG for each channel.

TABLE 92: VOLTAGE CLAMP MASK

MSK_ALARM_PMU_VCL MSK_ALARM_PMU_VCH	ALARM
0	Alarm Enabled
1	Alarm Masked

Driver Short

The Driver Short Alarm is enabled when the driver short circuit protection is engaged. The alarm indicates when the driver is sourcing or sinking over 60mA.

The Driver Short can be latched or real time.

TABLE 93: ALARM MODE - DRIVER SHORT

ALARM_MODE	MODE	ALARM
0	Latched	ALARM_LTCH_SHORT
1	Unlatched	ALARM_SHORT

The Driver Short Alarm can be masked from setting the ALARM_FLAG for each channel.

TABLE 94: DRIVER SHORT ALARM MASK

MSK_ALARM_SHORT	ALARM
0	Alarm Enabled
1	Alarm Masked

Alarm Force

Manually assert an alarm for diagnostics or testing.

TABLE 95: ALARM MASK

ALARM_FORCE	ALARM
0	Normal Operation
1	Set ALARM_FLAG bit

Chip Alarm

The ALARM pin indicates that an alarm from one of the channels has occurred. The ALARM output is a logical ‘or’ of the ALARM_FLAG bit from all the channels. This output is open-drain and needs an external 10kΩ resistor to VDD.

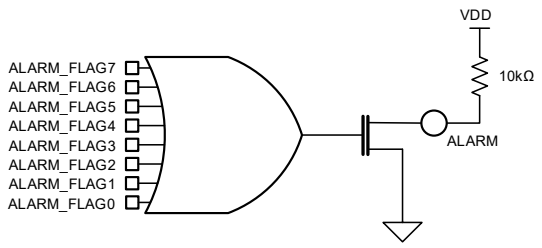


FIGURE 50: CHIP ALARM

Monitor and Diagnostics

A group of five analog test and calibration buses are implemented for various use measurements. These buses are used to route internal diagnostic nodes and measure voltages to external pins that can be measured for test, calibration, and diagnostic analysis. The pins that can be connected to these buses are MON_0, MON_1, MON_REF_0, MON_REF_1, EXT_SNS_HI, EXT_SNS_LO, EXT_FRC. There are internal switches controlled through the SPI port that make each one of these connections possible. The buses and usage are listed below.

TABLE 96: MEASUREMENT AND CALIBRATION BUS

MEASUREMENT AND CALIBRATION BUS	USAGE
FORCE	Connects each channel. PPMU output to the EXT_FRC pin.
CAL_MH	Connects the MON_MH_0 and MON_MH_1 bus to the EXT_SNS_HI pin
CAL_ML	Connects the MON_ML_0 and MON_ML_1 bus to the EXT_SNS_LO pin.
MON_MH_0 MON_MH_1	Connects to the positive output of the selected channel diagnostic mux. Can be connected to the MON_0 or MON_1 pin or to the CAL_MH bus.
MON_ML_0 MON_ML_1	Connects to the negative output of the selected channel diagnostic mux. Can be connected to the MON_REF_0 or MON_REF_1 pin or to the CAL_ML bus.

MON_MH and MON_ML Buses

- There are two MON_MH and two MON_ML buses. The MON_MH_0 and MON_ML_0 buses connect to the output pins MON_0 and MON_REF_0. The MON_MH_1 and MON_ML_1 buses connect to the output pins MON_1 and MON_REF_1.
- The MON_MH_0 and MON_MH_1 buses can be connected to the CAL_MH bus using the MXH_ENA [bit 0] register bits.
- The MON_ML_0 and MON_ML_1 buses can be connected to the CAL_ML bus using the MXL_ENA [bit 1] register bits.
- The MON_MH_0, MON_MH_1, MON_ML_0, and MON_ML_1 buses are connected to output pins as listed in Table 95. These buses are connected to the external pins using high impedance unity gain buffers. These buffers are added to be able to drive an external load and prevent IR drops across external switches which induce measurement error.

TABLE 97: MON_MH/MON_ML PIN CONNECTIONS

BUS	PIN CONNECTION
MON_MH_0	MON_0
MON_MH_1	MON_1
MON_ML_0	MON_REF_0
MON_ML_1	MON_REF_1

MON_MH and MON_ML Transfer Function

When measuring voltage, the MON_MH/MON_ML buses have a 1:1 transfer function with the voltages they are measuring.

When measuring current, the voltage at MON_MH/MON_ML varies proportionally to the current flow and is dependent of the measure path used. Please refer to the Measure Current section and Table 68.

FORCE Bus

The FORCE bus is used to connect the DOUT_# pin to the EXT_FRC pin. This is a low impedance path which can be used for voltage or current calibration. To connect the DOUT_# pin to the EXT_FRC pin, both the FORCE [#] and the FORCE_ENA switches must be closed using the SPI port. Typical switch values are shown in Table 97 below.

TABLE 98: FORCE_ENA

FORCE_ENA	FORCE BUS
0	FORCE bus disconnected from EXT_FRC pin
1	FORCE bus connected to EXT_FRC pin

TABLE 99: FORCE_ENA/FORCE[7:0] SWITCH RESISTANCE

SWITCH	TYPICAL SWITCH RESISTANCE
FORCE_ENA	30Ω
FORCE[7:0]	30Ω

CAL_MH and CAL_ML Buses

The CAL_MH bus is used as an interconnect between the MON_MH buses and the EXT_SNS_HI pin. EXT_SNS_HI is connected/disconnected using the CAL_MH_ENA bit. The CAL_ML bus is used as an interconnect between the MON_ML buses and the EXT_SNS_LO pin. EXT_SNS_LO is connected/ disconnected using the CAL_ML_ENA bit. These connections are used during calibration and other voltage measurements.

TABLE 100: CALMH_ENA

CAL_MH_ENA	CAL_MH BUS
0	CAL_MH bus disconnected from EXT_SNS_HI pin
1	CAL_MH bus connected to EXT_SNS_HI pin

TABLE 101: CALML_ENA

CAL_ML_ENA	CAL_ML BUS
0	CAL_ML bus disconnected from EXT_SNS_LO pin
1	CAL_ML bus connected to EXT_SNS_LO pin

Analog Mux Connections

Table 100 and Table 101 list analog nodes accessible through the MON_MH and MON_ML calibration busses.

- Use the MH_SELGP [1:0] and MH_SEL [4:0] to connect to the MON_MH buses.
- Use the ML_SELGP [1:0] and ML_SEL [4:0] to connect to the MON_ML buses.

MH_SELGP [1:0] and ML_SELGP [1:0] selects which subgroup (column) of the analog nodes will be selected.

MH_SEL [4:0] and ML_SEL [4:0] selects which internal channel node within the selected subgroup for connection to the CAL_MH or CAL_ML bus.

Monitor Reference

MON_REF is a reference signal used as the inverting input to a differential off-chip ADC. The SPI port selects the reference signal as well as controls the high impedance function.

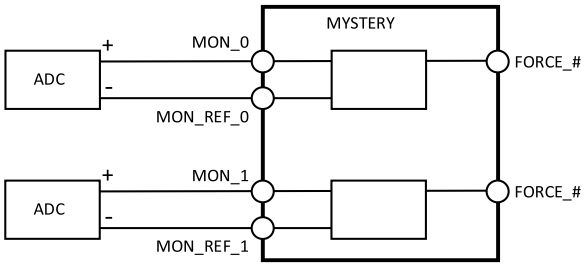


FIGURE 51: MONITOR REFERENCE

Analog Mux Connections

TABLE 102: ANALOG MUX CONNECTIONS - MON_MH

MH_SEL [4:0]	MH_SELGP [1:0]			
	PMU (0)	Drive (1)	Comparator (2)	Deskew (3)
0	No Connect	No Connection	No Connection	No Connection
1	DOUT output	DVH DAC_HV		
2	FV Mux Output, Note 1	DVL DAC_HV		
3	MI Output, Note 2	VTT DAC_HV		
4	MI Input +, Note 3	Temp Vb		
5		Vref		
6				
7				
8				
9				
10				
11				
12	GND_REF	DVH DAC_HS		
13	MI Output 2X, Note 4	DVL DAC_HS		
14	DUT_REMOTE	VTT DAC_HS		
15				

NOTES:

1. FV Mux Output. Mux is used to access internal DAC voltages and force them at the PMU output. This output is mainly used to calibrate internal DACs. This selection is made using the PMU_TESTMODE register.
2. Reference Voltage for MI Output is 2.25V.
3. Reference Voltage for MI Input+ is MI Input-. The ADC is doing the difference measurement. Common Mode range for MI Inp and MI Inn is approx. -1.5 to 5.5V.
4. Reference Voltage for MI Output is 2.25V. This MI measurement has a gain of 2.

TABLE 103: ANALOG MUX CONNECTIONS – MON_ML

ML_SEL [4:0]	ML_SELGP [1:0]			
	PMU (0)	Drive (1)	Comparator (2)	Deskew (3)
0	No Connection	No Connection	No Connection	No Connection
1	DGS	DGS		
2	GND_REF	GND_REF		
3	2.25V Ref, Note 1	2V_REF		
4	MI Input-	Temp Va		
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

NOTES:

1. 2.25V Reference on ADC_ML can be measured relative to GND_REF on ADC_MH.

External Components and Temp

Temperature Sensing

There are four sets of temperature diodes on chip that can be muxed to the MON_MH and MON_ML buses using the SPI port. These buses are discussed in the Monitor and Diagnostics section above. The temperature measurement is a differential voltage with the two voltages being generated using matched diodes. The two matched diodes are driven with different currents. The two voltages generated create a transfer function that track the internal junction temperature of the Mystery device. All circuitry and currents for temperature measurements are generated on chip.

As mentioned above, there are four sets of temperature diodes. Each set is shared between 2 adjacent channels (Channels 0/1, 2/3, 4/5, 6/7). If measuring the temperature on 2 adjacent channels, the user would read the same temperature.

The two internally generated voltages are:

- Temp Va
- Temp Vb

When measured, these may be used to calculate the junction temperature associated with the set of diodes as shown in the following equation.

$$TJ[^{\circ}C] = 1987 \cdot (Vb - Va) - 273$$

The on-chip temperature sensor provides a means for monitoring the relative temperature change of the IC. It is not intended for absolute temperature measurements.

DUT Ground Sense (DGS)

The actual ground reference level at the DUT may be different than that used by the DAC reference. DGS is a high impedance analog voltage that provides a means of tracking the destination ground and making an additional offset to the programmed internal DAC level, so the programmed level is correct with respect to the DUT. There is only one DGS input pin per chip.

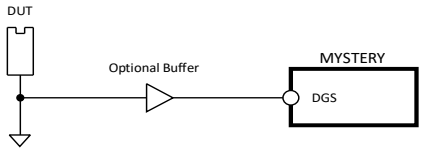


FIGURE 52: DGS

The input at DGS should be:

- Filtered for noise
- Stable
- Reflect the actual ground at the DUT

DGS is not added into the DC level when measuring a current by the PMU or forcing a current.

Required Off Chip Components

A precision voltage reference level and external resistor is required per chip. However, there may be a need for decoupling capacitors on the power supply pins. The need for decoupling capacitors is dependent upon the particular application and is therefore system dependent.

VREF

VREF is an analog input voltage this is used to program the on-chip DC levels. VREF should be held at +1.25V with respect to GND. There is one VREF pin shared by all channels on the same chip. This pin is a high impedance CMOS gate input.

RREF

RREF is a 12.4KΩ precision external resistor used to control various internal bias current.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VEEO, VEE <= GND
2. VCC <= VHH
3. VCCO <= VCC
4. VDD, VDDA <= VCCO
5. VEE <= VEEO

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation. The diodes will protect against power supply failure or inadvertent power supply sequencing. The forward voltage of the external Schottky diodes should be less than 500mV.

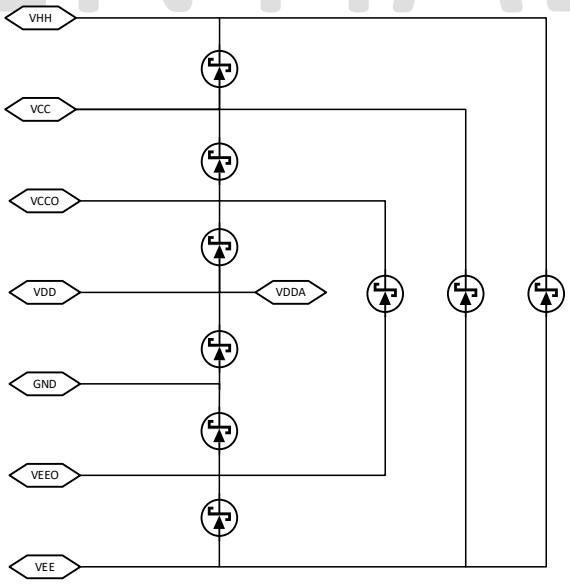


FIGURE 53: SCHOTTKY DIODES

Power Supply/Analog Voltage Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VHH
3. VCC
4. VCCO
5. VDD/VDDA
6. VREF
7. VEEO

Use the reverse sequence during power down.

Chip Reset

The RESET pin is an active high input that places all internal registers to a default state. The default state for each register is shown in the register map. The internal state of the Mystery registers is indeterminate following power-up and is not guaranteed on power-up alone. For this reason, a reset must be executed after a power-up to make sure all registers are in their default state. An internal pull-up resistor to VDD holds the pin high when left floating.

In addition, the SPI port can execute a reset (as a write only transaction). If the SW_RESET is written to, SW_RESET will fire off a one-shot pulse that performs the same function as an external RESET. SW_RESET is accessed in the SPI slave register using RSRC address = 14. This is shown in the register map section of the datasheet.

SPI - Host Serial Data Bus

The Mystery IC has a SPI Slave serial interface for host access to the registers. The full digital block is shown in Figure 54.

The composition of the signals in the SPI Bus are:

- Input serial clock (SPI_CLK)
- Data output port (SPI_SDO)
- Data input port (SPI_SDI)
- Chip select input port (SPI_CS)

SPI_CLK, SPI_SDO and SPI_SDI can be shared among multiple Mystery or other SPI Slave devices, with each device having its own dedicated SPI_CS. SPI_CS is an active low input. This is shown in Figure 53. The interface is designed to run up to 100MHz in point-to-point configuration with no other devices on the bus, and when all recommended PCB design guidelines are adhered to. Serial data is transmitted most significant bit (MSB) first. The Mystery IC will latch the serial data (commands, address and write data) on the rising edge of the serial input clock – the Controller is expected to launch serial data with the falling edge. The Mystery IC will by default drive read data on the falling edge of the serial input clock. Read data is by default launched 3.5 clock cycles after capturing the last address bit. The SPI Slave design also includes a wide degree of read launch timing programmability, which is to adapt to a variety of customer scenarios. The programmability options are located in the MODE_SEL section of the register map.

The serial clock can be free running or may stop after a bus transaction. The Mystery IC with all default settings requires a minimum of 32 clock cycles for an atomic bus operation, which is when each transaction is encapsulated within an active SPI_CS pulse.

Read/Write SPI diagrams are provided in Figure 55. Respective DC and AC parameters are provided in the specification section of the datasheet.

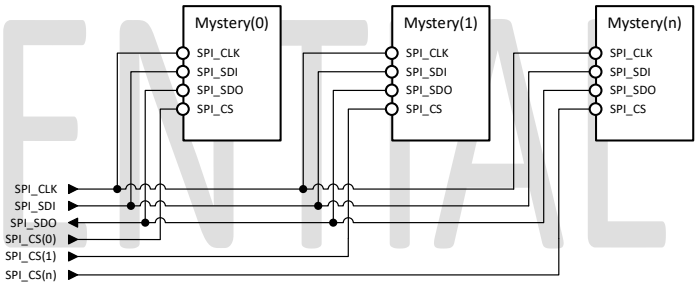


FIGURE 54: SPI INTERFACE CONNECT WITH MULTIPLE DEVICES

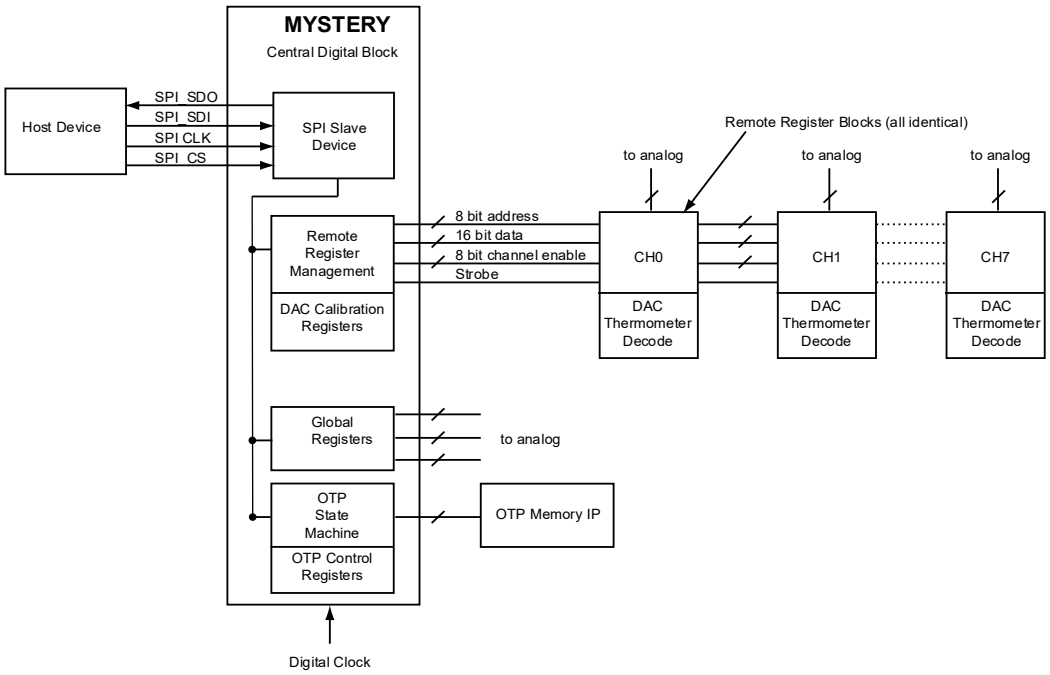


FIGURE 55: DIGITAL CONTROL BLOCK DIAGRAM

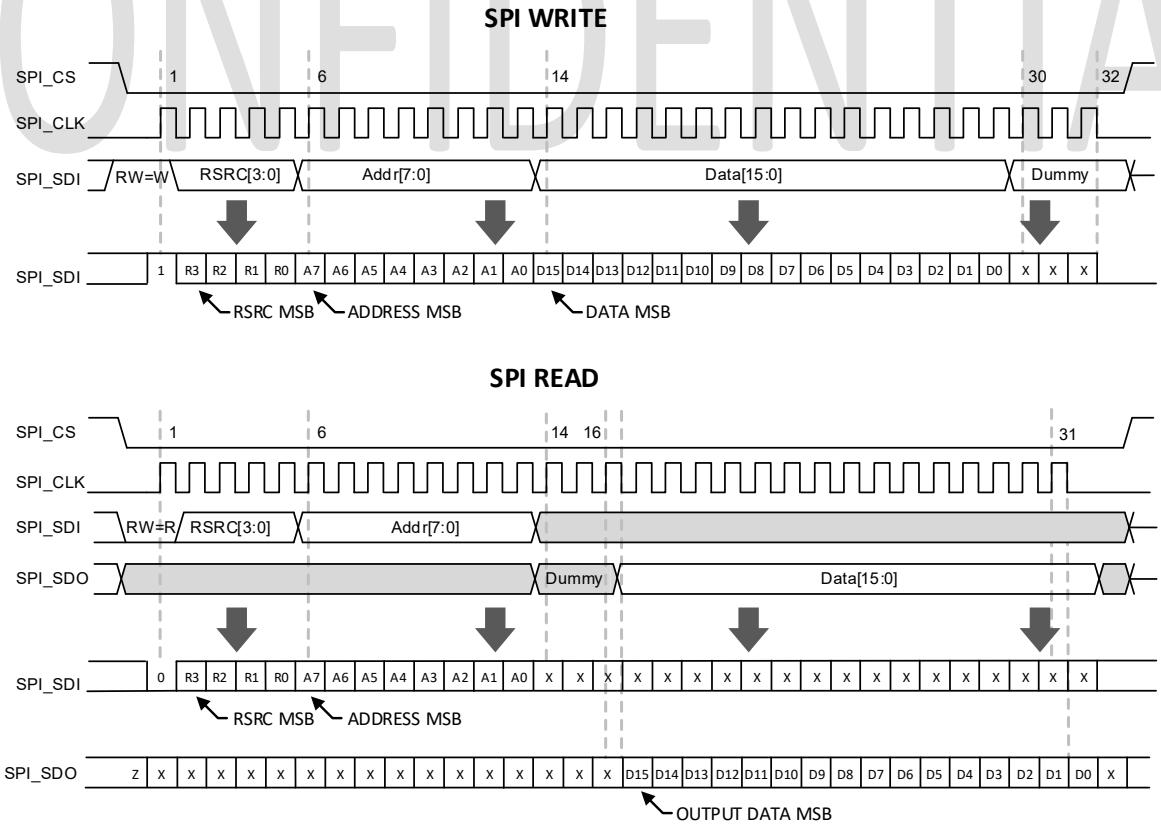


FIGURE 56: SPI INTERFACE

The SPI_CLK, SPI_CS, and SPI_SDI have 50Ω input termination resistors to VDD/2 which can be enabled or disabled using the

SPI port. These bits should be disabled when driving multiple Mystery devices with the same SPI bus.

TABLE 104: CLKTERM_ENA

CLKTERM_ENA	SPI_CLK/SPI_CS - 50Ω TERMINATION to VDD/2
0	Disabled
1	Enabled

TABLE 105: DATTERM_ENA

DATTERM_ENA	SPI_SDI - 50Ω TERMINATION to VDD/2
0	Disabled
1	Enabled

Host Interface Protocol

- The serial host protocol starts with a 1-bit read/write command, followed by a 4-bit resource selection field (RSRC), followed by an 8-bit address field on SPI_SDI. For write commands, the address is immediately followed by a 16-bit data field and then 3 dummy bits. The clock cycles of the dummy bits are used to push the data into the appropriate register. During read commands immediately following the address field on the SPI_SDI, there are 3 dummy bits after which a 16-bit data field is transmitted on the SPI_SDO port. Note that the Mystery IC will drive out of SPI_SDO on the falling edge of the serial input clock with the expectation that the host will latch each bit on the rising edge of the clock.
- The resource field (RSRC) is 4-bits that selects the type of register, channel, and number of registers which will be written or read. Selecting more than one resource for reads is not valid as only one channel can be read back at once. The 4-bit resource field is decoded as shown in Table 104.
- To write or read any single channel register, the resource field is programmed to the desired channel number (0 through 7).
- RSRC#14 configures specific behavior of the SPI Registers of the SPI port. These are referred to as the SPI Slave Registers. Please contact Elevate Semiconductor for additional detail.
- RSRC#15 is dedicated to Write-Multicast. This is writing the same value to an arbitrary combination of channels as programmed into RSRC_REG. RSRC_REG default is set to work as Write-Broadcast to all 8 channels which means that a write to RSRC#15 will reach all 8 channels. Should another replication pattern be desired (with different channels specified), the RSRC_REG should first be programmed with the channels desired, then issue a write to RSRC#15. That pattern will then stay in effect until reprogrammed, or device reset. The lower 8 bits of this RSRC_REG register are used to define multi-channel writes of any combination of channels. Bit 7 corresponds to channel 7 down to bit 0 for channel 0. Set the bit associated with the desired channels to "1" and the others to "0". For example, to multicast to all even channels you would write "01010101" (55 Hex) into the RSRC_REG register. See the register description section for additional detail.

TABLE 106: RESOURCE SELECTION

RSRC [3:0] Field Value (decimal)	Description	Address Range	Location
0 - 7	Remote Channel Registers	0x00 to 0x3F	Remote Register Block
0-7	Central Channel OTP	0x90 to 0x9F	Central Digital Block
13	Central Global Registers	0x80 to 0x8F	Central Digital Block
14	SPI Slave Registers	0x80 to 0x8F	Central Digital Block
15	Write-Multicast	0x00 to 0xFF	Central Digital Block

Mystery Digital Architecture

The digital architecture of Mystery is comprised of a central control block plus 8 channel register blocks which are connected to the central block via a parallel bus.

Central Registers

The central block contains the SPI serial port interface, channel register control and management, global registers and fuse memory control. The channel register control and management block in the main digital block is the interface between the SPI serial port and the channel registers in the channel register blocks. It also has global registers that control global chip functionality.

As mentioned above, the Mystery IC has fuse memory onboard to hold specific calibration data. These fuses are OTP (One Time Programmable) memory; meaning non-volatile and can be written only once. This memory is written during ATE test and holds various register values used to achieve optimal performance in the device. The data that is stored in OTP is explained in this datasheet and can be programmed to be used or bypassed.

Register Bit Mapping

Many registers have multiple smaller bit fields that can be written independently without affecting the other bit fields in that register. For these registers each independent bit field has a WE (write enable) bit defined that must be set to "1" for those bits to be affected by a write. Any bit fields whose WE bit is set to "0" during a write to that register will not be changed. Not all registers have WE bits.

Channel Register Blocks

The central block is connected to the eight remote blocks via a parallel bus interface. All the channel register blocks contain the same set of registers for each channel. They are differentiated in addressing only by the RSRC field of SPI frame, or the RSRC_REG when Write-Multicast is used. Write-Broadcast can be used to speed up configuration, which is by concurrently setting up all channels.

Fuse Memory

As mentioned above in the Central Registers section, Mystery contains onboard fuse memory that is one-time programmable and contains many of the calibration values needed for the device to meet specified limits. The calibration values in Fuse Memory are calculated and burned at ATE test and can be used or bypassed depending on the user. The user may opt to calibrate the device registers themselves.

The Fuse Memory data is located at address 0x98 to 0x9F.

The calibration values held in fuse memory are implemented in 3 ways and shown below. The 3 types are:

1. Calibration values stored in fuse memory are automatically used unless specifically bypassed by the user.
   - Example: RO_SINK_HV_FUSE [3:0]
2. Calibration values stored in fuse memory must be manually copied from Fuse Memory to its appropriate Calibration Register.
   - Example: OS_DVL_HS_FUSE [3:0]
3. Calibration values burned into fuse memory can be constructed into a linear calibration equation. These types of calibration values are signified with the suffixes: "Top" and "Bot". Using the calibration values in Fuse Memory, one can construct a calibration transfer function using the linear equation:

$$y = (m * x) + b:$$

$$where:\ m = slope,$$

$$b = y - intercept,$$

$$x = independent\ variable,$$

$$y = dependent\ variable$$

As shown below, the independent variable (x) is stored in Fuse Memory and the dependent variable (y) is in the description column in Table 105.

An example of this type of calibration is shown in the register: ICH_IR50m [7:0] – This register sets current clamps for the 50mA current range. This register has a range for from 2mA up to 70mA.

Two calibration values are burned into fuse memory for the 50mA point and the 10mA point:

ICH_IR50m_FUSE_TOP [7:0] = Calibration register value to set 50mA Current Clamp High ICH_IR50m_FUSE_BOT [5:0] = Calibration register value to set 10mA Current Clamp Low

From these 2 values, the user can construct a transfer function using the equation above. The 'x' values will be the values stored in fuse memory, and the 'y' values will be 50mA and 10mA.

Example: Set Current Clamp High = 35mA. Assume for this example the following values are written to Current Clamp High fuse memory.

ICH_IR50m_FUSE_TOP [7:0] = 180

ICH_IR50m_FUSE_BOT [5:0] = 30

1) x1 = ICH_IR50m_FUSE_TOP [7:0]:

   x1 = 180

2) x2 = ICH_IR50m_FUSE_BOT [5:0]

   x2 = 30

3) Calculate the slope from the above values: m = (y2 – y1) / (x2 – x1)

   m = (50 – 10) / (180 – 30)

   m = 0.2667

4) Calculate the y-intercept:

   b = y1 – (m * x1)

   b = 50 – (0.2667 * 180)

   b = 2

5) Find X value corresponding to 35mA.

   X = (Y – b)/m:

   X = (35 – b)/m

   X = (35-2)/0.2667

   X = 124

6) Write the X-value into the current clamp high register: ICH_IR50m [7:0] = 124

If the user just wants a current clamp of 50mA, the contents of the ICH_IR50m_FUSE_TOP [7:0] register can be copied to the ICH_IR50m [7:0] register.

TABLE 107: FUSE MEMORY

USE MEMORY REGISTER	DESCRIPTION	NOTE
DSKW_TEMPCO_FUSE[4:0]	Temperature Compensation Value for deskews. The DSKW_TEMPCO_FUSE_OVERD bit selects whether to use the calibrated value stored in fuse memory or override with the values in the DSKW_TEMPCO[4:0] register. Default '0' value selects fuse data and '1' selects register data.	The FUSE value for DSKW_TEMPCO_FUSE[4:0] cannot be read from memory. No action needs to be taken by the user unless they want to override the fused calibration value.
RO_SINK_HV_FUSE[3:0] RO_SRC_HV_FUSE[3:0] RO_SINK_HS_FUSE[3:0] RO_SRC_HS_FUSE[3:0]	Output Resistance sourcing and sinking adjustment bits for the HV and HS Drivers. The RO_SRC_SNK_FUSE_OVRD bit selects whether to use the calibrated value stored in fuse memory or override with the values in the RO_SINK_HV[3:0], RO_SINK_HS[3:0], RO_SRC_HV3:0], and RO_SRC_HS3:0] registers. Default '0' value selects fuse data and '1' selects register data.	The FUSE memory values for output resistance can be read for reference. No action needs to be taken by the user unless they want to override the fused calibration value. Note 2.
ICH_IR50m_FUSE_TOP[7:0]	Calibrated register setting for Current Clamp High = 50mA	Can be used to calculate Current Clamp High transfer function. The ICH_IR50m[7:0] clamp can be used to set a clamp level from 2mA to 70mA. Note 5.
OS_DVL_HS_FUSE[3:0]	Calibrated DAC analog offset setting for DVL_DAC used in HS Mode.	Must be manually copied from Fuse Memory to OS_DVL_HS[3:0] register. Note 1.
OS_DVH_HV_FUSE[3:0]	Calibrated DAC analog offset control for DVH_DAC used in HV Mode.	Must be manually copied from Fuse Memory to OS_DVH_HV[3:0] register. Note 1.
OS_DVH_HS_FUSE[3:0]	Calibrated DAC analog offset control for DVH_DAC used in HS Mode.	Must be manually copied from Fuse Memory to OS_DVH_HS[3:0] register. Note 1.
CLL_FUSE_BOT[3:0]	Calibrated register setting for Voltage Clamp Low = -2V	Can be used to calculate Voltage Clamp Low transfer function. The CLL[7:0] clamp can be used to set a clamp level from -2.2V to 4V. Note 3.
OS_VTT_ILOAD_FUSE[3:0]	Calibrated DAC analog offset control for VTT_ILOAD_DAC.	Must be manually copied from Fuse Memory to OS_VTT_ILOAD[3:0] register. Note 1.
OS_VTT_HV_FUSE[3:0]	Calibrated DAC analog offset setting for VTT_DAC used in HV Mode.	Must be manually copied from Fuse Memory to OS_VTT_HV[3:0] register. Note 1.
OS_VTT_HS_FUSE[3:0]	Calibrated DAC analog offset setting for VTT_DAC used in HS Mode.	Must be manually copied from Fuse Memory to OS_VTT_HS[3:0] register. Note 1.
OS_DVL_HV_FUSE[3:0]	Calibrated DAC analog offset setting for DVL_DAC used in HV Mode.	Must be manually copied from Fuse Memory to OS_DVL_HV[3:0] register. Note 1.
OS_CVB_DIFF_FUSE[3:0]	Calibrated DAC analog offset setting for CVB_DAC used in DIFF Mode.	Must be manually copied from Fuse Memory to OS_CVB_DIFF[3:0] register. Note 1.
OS_CVA_DIFF_FUSE[3:0]	Calibrated DAC analog offset setting for CVA_DAC used in DIFF Mode.	Must be manually copied from Fuse Memory to OS_CVA[3:0] register. Note 1.
OS_CVB_FUSE[3:0]	Calibrated DAC analog offset setting for CVB_DAC	Must be manually copied from Fuse Memory to OS_CVB[3:0] register. Note 1.
OS_CVA_FUSE[3:0]	Calibrated DAC analog offset setting for CVA_DAC	Must be manually copied from Fuse Memory to OS_CVA[3:0] register. Note 1.
ICL_IR50m_FUSE_TOP[7:0]	Calibrated register setting for Current Clamp Low = -50mA	Can be used to calculate Current Clamp Low transfer function. The ICL_IR50m[7:0] clamp can be used to set a clamp level from -2mA to -70mA. Note 6.
OS_FV_FUSE[3:0]	Calibrated DAC analog offset setting for FV_DAC	Must be manually copied from Fuse Memory to OS_FV[3:0] register. Note 1.
CLH_FUSE_BOT[3:0]	Calibrated register setting for Voltage Clamp High = 0.5V	Can be used to calculate Voltage Clamp High transfer function. The CLH[7:0] clamp can be used to set a clamp level from 0V to 6.2V. Note 4.
ICL_IR2m_FUSE[2:0]	Calibrated register setting for Current Clamp Low = -3mA	Must be manually copied from Fuse Memory to ICL_IR2m[2:0]register. Note 8.
ICH_IR2m_FUSE[2:0]	Calibrated register setting for Current Clamp High = 3mA	Must be manually copied from Fuse Memory to ICH_IR2m[2:0] register. Note 7.
CLH_FUSE_TOP[4:0]	Calibrated register setting for Voltage Clamp High = 6.0V	Can be used to calculate Voltage Clamp High transfer function. The CLH[7:0] clamp can be used to set a clamp level from 0V to 6.2V. Note 4.
CLL_FUSE_TOP[4:0]	Calibrated register setting for Voltage Clamp Low = 2V	Can be used to calculate Voltage Clamp Low transfer function. The CLL[7:0] clamp can be used to set a clamp level from -2.2V to 4V. Note 3.

USE MEMORY REGISTER	DESCRIPTION	NOTE
ICH_IR50m_FUSE_BOT[5:0]	Calibrated register setting for Current Clamp High = 10mA	Can be used to calculate Current Clamp High transfer function. The ICH_IR50m[7:0] clamp can be used to set a clamp level from 2mA to 70mA. Note 5.
ICL_IR50m_FUSE_BOT[5:0]	Calibrated register setting for Current Clamp Low = -10mA	Can be used to calculate Current Clamp Low transfer function. The ICL_IR50m[7:0] clamp can be used to set a clamp level from -2mA to -70mA. Note 6.

Notes:

1. Offset DAC calibration: Each Level DAC (DVH_DAC, DVL_DAC, FV_DAC, etc) has an associated 4-bit Offset DAC which is used to optimally center the voltage range of the level DAC to 2V. The Offset DAC calibration code stored in fuse memory is the value, when written, sets the Level DAC mid-code (0x8000) voltage to within guaranteed specification limits (1 code of ideal) of 2V. The value stored in fuse memory should just be copied from fuse memory to the associate offset DAC location. In most instances the calibrated offset DAC value is 0x0.
2. ROUT calibration: The output impedance of the HS and HV drivers have independent calibration values for both sourcing and sinking current. Each of these 4 ROUT values (HS source, HS sink, HV source, HV sink) are calibrated using a 4-bit register. The calibration values are calculated using a two 2-point (code 0 and 15) linear regression algorithm and stored in fuse memory. Impedance values to within 50Ω ± 4Ω may be achieved using the values stored and are automatically used unless bypassed. If more accurate ROUT calibration values are needed, the fuse memory values may be bypassed, and a user implemented calibration method used.
3. Voltage Clamp Low: The low voltage clamps are calibrated using the CLL[7:0] register. Using the output measured clamp voltages at codes 32 and 64, a linear transfer function is calculated. The values stored in fuse memory are the values from this linear transfer function which give output voltages closest to -2V and +2V. The user can then use the values stored in fuse memory to calculate a CLL[7:0] register setting for the clamp voltage needed. The Voltage Clamp Low is linear between -2V and 6V, with the guaranteed clamp range given in the specification section of the datasheet.
4. Voltage Clamp High: The high voltage clamps are calibrated using the CLH[7:0] register. Using the output measured clamp voltages at codes 16 and 64, a linear transfer function is calculated. The values stored in fuse memory are the values from this linear transfer function which give output voltages closest to +6.0V and +0.5V. The user can then use the values stored in fuse memory to calculate a CLH[7:0] register setting for the clamp voltage needed. The Voltage Clamp High is linear between 0V and 6V, with the guaranteed clamp range given in the specification section of the datasheet.
5. 50mA Current Clamp High: The 50mA High Current clamp is calibrated using the ICH_IR50m[7:0]. Using the values stored in the Current Clamp High Fuse memory to form a linear transfer function will result in an accuracy of less than 5mA between the clamp values of 10mA and 50mA. Outside of the 10mA and 50mA clamp values, the clamp becomes non-linear.
6. 50mA Current Clamp Low: The 50mA Low Current clamp is calibrated using the ICL_IR50m[7:0]. Using the values stored in the Current Clamp High Fuse memory to form a linear transfer function will result in an accuracy of less than 5mA between the clamp values of -10mA and -50mA. Outside of the -10mA and -50mA clamp values, the clamp becomes non-linear.
7. 2mA Current Clamp High: The calibration code stored in fuse memory is the code which sets the 2mA Current clamp high to within 1 code of the ideal 3mA value. The value stored in fuse memory should be copied directly into the 2mA current clamp high 3-bit register ICH_IR2m[2:0].
8. 2mA Current Clamp Low: The calibration code stored in fuse memory is the code which sets the 2mA Current clamp low to within 1 code of the ideal -3mA value. The value stored in fuse memory should be copied directly into the 2mA Current Clamp Low 3-bit register ICL_IR2m[2:0].

Level DAC Implementation

Each channel has 17, 16-bit integrated DAC Level registers. These 17 registers drive 9 actual DACs. Some of the DAC level registers are shared between the 9 actual DACs, with the shared implementation of this shown in Table 106. Not all the DACs are shared.

Before using the DAC levels, each of the DACs need to be enabled independently of each other.

The Voltage Clamps and Current Clamps do not use a 16-bit DAC to set the clamp levels. The clamps are set in the channel registers using an 8-bit DAC. These DACs do not need to be enabled before use.

The DACs are shown below:

TABLE 108: DAC LEVEL IMPLEMENTATION

DAC	ENABLE BIT	SHARED LEVELS
DVH_DAC	DVH_DACENA	N/A
DVL_DAC	DVL_DACENA	N/A
FI_DAC	FI_DACENA	N/A
ILSRC_DAC	ILOAD_DACENA	N/A
ILSNK_DAC	ILOAD_DACENA	N/A
CVA_DAC	COMP_DACENA	CVA_DAC, CVA_DIFF_DAC, CVA_PMU_MV_DAC, CVA_PMU_MI_DAC
CVB_DAC	COMP_DACENA	CVB_DAC, CVB_DIFF_DAC, CVB_PMU_MV_DAC, CVB_PMU_MI_DAC
VTT_DAC	VTT_DACENA	VTT_DAC, VTT_ILOAD_DAC
FV_DAC	FV_DACENA	FV_DAC, FV_B_DAC

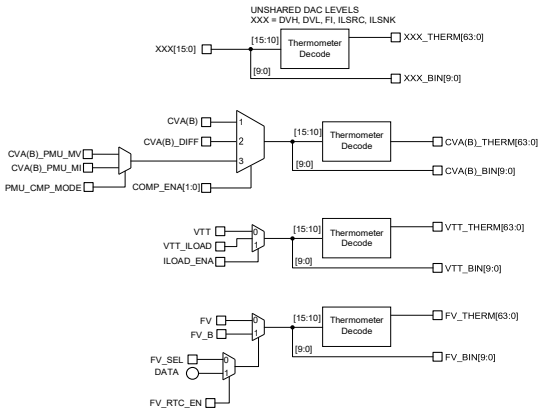


FIGURE 57: THERMOMETER DECODE BLOCK DIAGRAM

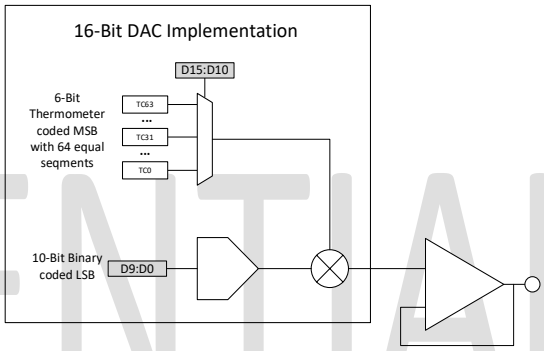


FIGURE 58: DAC ARCHITECTURE

DAC Thermometer Mode

Each channel's remote register block interfaces with the individual DAC. Each DAC is implemented as 10-bit binary LSB DAC plus a 63-segment thermometer coded MSB DAC. The 10 LSB bits are passed through directly, but the 6 MSB's must be decoded to a 63-bit thermometer code value.

In this mode the 10-bit binary DAC overlaps each thermometer segment, and each segment will have to be calibrated individually. Each of the 63 segments will have to be calibrated individually and a calibrated value must be written to the DAC register for the best results.

The Diagram below shows the Thermometer decode implementation.

DAC Offset Correction

There are 13 4-bit DAC offset level correction registers that can be used to optimally center the voltage range of each DAC by shifting the range up and down.

The offset correction registers are calibrated at ATE test and the values are burned into internal Fuse Memory. The user should copy these offset correction values from fuse memory to register memory which will implement the offset correction. In almost all cases, this value is written to 0x0.

Since this is calibrated at ATE, the user should not need to calibrate the DAC offset.

DAC Offset Implementation

As seen above, many of the DACs are used for more than one mode. For example, the CVA DAC is used for single ended compare, differential compare, and PMU compare. For this reason, there are more offset registers than there are DACs. The offset register used for each DAC is based on the mode selected during usage. The shared offset registers are shown below along with the modes used for each. There is no offset associated with the active loads.

TABLE 109: DAC OFFSET REGISTERS

DAC OFFSET REGISTER	WHEN OFFSET REGISTER IS USED	MODES	DAC
OS_DVH_HS[3:0]	DRV_ENA[1:0] = 0, 1, or 3	Driver HS Mode Driver Standby Mode	DVH_DAC
OS_DVH_HV[3:0]	DRV_ENA[1:0] = 2	Drive HV Mode	DVH_DAC
OS_DVL_HS[3:0]	DRV_ENA[1:0] = 0, 1, or 3	Driver HS Mode Driver Standby Mode	DVL_DAC
OS_DVL_HV[3:0]	DRV_ENA[1:0] = 2	Drive HV Mode	DVL_DAC
OS_VTT_HS[3:0]	(DRV_ENA[1:0] = 0, 1, or 3) And (ILOAD_EN = 0)	Driver HS Mode Driver Standby Mode	VTT_DAC
OS_VTT_HV[3:0]	(DRV_ENA[1:0] = 2) And (ILOAD_EN = 0)	Driver HV Mode	VTT_DAC
OS_VTT_ILOAD[3:0]	ILOAD_EN = 1	Active Load Enabled	VTT_DAC
OS_CVA[3:0]	COMP_ENA = 0, 1, or 2	Comparators Disabled Single Ended Compare Mode PPMU Compare Mode	CVA_DAC
OS_CVB[3:0]	COMP_ENA = 0, 1, or 2	Comparators Disabled Single Ended Compare Mode PPMU Compare Mode	CVA_DAC
OS_CVA_DIFF[3:0]	COMP_ENA = 3	Differential Compare Mode	CVA_DIFF_DAC
OS_CVB_DIFF[3:0]	COMP_ENA = 3	Differential Compare Mode	CVB_DIFF_DAC
OS_FV[3:0]	FV or FV_B	Force Voltage Mode	FV_DAC
OS_ILSRC[3:0]	N/A	Not Implemented	N/A
OS_ILSRC[3:0]	N/A	Not Implemented	N/A

Device ID and Device Rev

The Device ID and the Device Rev information is stored on-chip and can be read back using the SPI port. This information is stored in read only registers that identify the product identification and device revision.

The details of these 2 registers can be viewed in the Global Registers Table using the DEV_ID and the DEV_REV registers.

TABLE 110: DEVICE ID AND REV

REGISTER	DESCRIPTION
DEV_ID	Device Identification
DEV_REV	Device Revision

Note: DEV_ID = 0x4D0 Hex = 1232 Decimal.

Register Types

TABLE 111: REGISTER TYPES

REGISTER	DESCRIPTION
WO_PULSE	Write Only, one shot pulse (no storage). A write to this register will trigger an internal pulse.
WE	Write Enable (no storage)
RW	Read/Write (storage for write)
RO	Read Only (no storage, live)
ROL	Read only Latched (storage for external signal)
ROL_CLR	Read only Latched, Clear on Read (storage for external signal is reset by reading register)

Register Maps

SPI Slave Registers

Located in central digital block. Only one copy of each of these registers is in the chip. Resource field (RSRC) = 14.

TABLE 112: SPI SLAVE REGISTERS

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
SW_RESET	0x80	[15:1]	—	—	*Reserved (unused)*	
		[0]	WO_PULSE	—	Write '1' to reset all digital logic outside of this SPIe-Slave	SW_RESET
RSRC_REG	0x81	[15:8]	—	—	*Reserved (unused):*	
		[7]	RW	1	When SPI_RSRC=15 and corresponding bit of RSRC_REG is set to 1, the so-designated external resource is selected for access. That effectively constitutes Write-Multicast feature. "Resource 0 to 7 is typically an independent Channel, replicated up to 8 times, each replica with same address layout. Write-Multicast default (0x00FF) is therefore acting as Write-Broadcast for the Channels.	CHANNEL_7
		[6]	RW	1		CHANNEL_6
		[5]	RW	1		CHANNEL_5
		[4]	RW	1		CHANNEL_4
		[3]	RW	1		CHANNEL_3
		[2]	RW	1		CHANNEL_2
		[1]	RW	1		CHANNEL_1
		[0]	RW	1	To WRITE the same value into an arbitrary combination of these 14 resources, this RSRC_REG must first be initialized with desired pattern, to only then generate SPI_RSRC=15 transaction. E.g., for the Write-Multicast to all even channels, set this RSRC_REG=0x55, then generate SPI_WRITE access with SPI_RSRC=15 There is no Multicast for READ. It's an invalid operation. Should the SW still issue Read-Multicast, the data returned would be a combination of all addressed resources, thus of no practical value.	CHANNEL_0
MODE_SEL	0x82	[15:8]	—	—	*Reserved (unused):*	
		[7]			Applies only to Legacy mode of SPIe-Slave (when MODE_IS_ELEV=0). It then controls whether auto-increment is enabled or disabled. Compared to Elevated mode, where the equivalent bit comes with SPIE frame, this control is in Legacy mode static. That makes it a bit more involved to change the setting from frame to frame. By default, auto-increment is disabled, such as when interacting with FIFOs, so that multiple data words can be written into same address and same resource. It's only when auto-incr is enabled that the RDINC_IS_RSRC or WRINC_IS_ADDR come into play. - 0: Auto-Incr is disabled for Legacy Mode (Default) - 1: Auto-Incr is enabled for Legacy mode	ENINC4LEGACY
		[6]	RW	0	Selects the target of auto-increment for Read Burst. Comes into play only when auto-increment is enabled, be it through static ENINC4LEGACY CSR in Legacy mode, or frame-to-frame dynamic control for Elevated mode: - 0: Auto-Incr Read Address (Default) - 1: Auto-Incr Read Resource	RDINC_IS_RSRC
		[5]	RW	0	Selects the target of auto-increment for Write Burst. Comes into play only when auto-increment is enabled, be it through static ENINC4LEGACY CSR in Legacy mode, or frame-to-frame dynamic control for Elevated mode: - 0: Auto-Incr Write Resource (Default) - 1: Auto-Incr Write Address	WRINC_IS_ADDR
		[4:3]	RW	0	Selects the launch edge of SPI-Slave Read Data towards Controller: - x1: posedge0 (0.5 cycle earlier) - 00: negedge0 (Default, Legacy, Nominal) - 10: posedge1 (0.5 cycle later)	READ_PHASE

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
MODE_SEL	0x82	[2:1]	RW	0	Selects the number of wait states between SPI Address and first Read Data beat presented to Controller: - 00: 3 dummies - 01: 1 dummy – The most aggressive setting. Check chip datasheet for the max clock frequency that the timing is closed for with this setting - 10: 2 dummies (Default) - 11: 4 dummies	READ_DUMMY _CYCLE
		[0]	RW	0	Selects SPI-Slave Mode of operation: 0: Legacy mode (Default). SPIe operates as plain-old SPI: - no Double-Pumping - new, burst transactions still apply, except that they cannot be dynamically commanded from within SPI frame. They are instead controlled from the static ENINC4LEGACY field - new, expanded Resource Mapping still applies - new READ_PHASE[1:0] setting still applies - new READ_DUMMY_CYCLE[1:0] setting still applies 1: Elevated mode - all the enhancements including Double-Pumping and dynamically controlled Bursting	MODE_IS_ELEV
		[15:0]	—	0	Reserved for future expansion, such as to support tunable Delay Line on SPI clock and Read Training	
FUTURE	0x83	[15:0]	RW	0	Uncommitted register for quick validation of end-to-end integrity of SPI access	SCRATCHPAD
SCRATCHPAD	0x84	[15:0]	RO	0	Read Data returned by SPI-Slave in the most recent prior read cycle, regardless of SPI_ADDR. Used for debug. Subsequent reads of this address should return same value	LAST_RDAT
LAST_RDAT	0x85	[15:0]	RO	0	Write Data presented to SPI-Slave in the most recent prior write cycle, regardless of SPI_ADDR. Used for debug. Can emulate address-ignorant Scratchpad	LAST_WDAT
LAST_WDAT	0x86	[15:14]	—	—	*Reserved (unused)*	
LAST_MISC	0x87	[13:12]	RO	0	Command presented to SPI-Slave in the most recent prior cycle. Used for debug - bit[13]=1 when any of the autoincrementing is enabled. That's in Legacy mode (when MODE_IS_ELEV=0) the function of ENINC4LEGACY	LAST_CMD
		[11:8]	RO	0	Resource presented to SPI-Slave in the most recent prior cycle. Used for debug	LAST_RSRC
		[7:0]	RO	0	Address presented to SPI-Slave in the most recent prior cycle. Used for debug. Second read of this register will return its own address (=0x87)	LAST_ADDR

SPI Global Registers

Located in central digital block. Only one copy of each of these registers is in the chip. Resource field (RSRC) = 13.

TABLE 113: SPI GLOBAL REGISTERS

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
DEV_ID	0x80	[15:12]	—	—	*Reserved (unused):*	
		[11:0]	RO	—	CHIP_ID: Chip identification. Elevate chip ID is '4D0h'	DEV_ID [11:0]
DEV_REV	0x81	[15:12]	—	—	*Reserved (unused)*	
		[3:0]	RO	—	MAJOR_REV: This bit field is incremented to indicate a significant change that requires modification of the software. First silicon starts at revision 0001.	DEV_REV [3:0]
FORCE	0x82	[15:11]	—	—	Reserved (unused)	
		[10]	WE	—	FORCE_ENA_WE:	
		[9]	RW	0	FORCE_ENA: Connects FORCE bus to the output pad. "0" sets output pin to HiZ.	FORCE_ENA
		[8]	WE	—	FORCE_WE:	
		[7:0]	RW	0	FORCE: Bit 7 Connects Channel 7 to FORCE bus. Bit 6 Connects Channel 6 to FORCE bus. Bit 0 Connects Channel 0 to FORCE bus.	FORCE [7:0]
MON_SEL_0	0x83	[15:8]	RW	0	MON_ML_0: Connects selected channel ML bus to the MON_ML_0 bus. Bit [7] – connect channel 7 Bit [6] – connect channel 6 Bit [0] – connect channel 0	MON_ML_0[7:0]
		[7:0]	RW	0	MON_MH_0: Connects selected channel MH bus to the MON_MH_0 bus. Bit [7] – connect channel 7 Bit [6] – connect channel 6 Bit [0] – connect channel 0	MON_MH_0[7:0]
MON_XCTRL	0x84	[15:10]	—	—	*Reserved (unused):*	
		[9]	WE		CALML_ENA_WE:	
		[8]	RW	0	CALML_ENA: Connects CAL_ML bus to output pad. "0" sets output pad to HiZ.	CALML_ENA
		[7]	WE	—	CALMH_ENA_WE:	
		[6]	RW	0	CALMH_ENA: Connects CAL_MH bus to output pad. "0" sets output pad to HiZ.	CALMH_ENA
		[5]	WE	—	MXH_ENA_WE:	
		[4:3]	RW	0	MXH_ENA: Bit 1 - Enables connection of CAL_MH bus to MON_MH[1] bus. Bit 0 - Enables connection of CAL_MH bus to MON_MH[0] bus.	MXH_ENA [1:0]
		[2]	WE	—	MXL_ENA_WE:	
		[1:0]	RW	0	MXL_ENA: Bit 1 - Enables connection of CAL_ML bus to MON_ML_1 bus. Bit 0 - Enables connection of CAL_ML bus to MON_ML_0 bus.	MXL_ENA [1:0]
SPI_TERM	0x85	[15:3]	—	—	*Reserved (unused):*	
		[2]	WE		SPI_TERM_ENA_WE	
		[1]	RW	0	DATTERM_ENA: Set to "1" to enable termination in SPI_SDI input.	DATTERM_ENA
		[0]	RW	0	CLKTERM_ENA: Set to "1" to enable termination in SPI_CLK input.	CLKTERM_ENA
MON_SEL_1	0x86	[15:8]	RW	0	MON_ML_1: Connects selected channel ML bus to the MON_ML_1 bus. Bit [7] – connect channel 7 Bit [6] – connect channel 6 Bit [0] – connect channel 0	MON_ML_1[7:0]
		[7:0]	RW	0	MON_MH_1: Connects selected channel MH bus to the MON_MH_1 bus. Bit [7] – connect channel 7 Bit [6] – connect channel 6 Bit [0] – connect channel 0	MON_MH_1[7:0]

SPI Remote Register Block Addresses

Per Channel Configuration and Miscellaneous Control. There will be 8 copies of the remote registers connected to the central digital block via a parallel bus interface.

TABLE 114: SPI REMOTE REGISTER BLOCK ADDRESSES

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
PWR_CTRL	0x00	[15:14]	—		*Reserved (unused):*	
		[13]	WE		DRV_ENA_WE:	
		[12:11]	RW	0	DRV_ENA[1:0]: Power up enable for driver. 0 = Reduced power standby state (both driver modes) 1 = HS Driver mode enabled 2 = HV Driver mode enabled 3 = Reduced power standby state (both driver modes)	DRV_ENA[1:0]
		[10]	WE		PMU_ENA_WE:	
		[9]	RW	0	PMU_ENA: Power up enable for PMU. 0 = Low power standby state 1 = Enabled	PMU_ENA
		[8]	WE		COMP_ENA_WE:	
		[7:6]	RW	0	COMP_ENA: 0 = All Comparators disabled 1 = Single ended comparators enabled 2 = PMU comparators enabled 3 = Differential mode comparators enabled Comparators are non-functional in Standby mode.	COMP_ENA[1:0]
		[5]	WE		DESKEW_ENA_WE:	
		[4]	RW	0	DESKEW_EN_ENA: Power up enable for enable path de-skew. A logic 1 powers on enable path de-skew and a logic 0 bypasses and puts de-skew in a low power standby mode.	DESKEW_EN _ENA
		[3]	RW	0	DESKEW_DRV_ENA: Power up enable for drive path de-skew. A logic 1 powers on drive path de-skew and a logic 0 bypasses and puts de-skew in a low power standby mode.	DESKEW_DRV _ENA
		[2]	RW	0	DESKEW_CMP_ENA: Power up enable for compare path de-skews. A logic 1 powers on compare path de-skew and a logic 0 bypasses and puts de-skew in a low power standby mode.	DESKEW_CMP _ENA
		[1]	WE		ILOAD_ENA_WE:	
		[0]	RW	0	ILOAD_ENA: Power up enable for Active loads.	ILOAD_ENA
DAC_ PWRCTL	0x01	[15:14]	—		*Reserved (unused):*	
		[13]	WE		FI_DACENA_WE:	
		[12]	RW	0	FI_DACENA: Power up enable for FI level DAC. Controls “Enable DAC” pin on the FI DAC core.	FI_DACENA
		[11]	WE		FV_DACENA_WE:	
		[10]	RW	0	FV_DACENA: Power up enable for FV level DAC. Controls “Enable DAC” pin on the FV DAC core.	FV_DACENA
		[9]	WE		COMP_DACENA_WE:	
		[8]	RW	0	COMP_DACENA: Power up enable for all compare level DAC’s. Controls “Enable DAC” pin on the compare DAC cores.	CMP_DACENA
		[7]	WE		ILOAD_DACENA_WE:	
		[6]	RW	0	ILOAD_DACENA: Power up enable for both Iload level DAC’s. Controls “Enable DAC” pin on the Iload DAC cores.	ILOAD_DACENA
		[5]	WE		DVH_DACENA_WE:	
		[4]	RW	0	DVH_DACENA: Power up enable for the DVH level DAC. Controls “Enable DAC” pin on the DVH DAC core.	DVH_DACENA
		[3]	WE		DVL_DACENA_WE:	
		[2]	RW	0	DVL_DACENA: Power up enable for the DVL level DAC. Controls “Enable DAC” pin on the DVL DAC core.	DVL_DACENA
		[1]	WE		VTT_DACENA_WE:	
		[0]	RW	0	VTT_DACENA: Power up enable for the VTT level DAC. Controls “Enable DAC” pin on the VTT DAC core.	VTT_DACENA
DIG_TERM	0x02	[15]	WE		SPARE_1_WE	

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[14:10]	RW	0	OI_CLAMP_TESTMODE: Used for driver overcurrent clamp test mode. Bit[0] '0' Normal operation '1' Driver overcurrent clamp test mode. Open loop on clamp.	
		[9]	—		DIG_INVERT_WE:	
		[8]	RW	0	COMPA_INVERT: A logic 1 inverts polarity of COMP_A output	COMPA_INVERT
		[7]	RW	0	COMPB_INVERT: A logic 1 inverts polarity of COMP_B output	COMPB_INVERT
		[6]	RW	0	DAT_INVERT: A logic 1 inverts polarity of DAT input	DAT_INVERT
		[5]	RW	0	EN_INVERT: A logic 1 inverts polarity of EN input	EN_INVERT
		[4]	—		DIG_TERM_WE:	
		[3:2]	RW	0	DAT_TERM: Sets termination configuration of FlexIO DAT input termination. 0 = No termination 1 = 100Ω differential 2 = 100Ω differential 3 = 50Ω single ended	DIG_TERM[1:0]
		[1:0]	RW	0	EN_TERM: Sets termination configuration of FlexIO EN input termination. 0 = No termination 1 = 100Ω differential 2 = 100Ω differential 3 = 50Ω single ended	EN_TERM[1:0]
MON_CTRL	0x03	[15]	WE	—	MH_SEL_WE:	
		[14:13]	RW	0	MH_SELGP: Selects a subgroup of measure high signals. 0 = PMU 1 = Driver 2 = Comparator 3 = Deskew	MH_SELGP[1:0]
		[12:8]	RW	0	MH_SEL: Selects internal channel node within the selected subgroup for connection to the channel MH (measure high) bus. 0 = No connection 1 to 31 = See Table 102: Analog MUX Connections - MON_MH	MH_SEL[4:0]
		[7]	WE	—	ML_SEL_WE:	
		[6:5]	RW	0	ML_SELGP: Selects a subgroup of measure low signals. 0 = PMU 1 = Driver 2 = Comparator 3 = Deskew	ML_SELGP[1:0]
		[4:0]	RW	0	ML_SEL: Selects internal channel node within the selected subgroup for connection to the channel ML (measure high) bus. 0 = No connection 1 to 31 = See Table 103: Analog MUX Connections – MON_ML	ML_SEL[4:0]
DAC_MODE	0x04	[15]	WE	—	ILOAD_COMP_WE	
		[14:10]	RW	0	ILOAD_COMP: Iload compensation settings.	ILOAD_COMP[4:0]
		[9]	WE	—	DACMODE_WE:	
		[8:0]	RW	0	DACMODE: 0=Thermometer mode [8] DVH_MODE [7] DVL_MODE [6] VTT_MODE [5] CVA_MODE [4] CVB_MODE [3] FI_MODE [2] FV_MODE [1] ILSRC_MODE [0] ILSNK_MODE	DACMODE [8:0]
DAC_OS_1	0x05	[15:12]	R	0	*Reserved (unused):*	
		[11:8]	RW	1000	OS_DVH_HS: DAC analog offset control for DVH DAC. This for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when DRV_ENA[1:0] = 0,1 or 3	OS_DVH[3:0]
DAC_OS_1	0x05	[7:4]	RW	1000	OS_DVH_HV: DAC analog offset control for DVH DAC. This for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when DRV_ENA[1:0] = 2	OS_DVH[3:0]

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[3:0]	RW	1000	OS_DVL_HS: DAC analog offset control for DVL DAC. This for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when DRV_ENA[1:0] = 0,1 or 3	OS_DVL[3:0]
DAC_OS_2	0x06	[15:12]	RW	1000	OS_DVL_HV: DAC analog offset control for DVL DAC. This for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when DRV_ENA[1:0] = 2	OS_DVL[3:0]
		[11:8]	RW	1000	OS_VTT_HS: DAC analog offset control for VTT DAC. This for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when DRV_ENA[1:0] = 0,1 or 3 AND ILOAD_ENA = 0.	OS_VTT[3:0]
		[7:4]	RW	1000	OS_VTT_HV: DAC analog offset control for VTT DAC. This is for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when DRV_ENA[1:0] = 2 AND ILOAD_ENA = 0.	OS_VTT[3:0]
		[3:0]	RW	1000	OS_VTT_ILOAD: DAC analog offset control for VTT DAC. This is for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when ILOAD_ENA = 1.	OS_VTT[3:0]
DAC_OS_3	0x07	[15:12]	RW	1000	OS_CVA: DAC analog offset control for CVA DAC. This is for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when COMP_ENA[1:0] = 0, 1 or 2.	OS_CVA[3:0]
		[11:8]	RW	1000	OS_CVB: DAC analog offset control for CVB DAC. This is for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when COMP_ENA[1:0] = 0, 1 or 2.	OS_CVB[3:0]
		[7:4]	RW	1000	OS_CVA_DIFF: DAC analog offset control for CVA DAC. This is for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when COMP_ENA[1:0] = 3.	OS_CVA[3:0]
		[3:0]	RW	1000	OS_CVB_DIFF: DAC analog offset control for CVB DAC. This is for adjusting the level shift offset current output from the DAC core. These bits are muxed to output pins when COMP_ENA[1:0] = 3.	OS_CVB[3:0]
DAC_OS_4	0x08	[15:12]			*Reserved (unused):*	
		[11:8]	RW	1000	OS_FV: DAC analog offset control for FV DAC. This is for adjusting the level shift offset current output from the DAC core.	OS_FV[3:0]
		[7:4]	RW	1000	*Unused:*	
		[3:0]	RW	1000	*Unused:*	
PMU_CFG	0x09	[15]	WE	—	DISC_COMP_OUT_WE:	
		[14]	RW	0	DISC_COMP_OUT: This bit connects or disconnects the output stage local loop compensation used for heavy load conditions. This will help speed up the PMU output. The recommended setting for this is 0.	DISC_COMP_OUT
		[13]	WE	—	CON_COMP_RSEN_WE:	
		[12:11]	RW	11	CON_COMP_RSEN: This bit is used to connect compensation capacitors across Rsense. The recommended setting is to have this register bit set to 0b11 for all PMU configurations.	CON_COMP_RSEN[1:0]
		[10]	WE	—	REMOTE_WE:	
		[9]	RW	0	REMOTE: This bit enables PMU remote sense mode. This bit needs to be set on the channel that is being used as the force. The channel that is being used as sense must be configured through register settings such that the PMU is disconnected, and the driver is tri-stated. Hi-Z of sense channel is not automated within the hardware. 0: Normal PMU operation 1: Remote sense is connected to adjacent channel DUT pin. Adjacent odd/even channel pairs can be used together to force voltage and sense voltage at the DUT. LOOP must also be set to "1". See Chart	REMOTE
		[8]	WE	—	FB_WE:	
		[7:6]	RW	10	FB: This bit selects the PMU feedback mode. 00: Output stage feedback from amplifier output (internal side of sense resistor). 01: Output stage internal feedback from DUT output. When FB=01 the pmu connect switch (CONNECT) is in the feedback path. Therefore, when the pmu connect switch is opened the FB bit should be set back to 0b0. 1X: Output stage feedback from just inside connect switch.	FB[1:0]
		[5]	WE	—	LOOP_WE:	
		[4]	RW	0	LOOP: This bit selects between tight loop operation and normal operation on the PMU. Tight loop is used for setting a stable default condition and when	LOOP

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
					forcing voltage while PMU is being used as a resistive load. 0: Default, tight loop enabled 1: Normal PMU operation	
		[3]	WE	—	FI_FV_WE:	
		[2]	RW	0	FI_FV: This bit selects between FI or FV mode. 0: FV 1: FI	FI_FV
PMU_CFG	0x09	[1]	WE	—	CONNECT_WE:	
		[0]	RW	0	CONNECT: This bit enables PMU output. 0: PMU output is tri-stated 1: PMU is active	CONNECT
PMU_IRNG	0x0A	[15]	WE	—	FlexIO_LS_WE:	
		[14:13]	RW	0	FlexIO_LS: This bit is used to setup the comparator output stage.	FlexIO_LS
		[12]	WE	0	COMPC_WE:	
		[11:7]	RW	11000	COMPC: This bit selects compensation capacitor. Each bit enables one. Bit [0]: 10pF Bit [1]: 20pF Bit [2]: 40pF Bit [3]: 70pF Bit [4]: 150pF	COMPC[4:0]
		[6]	WE	—	RNG_WE[5:0]:	
		[5:0]	RW	00001	RNG[5:0]: PMU Range selection: When PMU_TERM_ENA is set to '0' these bits are used to control RNG[5:0] Bit [0] = Selects PMU FI/MI range of 2μA (250kΩ resistor) Bit [1] = Selects PMU FI/MI range of 20μA (25kΩ resistor) Bit [2] = Selects PMU FI/MI range of 200μA (2.5 kΩ resistor) Bit [3] = Selects PMU FI/MI range of 2mA (250Ω resistor) Bit [4] = Selects PMU FI/MI range of 50mA (10Ω resistor). Reduced voltage range at max current in this mode. Bit [5] = Unused	RNG[5:0]
PMU_TERM	0x0B	[15]	WE	—	PMU_TERM_ENA_WE:	
		[14]	RW	0	PMU_TERM_ENA: When set to "1" PMU_TERM is enabled and the range control selection for all PMU resistors including the core FI range resistors is switched over to this register (bits [5:0]). When set to "0" all PMU_TERM[x] signals are forced low, and control of the MI range resistors is set to the RNG[5:0] register. PMU needs to be also configured for FV mode.	PMU_TERM _ENA
		[13]	WE	—	RES_WE:	
		[12:6]	RW	0	RES[6:0]: Selects termination mode resistors when PMU_TERM_ENA is set to "1". When PMU_TERM_ENA is set to "0" then all of these bits are forced to "0". Digital block output pin Bit [0] = Selects term mode driver with 125Ω resistor for termination mode only. Bit [1] = Selects term mode driver with 570Ω resistor for termination mode only. Bit [2] = Selects term mode driver with 1425Ω resistor for termination mode only. Bit [3] = When enabled in conjunction with RNG_TERM[1] (5kΩ) this switch sets a resistance of 5kΩ total. Bit [4] = When enabled in conjunction with RNG_TERM [1] (25kΩ) this switch sets a resistance of 10kΩ total. Bit [5] = When enabled in conjunction with RNG_TERM [0] (250kΩ) this switch sets a resistance of 50kΩ total. Bit [6] = Unused	RES[6:0]
		[5:0]	RW	0	RNG_TRM: Selection of PMU range resistors during PMU termination mode. When PMU_TERM_EN is set to "1" these bits are used to control pins RNG_TRM[5:0]. Bit [0] = Selects PMU FI/MI range of 2μA (250kΩ resistor) Bit [1] = Selects PMU FI/MI range of 20μA (25kΩ resistor) Bit [2] = Selects PMU FI/MI range of 200μA (2.5kΩ resistor) Bit [3] = Selects PMU FI/MI range of 2mA (250Ω resistor) Bit [4] = Selects PMU FI/MI range of 50mA (10Ω resistor). Reduced voltage range at max current in this mode. Bit [5] = Unused	RNG_TRM[5:0]
PMU_FI_VCL	0x0C	[15]	WE	—	PMU_GAIN_WE:	
		[14:11]	RW	0	PMU_GAIN: Selects gm settings for PMU amplifiers.	PMU_GAIN[3:0]

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
					Bit [3] = Unused Bit [2] = selects higher output gm Bit [1] = selects lower input gm Bit [0] = selects lower clamp gm	
		[10]	WE	—	CLL_DIS_WE:	
		[9]	RW	0	CLL_DIS: Set to "1" to disable the low voltage clamp. This bit also disables the current sinking clamp in FV as both clamp circuits use the same amplifier.	CLL_DIS
PMU_FI_VCL	0x0C	[8]	WE	—	CLL_WE:	
		[7:0]	RW	0	CLL: The PMU Low Voltage Clamp value Bit [7] Unused.	CLL[7:0]
PMU_FI _VCH	0x0D	[15]	WE	—	SPARE_4_WE:	
		[14:11]	RW	0	SPARE_4: TBD	SPARE_4[3:0]
		[10]	WE	—	CLH_DIS_WE:	
		[9]	RW	0	CLH_DIS: Set to "1" to disable the high voltage clamp. This bit also disables the current sourcing clamp in FV as both clamp circuits use the same amplifier.	CLH_DIS
		[8]	WE	—	CLH_WE:	
		[7:0]	RW	0x7F	CLH: The PMU High Voltage Clamp value Bit[7] Unused.	CLH[7:0]
PMU_MISC	0x0E	[15]	WE	—	PMU_TESTMODE_WE:	
		[14:11]	RW	0	PMU_TESTMODE: Test control bits to select internal DAC voltages to be connected to the PMU output for production test. Must also select option 2 under PMU in MON mux control. 0 = FV_DAC: Force Voltage DAC 1 = CCL: Voltage Clamp Low DAC 2 = CCH: Voltage Camp High DAC 3 = FI_DAC: Force Current DAC 4 = CVB_DAC: 5 = CVA_DAC: 6 = DUT_MUX 7 - 15 = Unused	PMU_TESTMODE [3:0]
		[10]	WE	—	ICL_METHOD_WE:	
		[9]	RW	0	ICL_METHOD: This bit selects current clamp sense point is implemented. '0' = Output Stage: '1' = Use MI to clamp: For internal use only. Should always be set to '0'.	ICL_METHOD
		[8:0]	—	—	*Reserved (unused):*	
ILOAD_CFG	0x0F	[15]	WE	—	ILOAD_COMPMODE_WE:	
		[14:10]	RW	0	ILOAD_COMPMODE: Bit[4:1] = Unused Bit[0] = 0: default compensation recommended for most use cases. 1: use register ILOAD_COMP register for compensation setting.	ILOAD_ COMPMODE [4:0]
		[9]	WE	—	ILOAD_RANGE _WE:	
		[8:4]	RW	0	ILOAD_RANGE: Bit 0 used to switch Active Load to 2mA range. Bit[4:1] = Unused Bit[0] = 0: 24mA Active Load range 1: 1mA Active load range.	ILOAD_RANGE [4:0]
		[3]	WE	—	ILOAD_RT_WE:	
		[2]	RW	0	ILOAD_RT: Real time pattern control for Iload. When set to "1" the Iload connection is controlled by the real-time signal on the EN pins. When EN is low the Iload will be connected. Must also power up the Iload circuit first. When set to "0", the Iload connection is controlled by ILOAD_CONNECT.	ILOAD_RT
		[1]	WE	—	ILOAD_CONNECT_WE:	
		[0]	RW	0	ILOAD_CONNECT: Register control to connect Iload. When set to "1" Iload is connected to DOUT pin.	ILOAD _CONNECT
COMP_CFG	0x10	[15:7]	—	—	*Reserved (unused):*	
		[6]	WE	—	RING_EN_WE:	
		[5]	RW	0	RING_EN: Writing a "1" enables de-skew ring oscillator mode.	RING_EN
		[4]	WE	—	FRC_CV_EN_WE:	
		[3]	RW	0	FRC_CV_EN: This bit forces the output value of the comparators to the values programmed into register bits CVH_D and CVL_D.	FRC_CV_EN

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
					0: Comparator outputs operate normally and respond to their input signal. 1: Comparator output states forced to the value store in registers CVH_D and CVL_D. When in this mode this control overrides any signal seen at the input of the comparator.	
		[2]	WE	—	CVX_D_WE:	
		[1]	RW	0	CVA_D: This bit is used to determine comparator A output value while FRC_CV_EN is high. Used for all comparator modes. 0: Force compare high comparator output to a logic low state. 1: Force compare high comparator output to a logic high state.	CVA_D
		[0]	RW	0	CVB_D: This bit is used to determine comparator B output value while FRC_CV_EN is high. Used for all comparator modes. 0: Force compare low comparator output to a logic low state. 1: Force compare low comparator output to a logic high state.	CVB_D
CMP_MODE	0x11	[15:2]	WE		*Reserved (unused):*	
		[1]	WE	—	PMU_CMP_MODE_WE:	
		[0]	RW	0	PMU_CMP_MODE: Used to select whether PMU comparators are monitoring MV or MI. Set to "0" for MV and "1" for MI.	PMU_CMP _MODE
DRV_MODE	0x12	[15]	WE	—	FENA_WE:	
		[14:13]	RW	0	FENA: FORCE the state of the enable in the pin electronics driver. When this force is released, the driver will return to the enable state indicated by the Enable input pins. FIOE [1] FIOE [0] 0 X Pattern (EN) 1 0 Force Driver Off 1 1 Force Driver On	FENA [1:0]
		[12]	WE	—	FDAT_WE:	
		[11:10]	RW	0	FDAT: FORCE the DATA in the pin electronics driver. When this force is released, the driver will return to the logic state indicated by the Data input pins. FDAT [1] FDAT [0] 0 X Pattern (DAT) 1 0 Force Data 0 1 1 Force Data 1	FDAT [1:0]
		[9]	—	—	*Reserved (unused):*	
		[8]	WE	—	DRV_DIFF_WE:	
		[7]	RW	0	DRV_DIFF: Set to "1" to enable differential drive mode for the channel. This will result in this channel taking the inverted data from the adjacent channel of the channel pair (0/1, 2/3, 4/5, 6/7).	DRV_DIFF
		[6]	WE	—	HS_PRE_WE:	
		[5:2]	RW	1000	HS_PRE: 4-bit pre-emphasis control for high-speed driver	HS_PRE [3:0]
		[1]	WE		TERM_VTT_WE:	
		[0]	RW	0	TERM_VTT: Mode VTT select. This bit determines what state the driver goes to when disabled. 0: Selects drive HiZ when drive enable is low. 1: Selects drive to VTT level when drive enable is high. VTT voltage level is programmed with register VTERM.	TERM_VTT
DRV_SLEW _HV	0x13	[15:12]	—	—	*Reserved (unused):*	
		[11]	WE	—	RO_SRC_SNK_FUSE_OVRD_WE:	
		[10]	RW	0	RO_SRC_SNK_FUSE_OVRD: This bit selects whether to use the calibrated value stored in fuse memory or override with the value in registers RO_SRC_HS, RO_SINK_HS, RO_SRC_HV and RO_SINK_HV. Default "0" selects fuse data and "1" selects register data.	
		[9]	WE	—	SLEW_HV_N_WE:	
		[8:5]	RW	0	SLEW_HV_N: Negative slew rate control for HV driver only.	SLEW_HV_N [3:0]
		[4]	WE	—	SLEW_HV_P_WE:	
		[3:0]	RW	0	SLEW_HV_P: Positive slew rate control for HV driver only.	SLEW_HV_P [3:0]
DRV_ROUT _HS	0x14	[15:10]	—	—	*Reserved (unused):*	
		[9]	WE	—	RO_SRC_HS_WE:	
		[8:5]	RW	0	RO_SRC_HS: These bits adjust HS driver output sourcing resistance.	RO_SRC_HS [3:0]

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[4]	WE	—	RO_SINK_HS _WE:	
		[3:0]	RW	0	RO_SINK_HS: These bits adjust HS driver output sinking resistance.	RO_SINK_HS [3:0]
DRV_ROUT _HV	0x15	[15:10]	—	—	*Reserved (unused):*	
		[9]	WE	—	RO_SRC_HV_WE:	
		[8:5]	RW	0	RO_SRC_HV: These bits adjust HV driver output sourcing resistance.	RO_SRC_HV [3:0]
		[4]	WE	—	RO_SINK_HV _WE:	
		[3:0]	RW	0	RO_SINK_HV: These bits adjust HV driver output sinking resistance.	RO_SINK_HV [3:0]
DAT_DELAY	0x16	[15]	WE	—	DAT_CRS_DEL_WE:	
DAT_DELAY	0x16	[14:9]	RW	0	DAT_CRS_DEL: Delay value for the driver data path de-skew. (~10ns) “000000” = Min delay “100111” = Max delay. Code above “100111” not allowed.	DAT_CRS_DEL [5:0]
		[8]	WE	—	DAT_MED_DEL_WE:	
		[7:5]	RW	0	DAT_MED_DEL: Delay value for the compare path de-skew. (~375ps) “000” = Min delay “111” = Max delay	DAT_MED_DEL [2:0]
		[4]	WE	—	DAT_FINE_DEL_WE:	
		[3:0]	RW	0	DAT_FINE_DEL: Delay value for the driver data path de-skew. (~110ps) “0000” = Min delay “1111” = Max delay	DAT_FINE_DEL [3:0]
EN_DELAY	0x17	[15]	WE	—	EN_MED_DEL_WE:	
		[14:9]	RW	0	EN_CRS_DEL: Delay value for the driver enable path de-skew. (~10ns) “000000” = Min delay “10111” = Max delay. Code above “100111” not allowed.	EN_CRS_DEL [5:0]
		[8]	WE	—	EN_MED_DEL_WE:	
		[7:5]	RW	0	EN_MED_DEL: Delay value for the compare path de-skew. (~375ps) “000” = Min delay “111” = Max delay	EN_MED_DEL [2:0]
		[4]	WE	—	EN_FINE_DEL_WE:	
		[3:0]	RW	0	EN_FINE_DEL: Delay value for the driver enable path de-skew. (~110ps) “0000” = Min delay “1111” = Max delay	EN_FINE_DEL [3:0]
CMPA _DELAY	0x18	[15]	WE	—	CMPA_CRS_DEL_WE:	
		[14:9]	RW	0	CMPA_CRS_DEL: Delay value for the compare path de-skew. (~10ns) “000000” = Min delay “100111” = Max delay. Code above “100111” not allowed.	CMPA_CRS_DEL [5:0]
		[8]	WE	—	CMPA_MED_DEL_WE:	
		[7:5]	RW	0	CMPA_MED_DEL: Delay value for the compare path de-skew. (~375ps) “000” = Min delay “111” = Max delay	CMPA_MED _DEL [2:0]
		[4]	WE	—	CMPA_FINE_DEL_WE:	
		[3:0]	RW	0	CMPA_FINE_DEL: Delay value for the compare path de-skew. (~110ps) “0000” = Min delay “1111” = Max delay	CMPA_FINE_DEL [3:0]
CMPB _DELAY	0x19	[15]	WE	—	CMPB_CRS_DEL_WE:	
		[14:9]	RW	0	CMPB_CRS_DEL: Delay value for the compare path de-skew. (~10ns) “000000” = Min delay “100111” = Max delay. Code above “100111” not allowed.	CMPB_CRS_DEL [5:0]
		[8]	WE	—	CMPB_MED_DEL_WE:	
		[7:5]	RW	0	CMPB_MED_DEL: Delay value for the compare path de-skew. (~375ps) “000000” = Min delay “111111” = Max delay	CMPB_MED_DE L [2:0]
		[4]	WE	—	CMPB_FINE_DEL_WE:	
		[3:0]	RW	0	CMPB_FINE_DEL: Delay value for the compare path de-skew. (~110ps) “000000” = Min delay “111111” = Max delay	CMPB_FINE_DE L [3:0]

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
DRV_FEA	0x1A	[15:14]	R	0	*Reserved (unused):*	
		[13]	WE	—	DAT_FEA_WE:	
		[12:7]	RW	100000	DAT_FEA: Falling edge adjust for compare path de-skew. (~±50ps to ±100ps)	DAT_FEA [5:0]
		[6]	WE	—	EN_FEA_WE:	
		[5:0]	RW	100000	EN_FEA: Falling edge adjust for compare path de-skew. (~±50ps to ±100ps)	EN_FEA [5:0]
CMP_FEA	0x1B	[15:14]	R	0	*Reserved (unused):*	
		[13]	WE	—	CMPB_FEA_WE:	
		[12:7]	RW	100000	CMPB_FEA: Falling edge adjust for compare path de-skew. (~±50ps to ±100ps)	CMPB_FEA [5:0]
		[6]	WE	—	CMPA_FEA_WE:	
		[5:0]	RW	100000	CMPA_FEA: Falling edge adjust for compare path de-skew. (~±50ps to ±100ps)	CMPA_FEA [5:0]
DSKW_CFG	0x1C	[15]	WE	—	DAT_REA_WE:	
DSKW_CFG	0x1C	[14:12]	RW	100	DAT_REA:	DAT_REA [2:0]
		[11]	WE	—	EN_REA_WE:	
		[10:8]	RW	100	EN_REA:	EN_REA [2:0]
		[7]	WE	—	CMPA_REA_WE:	
		[6:4]	RW	100	CMPA_REA:	CMPA_REA [2:0]
		[3]	WE	—	CMPA_REA_WE:	
		[2:0]	RW	100	CMPB_REA:	CMPB_REA [2:0]
DSKW _TEMP	0x1D	[15:8]	—	—	*Reserved (unused):*	
		[7]	WE	—	DSKW_TEMPCO_FUSE_OVRD _WE	
		[6]	RW	0	DSKW_TEMPCO_FUSE_OVRD: This bit selects whether to use the calibrated value stored in fuse memory or override with the value in register DSKW_TEMPCO. Default "0" selects fuse data and "1" selects register data.	DSKW_TEMPCO _FUSE_OVRD
		[5]	WE	—	DSKW_TEMPCO_REG _WE	
		[4:0]	RW	10000	DSKW_TEMPCO_REG: Temperature compensation setting for de-skews.	DSKW_TEMPCO [4:0]
DRV_BIAS	0x1E	[15:10]	—	—	*Reserved (unused):*	
		[9]	WE	—	DRV_BIAS_HV_WE:	
		[8:5]	RW	0	DRV_BIAS_HV: Sets HV driver bias level. 0 = min F = max	DRV_BIAS_HV [3:0]
		[4]	WE	—	DRV_BIAS_HS_WE:	
		[3:0]	RW	0	DRV_BIAS_HS: Sets HS driver bias level. 0 = min F = max	DRV_BIAS_HS [3:0]
RING _PULSE	0x1F	[15:1]	—	—	*Reserved (unused):*	
		[0]	WO_P ULSE	0	RING_PULSE: Writing this bit generates a one-shot pulse (single clock cycle) to initiate oscillations in the ring oscillator. Cleared automatically after pulse in generated.	RING_PULSE
FV_DAC	0x20	[15:0]	RW	0x8000	FV_DAC: The PMU Force Voltage value. -2V to +6V supported range.	FV_DAC
FI_DAC	0x21	[15:0]	RW	0x8000	FI_DAC: The PMU Force Current value.	FI_DAC
DVH_DAC	0x22	[15:0]	RW	0x8000	DVH_DAC: Drive High Voltage reference value. –2V to +6V supported range.	DVH_DAC
DVL_DAC	0x23	[15:0]	RW	0x8000	DVL_DAC: Drive Low Voltage reference value. –2V to +6V supported range.	DVL_DAC
VTT_DAC	0x24	[15:0]	RW	0x8000	VTT_DAC: Drive Termination Voltage reference value. –2V to +6V supported range.	VTT_DAC
CVA_DAC	0x25	[15:0]	RW	0x8000	CVA_DAC: Comparator Threshold A Voltage reference value. –2V to +6V supported range.	CVA_DAC
CVB_DAC	0x26	[15:0]	RW	0x8000	CVB_DAC: Comparator Threshold B Voltage reference value. –2V to +6V supported range.	CVB_DAC
CVA_PMU _MV_DAC	0x27	[15:0]	RW	0x8000	CVA_PMU_MV_DAC: PMU Comparator Threshold A Voltage reference value. –2V to +6V supported range.	CVA_PMU_MV _DAC
CVB_PMU _MV_DAC	0x28	[15:0]	RW	0x8000	CVB_PMU_MV_DAC: PMU Comparator Threshold B Voltage reference value. –2V to +6V supported range.	CVB_PMU_MV _DAC
CVA_DIFF _DAC	0x29	[15:0]	RW	0x8000	CVA_DIFF_DAC: Differential Comparator Threshold A Voltage reference value. –2V to +6V supported range.	CVA_DIFF_DAC

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
CVB_DIFF _DAC	0x2A	[15:0]	RW	0x8000	CVB_DIFF_DAC: Differential Comparator Threshold B Voltage reference value. –2V to +6V supported range.	CVB_DIFF_DAC
ILSRC_DAC	0x2B	[15:0]	RW	0	ILSRC_DAC: Active load sourcing current value. 0 to 24mA supported range.	ILSRC_DAC
ILSNK_DAC	0x2C	[15:0]	RW	0	ILSNK_DAC: Active load sinking current value. 0 to –24mA supported range.	ILSNK_DAC
VTT_ILOAD _DAC	0x2D	[15:0]	RW	0x8000	VTT_ILOAD_DAC: Active load commutating voltage reference value. –2V to +6V supported range.	VTT_ILOAD_DAC
CVA_PMU _MI_DAC	0x2E	[15:0]	RW	0x8000	CVA_PMU_MI_DAC: PMU Comparator Threshold A Voltage reference value. –2V to +6V supported range.	CVA_PMU_MI _DAC
CVB_PMU _MI_DAC	0x2F	[15:0]	RW	0x8000	CVB_PMU_MI_DAC: PMU Comparator Threshold B Voltage reference value. –2V to +6V supported range.	CVB_PMU_MI _DAC
ALARM_CFG	0x33	[15:9]	—	0	*Reserved (unused):*	
		[8]	WE	—	ALARM_MODE_WE:	
		[7]	RW	0	ALARM_MODE: Set the mode for all alarms. Defaults to “0” which is latched mode with clear on read. Set to “1” to set to real time mode (unlatched)	ALARM_MODE
		[6]	WE	—	MASK_WE: These mask bits are used to block an alarm signal from asserting the ALARM_FLAG pin. The mask bits do not block the register from following the state of the alarm signals.	
ALARM_CFG	0x33	[5]	—	0	*Reserved (unused):*	
		[4]	RW	0	MSK_ALARM_PMU_VCL: Set to “1” to mask PMU voltage low clamp alarm.	MSK_ALARM _PMU_VCL
		[3]	RW	0	MSK_ALARM_PMU_VCH: Set to “1” to mask PMU voltage high clamp alarm.	MSK_ALARM _PMU_VCH
		[2]	RW	0	MSK_ALARM_PMU_ICL: Set to “1” to mask PMU negative over current clamp alarm.	MSK_ALARM _PMU_ICL
		[1]	RW	0	MSK_ALARM_PMU_ICH: Set to “1” to mask PMU positive over current clamp alarm.	MSK_ALARM _PMU_ICH
		[0]	RW	0	MSK_ALARM_SHORT: Set to “1” to mask driver shirt circuit protection alarm.	MSK_ALARM _SHORT
ALARM	0x34	[15:6]	—	—	*Reserved (unused):*	
		[5]	—	—	*Reserved (unused):*	
		[4]	RO	0	ALARM_PMU_VCL: Asserted when PMU low voltage clamp is engaged in FI mode.	ALARM_PMU _VCL
		[3]	RO	0	ALARM_PMU_VCH: Asserted when PMU high voltage clamp is engaged in FI mode.	ALARM_PMU _VCH
		[2]	RO	0	ALARM_PMU_ICL: Asserted when PMU negative current clamp is engaged in FV mode.	ALARM_PMU _ICL
		[1]	RO	0	ALARM_PMU_ICH: Asserted when PMU positive current clamp is engaged in FV mode.	ALARM_PMU _ICH
		[0]	RO	0	ALARM_SHORT: Asserted when driver short circuit protection is engaged.	ALARM_SHORT
ALARM _LTCH	0x35	[15:6]	—	—	*Reserved (unused):*	
		[5]	—	—	*Reserved (unused):*	
		[4]	ROL_C LR	0	ALARM_LTCH_PMU_VCL: Asserted when PMU low voltage clamp is engaged in FI mode.	ALARM_LTCH _PMU_VCL
		[3]	ROL_C LR	0	ALARM_LTCH_PMU_VCH: Asserted when PMU high voltage clamp is engaged in FI mode.	ALARM_LTCH _PMU_VCH
		[2]	ROL_C LR	0	ALARM_LTCH_PMU_ICL: Asserted when PMU negative current clamp is engaged in FV mode.	ALARM_LTCH _PMU_ICL
		[1]	ROL_C LR	0	ALARM_LTCH_PMU_ICH: Asserted when PMU positive current clamp is engaged in FV mode.	ALARM_LTCH _PMU_ICH
		[0]	ROL_C LR	0	ALARM_LTCH_SHORT: Asserted when driver short circuit protection is engaged.	ALARM_LTCH _SHORT
ALARM _FORCE	0x36	[15:1]	—	—	*Reserved (unused):*	
		[0]	RW	0	ALARM_FORCE: Set to "1" to manually assert ALARM_FLAG. ALARM_FLAG is the logical OR of all of the alarm bits. If the mode is set to latched, this alarm flag is derived from latched register state and if the mode is real-time then this flag is derived directly from real time signals.	ALARM_FORCE
CMP_STAT	0x37	[15:7]	—	—	*Reserved (unused):*	
		[6]	RO	—	ALARM_FLAG: Reads the current real time state of the ALARM signal from the channel	ALARM_FLAG
		[5]	RO	—	CVA_STAT: State of the comparator A output (single ended and differential)	CVA_STAT
		[4]	RO	—	CVB_STAT: State of the comparator B output (single ended and differential)	CVB_STAT

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
		[3]	RO	—	CVA_PMU_STAT: State of PMU comparator A	CVA_PMU_STAT
		[2]	RO	—	CVB_PMU_STAT: State of PMU comparator b	CVB_PMU_STAT
		[1]	RO	—	EN_STAT: state of the drive enables at the ENA pins	EN_STAT
		[0]	RO	—	DAT_STAT: state of the drive data at the DATA pins	DAT_STAT
PMU_FV _ICH	0x38	[15:13]	—	—	*Reserved (unused):*	
		[12]	WE	—	ICH_IR2m_WE:	
		[11:9]	RW	0	ICH_IR2m: Coarse clamp setting for 2mA range and lower ranges. Used to calibrate clamps to ~3mA for coarse DUT protection.	ICH_IR2m [2:0]
		[8]	WE	—	ICH_IR50m_WE:	
		[7:0]	RW	0	ICH_IR50m: Clamp setting for 50mA range. Can be used to set clamp level across 2mA to 70mA range.	ICH_IR50m [7:0]
PMU_FV_ICL	0x39	[15:13]	—	—	*Reserved (unused):*	
		[12]	WE	—	ICL_IR2m_WE:	
		[11:9]	RW	0	ICL_IR2m: Coarse clamp setting for 2mA range and lower ranges. Used to calibrate clamps to ~3mA for coarse DUT protection.	ICL_IR2m [2:0]
		[8]	WE	—	ICL_IR50m_WE:	
PMU_FV_ICL	0x39	[7:0]	RW	0	ICL_IR50m: Clamp setting for 50mA range. Can be used to set clamp level across 2mA to 70mA range.	ICL_IR50m [7:0]
FV_B_DAC	0x3A	[15:0]	RW	0x8000	FV_B_DAC: The PMU Force Voltage value.	
FV_RTC	0x3B	[15:4]	—	—	*Reserved (unused):*	
		[3]	WE	—	FV_SEL_WE:	
		[2]	RW	0	FV_SEL: When FV_RTC_EN=0, selects what Force Voltage value to use for driving out: - FV_SEL = "0" use FV value - FV_SEL = "1" use FV_B value	
		[1]	WE	—	FV_RTC_EN_WE:	
		[0]	RW	0	FV_RTC_EN: Enables real time switching between FV and FV_B using DAT input pin: - "0" use FV_SEL register to choose FV or FV_B value - "1" use DAT input to choose FV or FV_B value:- DAT="0" use FV value - DAT="1" use FV_B value	

FUSE Memory

TABLE 115: FUSE MEMORY

REG_NAME	REG ADR	BIT	R/W	RESET VALUE	DESCRIPTION	FIELD NAME
FUSE_OUT_15_0	0x98	[15:12]	RO		RO_SINK_HS_FUSE	RO_SINK_HS_FUSE [3:0]
		[11:8]	—		Reserved (unused)	
		[7:4]	RO		RO_SRC_HV_FUSE	RO_SRC_HV_FUSE [3:0]
		[3:0]	RO		RO_SINK_HV_FUSE	RO_SINK_HV_FUSE [3:0]
FUSE_OUT_31_16	0x99	[8:15]	RO		ICH_IR50m_FUSE_TOP	ICH_IR50m_FUSE_TOP [7:0]
		[7:4]	—		Reserved (unused)	
		[3:0]	RO		RO_SRC_HS_FUSE	RO_SRC_HS_FUSE [3:0]
FUSE_OUT_47_32	0x9A	[15:12]	RO		CLL_FUSE_BOT	CLL_FUSE_BOT [3:0]
		[11:8]	RO		OS_DVH_HS_FUSE	OS_DVH_HS_FUSE [3:0]
		[7:4]	RO		OS_DVH_HV_FUSE	OS_DVL_HV_FUSE [3:0]
		[3:0]	RO		OS_DVL_HS_FUSE	OS_DVL_HS_FUSE [3:0]
FUSE_OUT_63_48	0x9B	[15:12]	RO		OS_DVL_HV_FUSE	OS_DVL_HV_FUSE [3:0]
		[11:8]	RO		OS_VTT_HS_FUSE	OS_VTT_HS_FUSE [3:0]
		[7:4]	RO		OS_VTT_HV_FUSE	OS_VTT_HV_FUSE [3:0]
		[3:0]	RO		OS_VTT_ILOAD_FUSE	OS_VTT_ILOAD_FUSE [3:0]
FUSE_OUT_79_64	0x9C	[15:12]	RO		OS_CVA_FUSE	OS_CVA_FUSE [3:0]
		[11:8]	RO		OS_CVB_FUSE	OS_CVB_FUSE [3:0]
		[7:4]	RO		OS_CVA_DIFF_FUSE	OS_CVA_DIFF_FUSE [3:0]
		[3:0]	RO		OS_CVB_DIFF_FUSE	OS_CVB_DIFF_FUSE [3:0]
FUSE_OUT_95_80	0x9D	[15:12]	RO		CLH_FUSE_BOT	CLH_FUSE_BOT [3:0]
		[11:8]	RO		OS_FV_FUSE	OS_FV_FUSE [3:0]
		[7:0]	RO		ICL_IR50m_FUSE_Top	ICL_IR50m_FUSE_Top [7:0]
FUSE_OUT_111_96	0x9E	[15:11]	RO		CLH_FUSE_TOP	CLH_FUSE_TOP [4:0]
		[10:6]	RO		CLL_FUSE_TOP	CLL_FUSE_TOP [4:0]
		[5:3]	RO		ICH_IR2m_FUSE	ICH_IR2m_FUSE [2:0]
		[2:0]	RO		ICL_IR2m_FUSE	ICL_IR2m_FUSE [2:0]
FUSE_OUT_127_112	0x9F	[15:12]	—		Reserved (unused)	
		[11:6]	RO		ICL_IR50m_FUSE_BOT	ICL_IR50m_FUSE_BOT [5:0]
		[5:0]	RO		ICH_IR50m_FUSE_BOT	ICH_IR50m_FUSE_BOT [5:0]

See Table 103 for description of each register.

Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature equation is as follows:

$$TJ = Pd \bullet \theta JA + TA.$$

where:

T_J = Junction Temperature

P_D = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_A = Ambient Temperature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ_{JC}) plus the resistance from the case to ambient (θ_{CA})

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θ_{JA}. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta JA = \theta JC + \theta CA$$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

θJC Thermal Resistance (Junction to Case)

$$\theta JC = 0.096°C/W$$

The thermal resistance of any material is defined by:

$$\theta = (Intrinsic\ material\ resistivity) \bullet Thickness/Area$$

$$or$$

$$\theta = Thickness\ /\ (Intrinsic\ material\ conductivity \bullet Area)$$

Manufacturing

Moisture Sensitivity

Mt. Mystery is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All pre-production and production shipments will undergo the following process post final test:

- Baked @+125°C ±5°C for a duration of ≥ 43 hours.
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto the PCB.

- Product Floor Life ≤168 Hours

Units that exceed this floor life must be baked before being soldered to the PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is load-free.

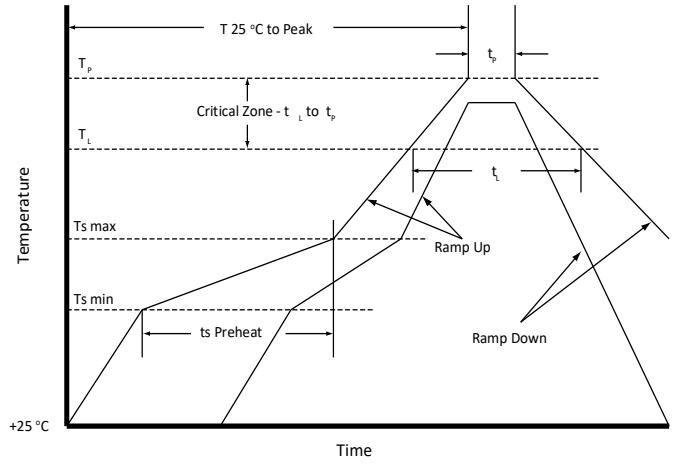


FIGURE 59: SOLDER TIME VS TEMPERATURE

TABLE 116: SOLDER PROFILE

Solder Profile	Pb-Free Assembly
Average ramp up rate (TL to TP)	3°C/sec (max)
Preheat Min Temp (Ts min) Max Temp (Ts max) Time (min to max) (ts)	 150°C 200°C 60 – 180 sec
Ts max to TL - Ramp Up Rate	3°C/sec (max)
Time above Temperature (TL) Time (tL)	 217°C 60 – 150 sec
Peak Temperature (TP)	260°C
Time within 5°C of actual peak temp (tp)	20 sec – 40 sec
Ramp down rate	6°C/sec (max)
Time 25°C to peak temperature	8 minutes (max)

Package Outline Drawing

14mm X 14mm 144 Ball FCBGA (Flip Chip Ball Grid Array)

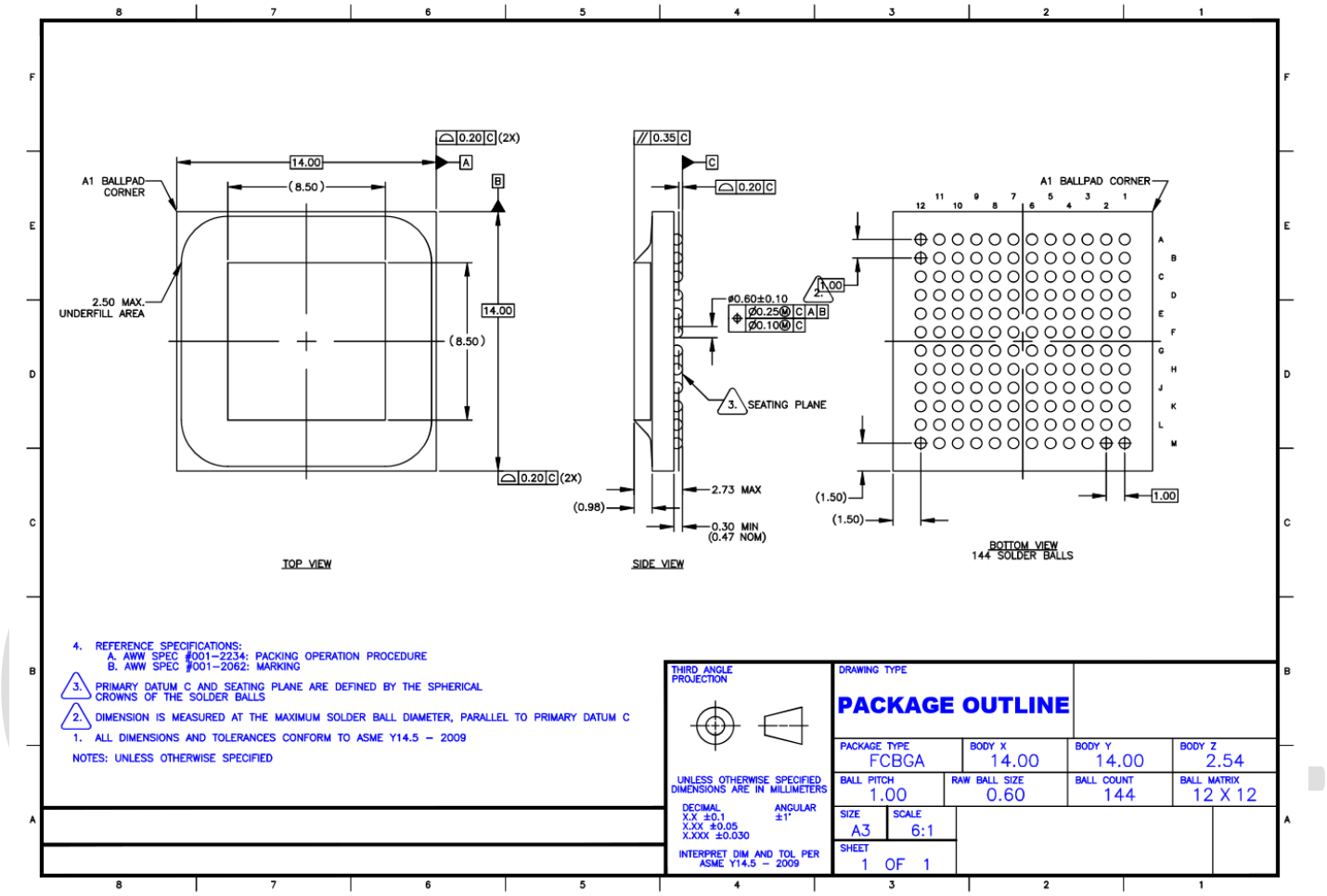


FIGURE 60: PACKAGE OUTLINE DRAWING FCBGA

14mm X 14mm 144 Ball FCCSP (Flip Chip Chip Scale Package)

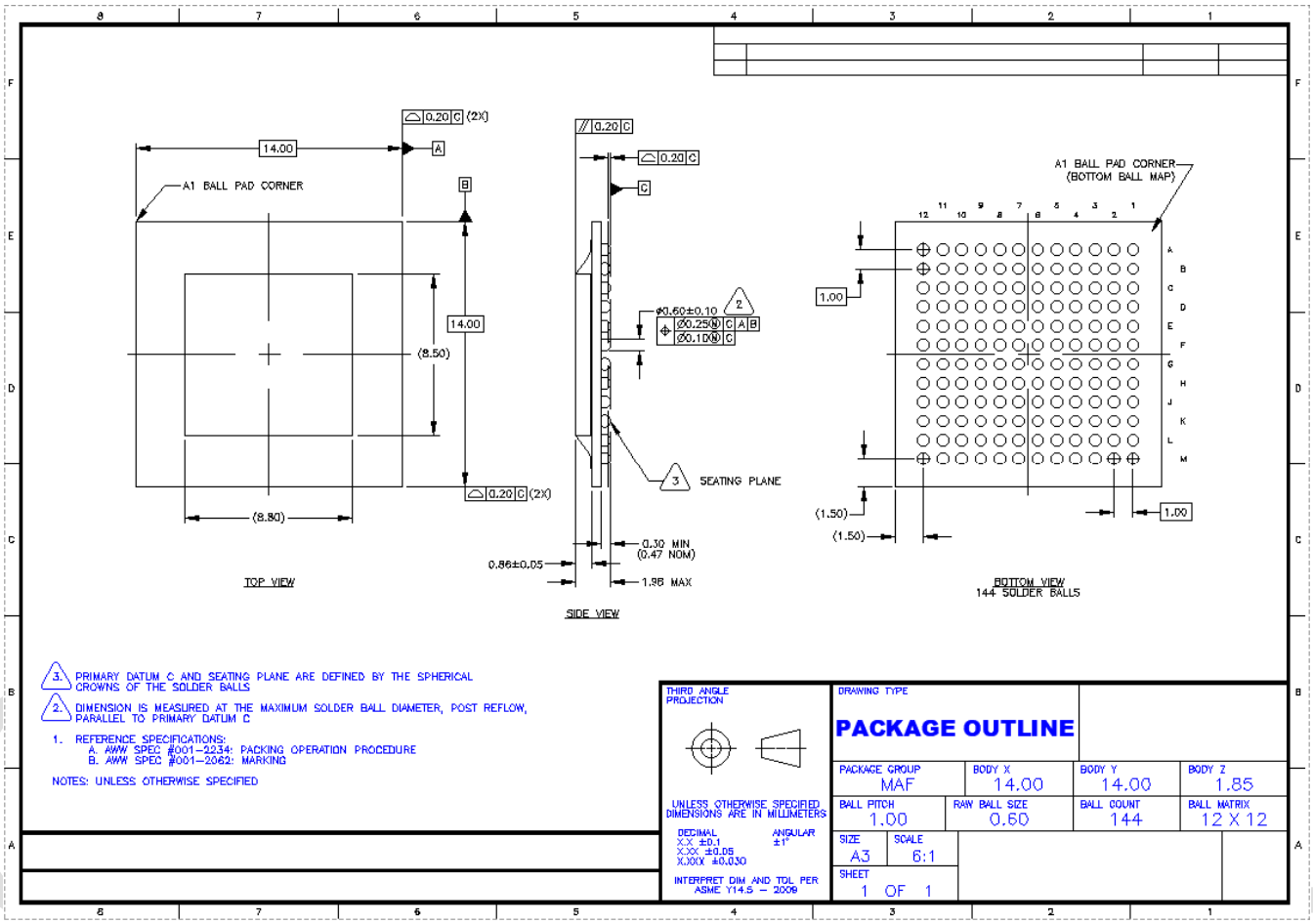


FIGURE 61: PACKAGE OUTLINE DRAWING FCCSP

TABLE 117: REVISION HISTORY

DATE	CHANGE
7/24/2023	• Figure 21: Alarms updated to use RNG[4] instead of RNG[5] to switch between 50mA and 2mA clamp DACs. • Updated EN_STAT and DAT_STAT readback locations. The readback locations are before FDAT[1:0] and FENA[1:0] muxes. • Update the following in the Moisture Sensitivity section: Baked @+125°C ±5°C for a duration of ≥ 43 hours. • Table 74 updated with new values for Force Current transfer function.
2/5/2023	• Updated all instances of PMU_COMP_MODE to read PMU_CMP_MODE • Updated description of GND_REF in Pin Descriptions section. • Added fcCSP package option to datasheet. • Update temperature sensing equation. • Updated ICL_IR50m_FUSE_Top fuse register location in register map. • Changed header to remove Mt. from the title. • Changed PMU_GAIN[3:0] register recommended settings to 0000.
5/18/2022	• Update Figure 16 • Update Table 36 • CRS_DEL section updated. • PMU_ENA table and description updated. • Table 3: R_{RNG_REXT} Changed to R_{RNG_RREF} • Updated active load section to add tables for Active Load Compensation registers. include a description of the Active Load compensation.
11/24/2021	• Added thermal analysis page. • Remove OS_FI DAC. • Update power supply specs and conditions. • Page 18: Change MH0, ML0, MH1, ML1 to MON_0, MON_1, MON_REF_0, MON_REF_1. • Update alarm schematic.
01/29/2021	• Production Release
12/17/2020	• Update specs, tables, figures.
9/19/2019	• Preliminary Release

TABLE 118: PART NUMBER/MARKING

PART NUMBER (NOTE 1)	PART MARKING	TEMP RANGE (°C)	PACKAGE
ELE18MY1-FCT01	ELE18MY	+25 to +100	144 Lead, 14x14mm FCBGA. Note 1
ELE18MY1-CST01	ELE18MY	+25 to +100	144 Lead, 14x14mm FCCSP. Note 1
ELE18MY1A-EVM			Evaluation Board

NOTE:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets), molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020