Whitney Device Guide

Rev G: March 1, 2023

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

Document Revision History

Revision	Date	Description
A	06/17/2021	Initial Draft.
B	08/09/2021	Added recommended sequences for enabling and disabling PMU.
C	08/02/2022	Added warnings section.
D	10/20/2022	Minor corrections and Pin Name Corrections.
E	12/15/2022	Updated recommended sequences with setting FV to 0V prior to changing FF Cap switch state. Removed recommendation for additional external diodes. Corrected Figure 7 from VCCO/VEEO to VCC and VEE. Minor corrections to tables and formatting.
F	01/06/2023	Additional warning (7) for FF Caps and clarified language.
G	03/01/2023	Additional warning for thermal dissipation

Table of Contents

Table of Tables

Table of Figures

1 Introduction

This document describes the steps to perform an initial system check-out of a Whitney device as well as providing workarounds for common problems.

These instructions assume the customer system can set the Whitney supplies, has a mechanism to read/write registers, has the ability to measure voltages (either using an external DMM or system resource), control the digital input pins, and so on. The customer should also be able to adequately cool the Whitney device.

Important Notes:

- Carefully read the Warnings section of this document.
- The steps described below illustrate a cause and effect to demonstrate how to interface with the device. In a normal application sequencing, calibration and other factors may require the registers to be written in a different order.

2 Warnings

Whitney is a high-voltage part with the ability to source significantly over 200mA of current. Special care must be taken when using this product to ensure the safety of the device, board, and user. Please read the following cautions carefully and make sure that the hardware and software comply with the restrictions listed. Failure to adhere to the restrictions below can result in severe damage to the device. Users must read the datasheet and Device Guide thoroughly. In the event of confusion or uncertainty please reach out to the Elevate Applications Team for guidance. For Revision B Silicon see the errata for additional warnings and clarifications.

1. Power supply order MUST be followed exactly. Allow minimum 5mS between supplies. The power up order and minimum time sequence is by default, adhered to by the Whitney EVM power on sequence.

2. Output may NEVER go below VEEO.

3. VSUB must ALWAYS be the lowest supply in the system (as low as VEEO or VEE, whichever is lower).

4. The clamps CANNOT be engaged if the output is already over the clamp limit. Clamps should be set when the part is not outputting (HiZ).

5. Clamps will NOT prevent damage to the Whitney device from an external source, clamps will only limit what the chip itself will try to output. Do not use clamps to limit external current or voltage.

6. Fast transient voltages or currents can damage the output due to a large mismatch between internal and external nodes. Settling time may be needed (or a discharge path) to ensure that there is not a large difference between internal and external voltages.

7. Revision B of this part has feed forward capacitors (FF Caps) that are attached to pins that are 5V tolerant and connected to the VEE and VCC rails. These pins *will* be damaged if they are exposed to transient voltages outside these rails. It is **REQUIRED** for users to ensure that transient spikes are not generated when opening or closing the switch to the FF Cap pins. See Sections 4 and 5 of this document for safe procedures to avoid damaging these pins.

8. Users of the Whitney device must be very aware of power being dissipated in the part at any time and use proper thermal management techniques. See section 3.2 for details. *Even with temperature alarms and automatic tri-state enabled, Whitney can over-heat and the die can be permanently damaged if system designers do not properly implement thermal control*. **Be sure to always track how much power is dissipated in the part** when using the device, especially with large voltage rails and high current modes.

3 Setup

3.1 Set Whitney Supplies

The following restrictions must be met to avoid possible damage to the Whitney device:

1. VEEO => VSUB
2. VEE > VSUB
3. VEE < VGG, VGGA
4. VDD, VDDA > VGG, VGGA
5. VCC > VDD, VDDA
6. VCCO > VCC
7. VEEO < VCCO

Schottky diodes are recommended to protect against violations of the above power supply restrictions. The diodes are intended to protect against power supply failure or an inadvertent power supply sequencing issue. These diodes can be used on a once-per-board basis for all supplies, provided the diode current handling capability is sufficient that the diode forward voltage will not exceed 500mV under worst case conditions. If VCCO_0 and VCCO_1 or VEEO_0 and VEEO_1 use separate supply levels, they should have their own Schottky diodes.

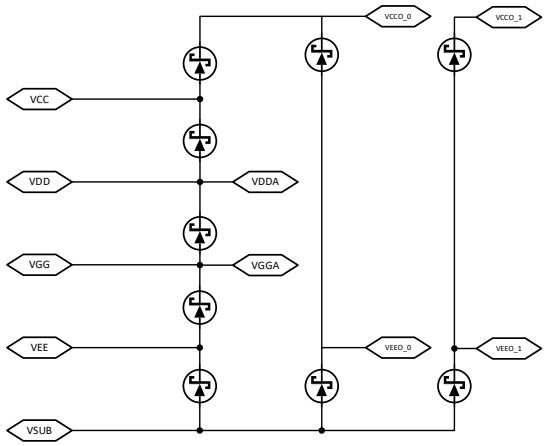

FIGURE 1: DIODE LAYOUT

The first step is to set ENA_0 and ENA_1 to a logic low state. Both enables must remain in a logic low state until the Channel 0 and Channel 1 registers have been initialized to a safe state.

Apply the appropriate supply voltages. After power is applied, it is recommended to toggle the hardware reset (active high) on the Whitney device. Ideally all power supplies would become active simultaneously. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. ENA_# to logic low state (VSS)
2. VSUB
3. VEEO_#
4. VEE
5. VCCO_#
6. VCC
7. VDD/VDDA
8. VREF
   To power down, disable PMU output and reverse the steps 8 to 2
9. Initial registers to safe state
10. ENA_# to logic high state

It is also recommended that additional Schottky diodes be added to several of the pins to prevent transients from damaging the parts. See the Warnings section for more details on how to implement this.

Verify the voltage at the Whitney pins to ensure there are no IR drops. In addition, the customer should verify the approximate current flow for each supply. Table 1 shows some typical current values after a hardware reset has been applied to the part. The example in Table 1 has VCCO_# set to +35V and VSUB/VEEO_# set to -35V, but ICCO, IEEO and ISUB will not vary significantly from this example when lower supply voltages are used.

Note: In some systems, it may not be possible to measure the supply currents on a device-by-device basis.

TABLE 1: POWER-ON CURRENT VALUES AFTER RESET

Supply	Voltage (V)	Approximate Current (mA)
VDD/VDDA	+1.8	38.0
VCC	+2.75	14.0
VEE	-2.75	24.0
VCCO_0	+35	9.0
VCCO_1	+35	9.0
VEEO_0	-35	1.0
VEEO_1	-35	1.0
VSUB	-35	13.0

3.1.1 Measure RREF Pin

The next step is to measure the voltage of RREF. RREF voltage should track the VREF voltage within 25mV.

3.1.2 Read Device ID Register

The following step performs a simple register read access to verify that the CPU port is functioning. Read the DEV_ID register (address = 0x0D80); you should read back a value of 0x0405.

3.1.3 Read Device Revision Register

Read the DEV_REV register (address = 0x0D81). Table 2 lists the expected return values for different silicon revisions. See the Whitney datasheet Register Maps (Global Registers) for a detailed explanation of the DEV_REV bit fields (MAJOR_REV, MINOR_REV, BUILD_REV).

TABLE 2: DIE ID REGISTER VALUES

Rev	Read-back Data (HEX)
A	0x0111
B	0x0211

3.2 Whitney Over-Temperature Protection

Under certain load conditions the Whitney die temperature can quickly rise to excessive levels. Following a reset, the alarms are disabled; to avoid damage to the Whitney device the OVERTEMP Alarm must be enabled by writing 0x0700 to the ALARM_CFG register and writing a “0” to the MSK_ALARM_OVERTEMP bit of the ALARM_CFG register.

Whitney is a device capable of outputting very high power in a short period of time. With 200mA output possible over a 60V range on 2 channels, over 24W can be dissipated on the die in a very small area. This amount of power can be output very quickly and even though Whitney has over-temperature protection, it may not be fast enough to tri-state the PMU before damage can occur if proper heat dissipation techniques are not used. It is the responsibility of the user while ramping power to dissipate heat fast enough to not damage the die.

On-chip thermal diodes and over-temperature protection will help monitor the heat close to the output stage, but there may be a time lag between the increasing die temperature and polling the diode readings. Caution must be taken to ensure that the die does not overheat during this lag. Because this is a system-dependent issue that will vary based on heatsinking and board design, customers must develop their own solutions. This includes designing thermal protection on their boards and using ramp speeds in high-power conditions that will not cause large thermal swings before heat sinking can stabilize the die. It is recommended to ALWAYS use the proper clamping to ensure voltage swings to the rails do not occur. Likewise, large swings can occur when changing from sinking to sourcing current. This can lead to temperature spikes if not handled correctly by returning voltage and current to low settings between sink and source operations. Users should always consider power

dissipated in the part when setting Whitney output levels. Temperatures should be closely monitored, and the over-temperature features and clamps should be used to avoid large thermal swings damaging the device.

Examples: If Whitney is using VCCO=35V / VEEO=-35V in VRNG5 / IRNG 5 and 200mA is being sourced from Channel 0 at 30V, then the part is dissipating 200mA*5V, or 1W of power in a steady state. If the current is changed from sourcing to sinking 200mA before the voltage is changed, then at that time the channel will be dissipating 200mA to VEEO, at 65V difference (30V to -35V) and will quickly spike to 13W on that channel. Depending on the ramp rate of the current change (which would be determined by the system capacitance), the thermal shutdown circuit may not be able to react in time to prevent damage. Likewise, if the output current were to stay sourcing but the voltage changed to -30V quickly, there would again be a 65V difference (-30V to VCCO at 35V) that would cause significant heat to develop over a short period of time. See Figure 2 below:

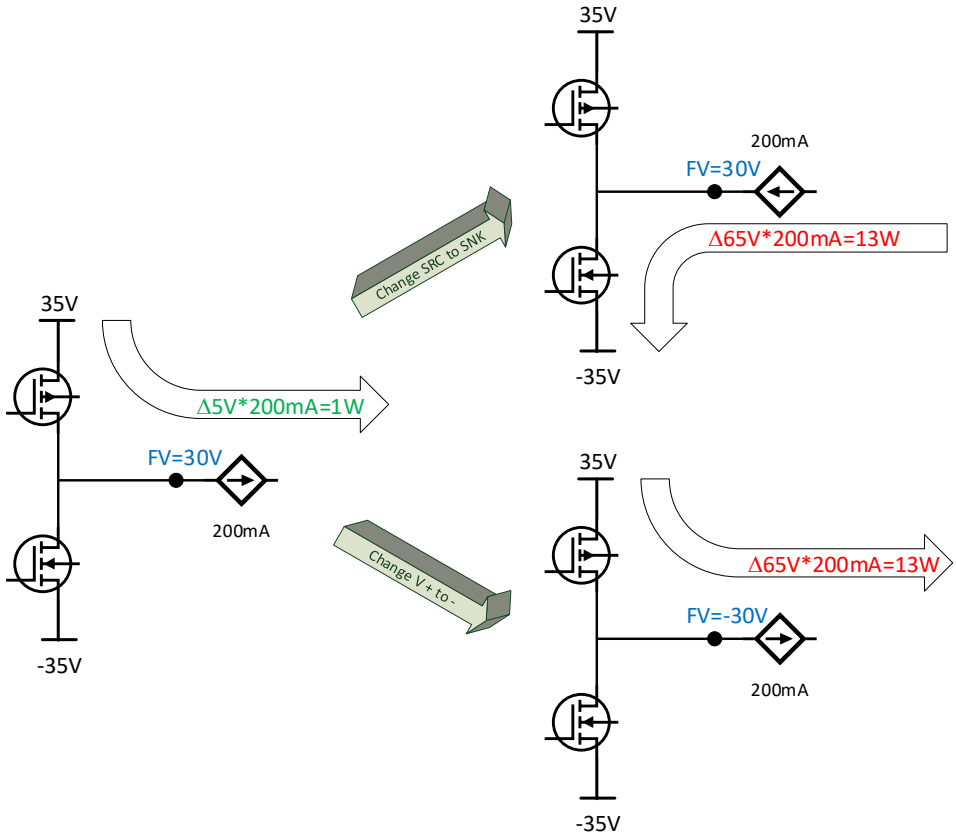

FIGURE 2: POWER INCREASE EXAMPLE FOR THERMAL CONTROL

Thermal management in cases like this is critical for the robust use of the part. Heat dissipation, ramp rate, or tri-stating the PMU are all strategies that should be used to prevent part damage. Excess power dissipation can be managed also by decreasing the VCCO / VEEO rails on Whitney if the large voltage ranges are not needed. This will also increase power efficiency at the system level. It is recommended to closely manage the output rail voltages for both safety and efficiency.=

3.3 MON_TJ_# Load Impedance

The on-chip temperature sensor diode voltages can be read via the MON_TJ_0 and MON_TJ_1 pins. These nodes are high impedance (the pairs of series connected temperature sensor diodes are biased by 1µA current sources) and are not buffered. To minimize measurement errors, the MON_TJ_# load impedance should be => 10MΩ. If the impedance of the voltage measurement resource is less than 10MΩ the MON_TJ_# pins should be externally buffered. Note: A buffer offset voltage of 10mV will cause a temperature measurement error of 5°C. The buffer offset can be measured by setting TEMP_SEL[4:0] to 0x1F (VSS).

Revised thermal diode equation to compensate for the offset voltage of an external MON_TJ_# buffer:

Temperature (°C) = (1.4559 – BUFFER_OFFSET - VTEMP) / 0.004149

For additional examples and explanations, see the datasheet.

3.4 Reset State

Whenever a Hardware or Software reset is issued, the device is configured into the following state. This example shows all registers unique to Channel 0. To read to the corresponding Channel 1 register, set bit 8 of the address (for example, the CH1 PMU_CFG register address is 0x180).

TABLE 3: CH0 RESET REGISTER SETTINGS

Addr (HEX)	Data (HEX)	Register Name	Comments
0x080	0x0000	PMU_CFG	PMU disabled and disconnected
0x081	0x0000	FAST_CLAMP_SNK	
0x082	0x0000	STABILITY	
0x083	0x0000	SLEW	
0x084	0x0001	VRNG	VRNG0
0x085	0x0001	XIRNG	Minimum setting (0x0001)
0x086	0x0001	IRNG	IRNG0
0x087	0x0000	MON_CTRL	MON_A/B_0=HIZ
0x088	0x0000	VTEMP	
0x089	0x0000	CLEAR_OVERTEMP	
0x08A	0x0000	ICLAMP_H	
0x08B	0xFFFF	ICLAMP_L	
0x08C	0x0000	VCLAMP_H	
0x08D	0xFFFF	VCLAMP_L	
0x08E	0xFFFF	FV_A	
0x08F	0xFFFF	FV_B	
0x090	0xFFFF	FI	
0x091	0xFFFF	VCNTR	
0x092	0xFFFF	CVA	
0x093	0xFFFF	CVB	
0x094	0xFFFF	CVA_MI	
0x095	0xFFFF	CVB_MI	
0x096	0x0000	COMP_CFG	
0x097	0x8888	DAC_OS_3	
0x098	0x0088	DAC_OS_2	
0x099	0x8888	DAC_OS_1	
0x09A	0x0000	DAC_MODE	
0x09B	0x8000	FV_A_STOP_VAL	
0x09C	0xFFFF	FV_A_FSM_VAL	
0x09D	0x0000	FV_A_RAMP	
0x09E	0x0000	FV_A_RAMP_TRIG	
0x09F	0x8000	FV_B_STOP_VAL	
0x0A0	0xFFFF	FV_B_FSM_VAL	
0x0A1	0x0000	FV_B_RAMP	
0x0A2	0x0000	FV_B_RAMP_TRIG	
0x0A3	0x8000	FI_STOP_VAL	
0x0A4	0xFFFF	FI_FSM_VAL	
0x0A5	0x0000	FI_RAMP	

Addr (HEX)	Data (HEX)	Register Name	Comments
0x0A6	0x0000	FI_RAMP_TRIG	
0x0A7	0x0000	COMP_STAT	
0x0A8	0x0000	FUSE_BYP	
0x0AA	0x0000	DAC_MODE_BIN	
0x0AF	0x0000	CLAMP_CFG	
0x0B0	0x0088	FAST_CLAMP	
0x0B1	0x0000	PMU_GANGING	
0x0B2	0x0000	ALARM_FORCE	
0x0B3	0x0000	ALARM_LTCH	
0x0B4	0x0000	ALARM	
0x0B5	0x0000	ALARM_CFG	
0x0B6	0x0000	COMP	Must be later set to 0x0001 for proper chip function
0x0B7	0x0000	OUTPUT_ISTATIC	
0x0B8	0x0000	FAST_CLAMP_SRC	
0x0B9	0x0000	KELVIN	
0x0BA	0x0000	SPARE_IN	

3.5 Set a Force Voltage Output on FORCE_L_0

Prior to a hardware or software reset, ENA_0 and ENA_1 (ENA_# hereafter) must be set to a logic low state. Following a hardware or software reset, ENA_# must be set to a logic high state. After this change, ENA_# should not be used to disable or enable the CH0 PMU and CH1 PMU under normal operating conditions. Instead, follow the **Recommended PMU Enable and Disable Sequences** in section 4.

Use the register settings in Table 4 to initialize the CH0 PMU into Force Voltage mode. The FORCE_L_0 pin and SENSE_H_0 pin must be connected external to the Whitney device. This example shows all registers unique to Channel 0. Note that the chip has not been calibrated, so all values show here, and the table below will be approximate. For better accuracy the part must go through full calibration. These registers settings will configure the Whitney device to force 4.2V on the FORCE_L_0 output.

Once the CH0 registers have been initialized to this safe Force Voltage state, follow the Recommended PMU Force Voltage Enable Sequence in section 4.1 to enable the CH0 PMU in Force Voltage mode

To write to the corresponding Channel 1 registers, set bit 8 of the address (for example, the CH1 PMU_CFG register address is 0x180). The FORCE_L_1 pin and SENSE_H_1 pin must be connected external to the Whitney device.

Once the CH1 registers have been initialized to this safe Force Voltage state, follow the Recommended PMU Force Voltage Enable Sequence in section 4.1 to enable the CH1 PMU in Force Voltage mode.

TABLE 4: CH0 FORCE VOLTAGE REGISTER SETTINGS EXAMPLE

Addr (HEX)	Data (HEX)	Register Name	Comments (Data value include WE Bits)
0x080	0xEBBE	PMU_CFG	Mode=FV, FV DAC=FV_A, LOOP enabled, PMU Enabled but not Connected (the CONNECT bit is cleared). Once connected, the PMU will be disconnected if the OVERTEMP alarm is asserted. PMU will NOT be disconnected if the Kelvin alarms are asserted.
0x081	0x0300	FAST_CLAMP_SNK	120% of selected current range
0x082	0x0600	STABILITY	External 1µf feed-forward capacitor enabled
0x083		SLEW	Reserved
0x084	0x0008	VRNG	VRNG3 (±7.5V Force Voltage and Measure Voltage Range when VCNTR=0V)
0x085	0x0001	IRNG	Recommended setting for the 2mA Range
0x086	0x0008	MIRNG	MIRNG3 (2mA Force Current and Measure Current Range)
0x087	0x0CB3	MON_CTRL	MON_A_0=MI, MON_B_0=MV
0x088	0x0462	VTEMP	TEMP_ALARM Threshold = 120 Deg C
0x089	0x0000	CLEAR_OVERTEMP	If the OVERTEMP or Kelvin alarms are asserted, clear the alarm condition, and write “1” to bit 0 of this register to reset the alarm and re-enable the PMU
0x08A	0x011B	ICLAMP_H	+2 mA Clamp
0x08B	0x02E0	ICLAMP_L	-2 mA Clamp
0x08C	0x0052	VCLAMP_H	+7.6V Clamp
0x08D	0x03A5	VCLAMP_L	-7.6V Clamp
0x08E	0xC000	FV_A	This Force Voltage DAC is selected and is the active source for Force Voltage
0x08F	0x0000	FV_B	This DAC is NOT selected
0x090	0x8000	FI	Force Current DAC
0x091	0x7DE3	VCNTR	VCNTR is set to about 0V
0x092	0x909C	CVA	
0x093	0x719D	CVB	
0x094	0x0200	CVA_MI	
0x095	0x0200	CVB_MI	
0x096	0x0254	COMP_CFG	Recommended initial setting
0x097	0x8888	DAC_OS_3	Recommended initial setting
0x098	0x0088	DAC_OS_2	Recommended initial setting
0x099	0x8888	DAC_OS_1	Recommended initial setting
0x09A	0x0240	DAC_MODE	Recommended setting
0x09B	0x8000	FV_A_STOP_VAL	
0x09C	0xC000	FV_A_FSM_VAL	
0x09D	0x0842	FV_A_RAMP	Not Enabled
0x09E	0x0000	FV_A_RAMP_TRIG	
0x09F	0x8000	FV_B_STOP_VAL	
0x0A0	0x0000	FV_B_FSM_VAL	
0x0A1	0x0842	FV_B_RAMP	Not enabled
0x0A2	0x0000	FV_B_RAMP_TRIG	
0x0A3	0x8000	FI_STOP_VAL	
0x0A4	0x8000	FI_FSM_VAL	
0x0A5	0x0842	FI_RAMP	Not enabled

Addr (HEX)	Data (HEX)	Register Name	Comments (Data value include WE Bits)
0x0A6	0x0000	FI_RAMP_TRIG	
0x0A7		COMP_STAT	Read only
0x0A8	0x04FF	FUSE_BYP	Recommended setting
0x0AA	0x0001	DAC_MODE_BIN	Recommended setting
0x0AF	0x00FF	CLAMP_CFG	Accurate Voltage and Current Clamps Disabled
0x0B0	0x0A88	FAST_CLAMP	Fast Current Clamps Enabled
0x0B1	0x8022	PMU_GANGING	PMU Ganging disabled
0x0B2		ALARM_FORCE	Write to this register to manually enforce assertion of Alarms
0x0B3		ALARM_LTCH	Read only
0x0B4		ALARM	Read only
0x0B5	0x0700	ALARM_CFG	Alarms enabled
0x0B6	0x8181	COMP	VCNTR range=1, External 33pf compensation capacitor enabled
0x0B7		OUTPUT_ISTATIC	Reserved
0x0B8	0x0300	FAST_CLAMP_SRC	120% of selected current range
0x0B9	0xC0C0	KELVIN	KELVIN_HIGH alarm +2.8V, KELVIN_LOW alarm -2.8V
0x0BA		SPARE_IN	Reserved

3.6 Enabling and Setting Accurate Current Clamps

In this example, Whitney CH0 is set to Force Voltage in the 20mA range. The FV_A Digital Ramp is used to control the FV slew rate; the digital ramp FV_A step size is set to 9. The voltage range is VRNG3. For the Current Clamps to work properly, the Voltage Clamps must also be enabled. The Voltage Clamps are set to ±5V, and the Accurate Current Clamps are set to ±15mA. Again, pre-calibration all values will be approximate.

The resistive load is the impedance of a 50Ω oscilloscope input. Only the register settings that differ from Table 4 (Reset condition) are shown.

TABLE 5: REGISTER SETTINGS TO ENABLE FORCE VOLTAGE MODE AND SET ACCURATE CURRENT CLAMPS

Addr (HEX)	Data (HEX)	Register Name	Comments (Data value include WE Bits)
0x082	0x0500	STABILITY	External 100nf feed-forward capacitor enabled
0x085	0x000E	XIRNG	Recommended setting for the 20mA Range
0x086	0x0010	IRNG	IRNG4 (20mA Force Current and Measure Current Range)
0x08A	0x01B7	ICLAMP_H	ICH=+15mA
0x08B	0x0235	ICLAMP_L	ICL=-15mA
0x08C	0x00CD	VCLAMP_H	VCH=+5V
0x08D	0x032A	VCLAMP_L	VCL=-5V
0x09B	0x59D4	FV_A_STOP_VAL	FV = -2.5V
0x09B	0xA72A	FV_A_STOP_VAL	FV = +2.5V
0x09D	0x0867	FV_A_RAMP	Force Voltage Ramp Enabled, FV_A Step Size = 9
0x0AF	0x00AA	CLAMP_CFG	Accurate Voltage and Current Clamps Enabled

TABLE 6: REGISTER SETTINGS TO DISABLE ACCURATE VOLTAGE AND CURRENT CLAMPS

Addr (HEX)	Data (HEX)	Register Name	Comments (Data value include WE Bits)
0x0AF	0x00FF	CLAMP_CFG	Accurate Voltage and Current Clamps Disabled

Sequence to duplicate the Figure 3 and Figure 4 waveforms (Current Clamps Enabled):

1. Update the Whitney CH0 registers to the Table 5 settings
2. Write 0x59D4 (-2.5V) to the FV_A_STOP_VAL register
3. Write 0x0001 to the FV_A_RAMP_TRIG register to trigger the Force Voltage Ramp
4. Set the oscilloscope trigger @ 0V, rising edge
5. Write 0xA72A (+2.5V) to the FV_A_STOP_VAL register
6. Write 0x0001 to the FV_A_RAMP_TRIG register to trigger the Force Voltage Ramp
7. Set the oscilloscope trigger @ 0V, falling edge
8. Write 0x59D4 (-2.5V) to the FV_A_STOP_VAL register
9. Write 0x0001 to the FV_A_RAMP_TRIG register to trigger the Force Voltage Ramp

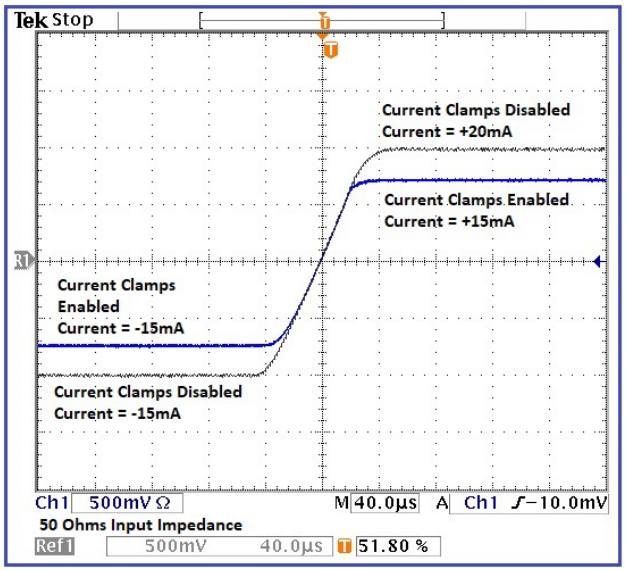

FIGURE 3: FORCE VOLTAGE RISING EDGE WITH CURRENT CLAMPS DISABLED AND ENABLED

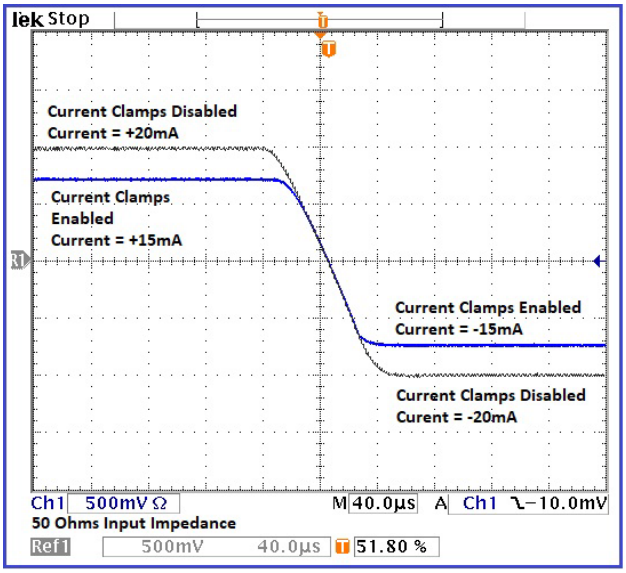

FIGURE 4: FORCE VOLTAGE FALLING EDGE WITH CURRENT CLAMPS DISABLED AND ENABLED

3.7 Enabling and Setting Force Current Mode and Accurate Voltage Clamps

In this example, Whitney CH0 is set to Force Current in the 20mA range. The recommended PMU disable sequence must be followed prior to changing the mode from Force Voltage to Force Current. The FI Digital Ramp is used to control the FI slew rate; the digital ramp FI step size is set to 11. The voltage range is VRNG3. For the Voltage Clamps to work properly, the Current Clamps must also be enabled. The Voltage Clamps are set to ±2V and the Current Clamps are set to ±25mA. Note that when the voltage clamps are enabled the compensation capacitance must be increased from 33pf to 220pf.

The resistive load is the impedance of a 50Ω oscilloscope input. Only the register settings that differ from Table 4 (The reset table) are shown.

TABLE 7: REGISTER SETTINGS TO ENABLE FORCE CURRENT MODE AND SET ACCURATE VOLTAGE CLAMPS

Addr (HEX)	Data (HEX)	Register Name	Comments (Data value include WE Bits)
0x080	0xEBFE	PMU_CFG	Mode=FI, FV DAC=FV_A, LOOP enabled, PMU Enabled but not Connected (the CONNECT bit is cleared). PMU will be disconnected if the OVERTEMP alarm is asserted. PMU will NOT be disconnected if the Kelvin alarms are asserted.
0x082	0x0500	STABILITY	External 100nf feed-forward capacitor enabled
0x085	0x000E	XIRNG	Recommended setting for the 20mA Range
0x086	0x0010	IRNG	IRNG4 (20mA Force Current and Measure Current Range)
0x08A	0x018C	ICLAMP_H	ICH=+25mA
0x08B	0x0260	ICLAMP_L	ICL=-25mA
0x08C	0x0187	VCLAMP_H	VCH=+2V
0x08D	0x0272	VCLAMP_L	VCL=-2V
0x0A3	0x6D6C	FI_STOP_VAL	FI = -20mA
0x0A3	0x96D2	FI_STOP_VAL	FI = +20mA
0x0A5	0x086F	FI_RAMP	Force Current Ramp Enabled, FI Step Size = 11
0x0AF	0x00AA	CLAMP_CFG	Accurate Voltage and Current Clamps Enabled
0x0B6	0x8281	COMP	VCNTR range=1, External 220pf compensation capacitor enabled

Sequence to duplicate the Figure 5 and Figure 6 waveforms (Voltage Clamps Enabled):

1. Set the CONNECT bit of the PMU_CFG register to 0
2. Update the Whitney CH0 registers to the Table 7 settings
3. Write 0x6D6C (-20mA) to the FI_STOP_VAL register
4. Write 0x0001 to the FI_RAMP_TRIG register to trigger the Force Current Ramp
5. Set the CONNECT bit of the PMU_CFG register to enable the PMU output
6. Set the oscilloscope trigger @ 0V, rising edge
7. Write 0x96D2 (+20mA) to the FI_STOP_VAL register
8. Write 0x0001 to the FI_RAMP_TRIG register to trigger the Force Current Ramp
9. Set the oscilloscope trigger @ 0V, falling edge
10. Write 0x6D6C (-20mA) to the FI_STOP_VAL register
11. Write 0x0001 to the FI_RAMP_TRIG register to trigger the Force Current Ramp

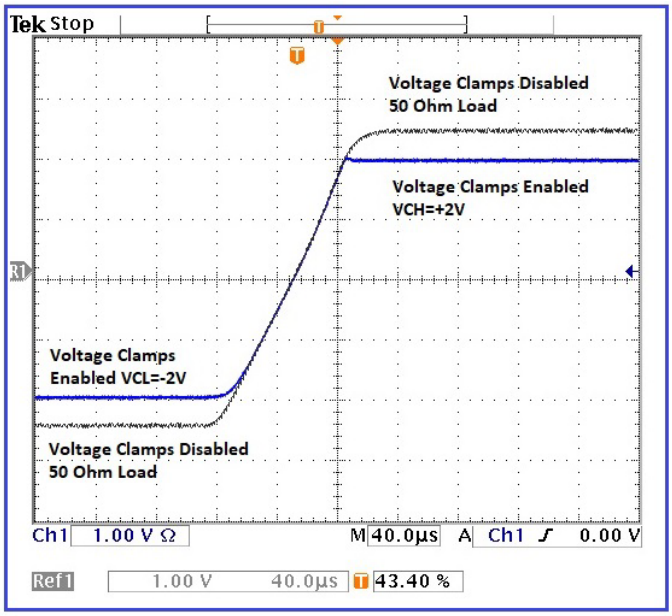

FIGURE 5: FORCE CURRENT RISING EDGE WITH VOLTAGE CLAMPS DISABLED AND ENABLED

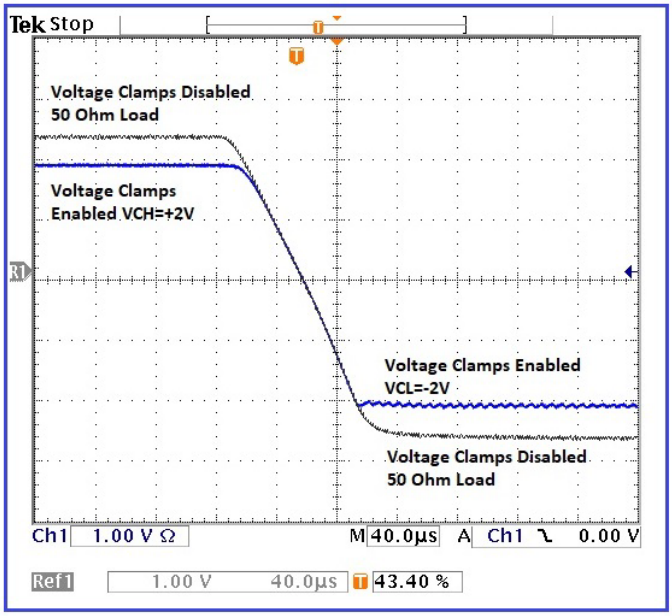

FIGURE 6: FORCE CURRENT FALLING EDGE WITH VOLTAGE CLAMPS DISABLED AND ENABLED

4 Recommended PMU Enable and Disable Sequences

When the PMU is disabled, all selected external compensation capacitors will be charged to the VCC rail (typically +2.65V). This is not an issue with the smaller value compensation capacitors (for example, 33pf) because they discharge very quickly. However, if the PMU is enabled with the external 47nf compensation capacitor charged to VCC the PMU output will be driven to the VCCO_# rail. The following recommended sequences are designed to minimize over-shoot and under-shoot when enabling and disabling the PMU. The ENA_0 and ENA_1 pins must remain set to a logic high during normal operation. Using the ENA_# pins to enable or disable the PMU can cause undesirable behavior.

Note: The Whitney datasheet recommends the use of an OPTO-SW to disconnect the feed-forward capacitors from the low-current outputs FORCE_L_0 and FORCE_L_1 when using the 2µA and 20µA current ranges (refer to Figure 7). This will significantly reduce the Measure Current and Force Current settling time. Failing to follow these recommendations can cause a transient high voltage across the pins and damage the Whitney device.

4.1 Enable PMU, Force Voltage Mode

Set IRNG to 200µA prior to enabling the PMU to achieve a consistent turn-on behavior, then set the desired current range.

1. Close OPTO-SW to connect feed-forward capacitors to the FORCE_L_# output (refer to Figure 7)
2. Select 100nf FF cap
3. Select 33pf COMP cap
4. Set XIRNG=1
5. Set IRNG to 200µA
6. Set CONNECT bit high to enable PMU
7. Set XIRNG to the recommended setting for the desired current range (See Errata for Rev B silicon).
8. Set IRNG to the desired current range
9. Select the recommended COMP cap for the desired current range (refer to Figure 7)
10. If the current range is 2µA or 20µA, OPTO-SW will be open on next step: Set FV to 0V. Prior to opening OPTO-SW, PMU output should be zero volts.
11. Select the recommended FF cap for the desired current range (refer to Figure 7)

4.2 Disable PMU, Force Voltage Mode, 2µA and 20µA Current Ranges

Set IRNG to 200µA prior to disabling the PMU to achieve a consistent turn-off behavior (also ensures that the 47nf COMP capacitor is not selected when the PMU is disabled).

1. If OPTO-SW is currently open: Set FV to 0V. Prior to closing OPTO-SW, PMU output should be zero volts.
2. If OPTO-SW is currently open: Select 100nf FF cap and 1µ FF cap.
3. Close OPTO-SW to connect feed-forward capacitors to the FORCE_L_# output (refer to Figure 7)
4. Select 100nf FF cap
5. Select 33pf COMP cap
6. Set IRNG to 200µA
7. Clear the CONNECT bit to disable PMU

4.3 Disable PMU, Force Voltage Mode, 200µA, 2mA, 20mA, and 200mA Current Ranges

Set IRNG to 200µA prior to disabling the PMU to achieve a consistent turn-off behavior.

1. Set XIRNG=1
2. Set IRNG to 200µA
3. Set FF cap to 100nf
4. Clear the CONNECT bit to disable PMU

4.4 Enable PMU, Force Current Mode, 2µA and 20µA Current Ranges

1. Do not use the PMU Mode = FI in the 2µA and 20µA ranges

4.5 Enable PMU, Force Current Mode, 200µA, 2mA, 20mA, 200mA Current Ranges

Enable PMU

1. Close OPTO-SW to connect feed-forward capacitors to the FORCE_L_# output (refer to Figure 7)
2. Select the recommended FF cap for the desired current range (refer to Figure 7)
3. Select the recommended COMP cap for the desired current range (refer to Figure 7)
4. Set XIRNG to the recommended setting for the desired current range (See Errata for Rev B silicon)
5. Set IRNG to the desired current range
6. Set CONNECT bit high to enable PMU

4.6 Disable PMU, Force Current Mode, 2µA and 20µA Current Ranges

1. Do not use the PMU Mode = FI in the 2µA and 20µA ranges

4.7 Disable PMU, Force Current Mode, 200µA, 2mA, 20mA, 200mA Current Ranges

Disable PMU

1. Write 0x8000 to the FI register to set Force Current to minimum
2. Close OPTO-SW to connect feed-forward capacitors to the FORCE_L_# output (refer to Figure 7)
3. Select 100nf FF cap
4. Select 220pf COMP cap
5. Clear the CONNECT bit to disable PMU

4.8 Changing from FV to FI

1. Disable PMU, Force Voltage Mode (see section 4.2 or section 4.3)
2. Enable PMU, Force Current Mode (see section 4.4 or section 4.5)

5 Recommended Sequence for Changing Current Ranges

5.1 Change Current Range Force Voltage Mode, only 2µA to 20µA or 20µA to 2µA

1. Set IRNG to the desired current range
   Note: No need to Close OPTO-SW which requires setting FV to 0V.

5.2 Change Current Range Force Voltage Mode, any change other than 5.1 (2mA to 2µA, 2mA to 20mA, etc.)

1. If OPTO-SW is currently open: Set FV to 0V. Prior to closing OPTO-SW, PMU output should be zero volts.
2. If OPTO-SW is currently open: Select 100nf FF cap and 1µ FF cap.
3. Close OPTO-SW to connect feed-forward capacitors to the FORCE_L_# output (refer to Figure 7)
4. Select the 100nf FF cap
5. Select the 33pf COMP cap
6. Set XIRNG to the recommended setting for the desired current range (See Errata for Rev B silicon)
7. Set IRNG to the desired current range
8. Select the recommended COMP cap for the desired current range (refer to Table 8)
9. Select the recommended FF cap for the desired current range (refer to Table 8)
10. If the current range is 2µA or 20µA, OPTO-SW will be open on the next step, Set FV to 0V. Prior to opening OPTO-SW, PMU output should be zero volts.
11. If the current range is 2µA or 20µA, open OPTO-SW to disconnect feed-forward capacitors from the FORCE_L_# output (refer to Figure 7)

5.3 Change Current Range, Force Current Mode

1. Close OPTO-SW to connect feed-forward capacitors to the FORCE_L_# output (refer to Figure 7)
2. Select the 100nf FF cap
3. Select the 220pf COMP cap
4. Set XIRNG to the recommended setting for the desired current range (See Errata for Rev B silicon)
5. Set IRNG to the desired current range
6. Select the recommended COMP cap for the desired current range (refer to Table 8)
7. Select the recommended FF cap for the desired current range (refer to Table 8)
8. If the desired current range is 2µA or 20µA, do not enter this current range in Force Current mode.

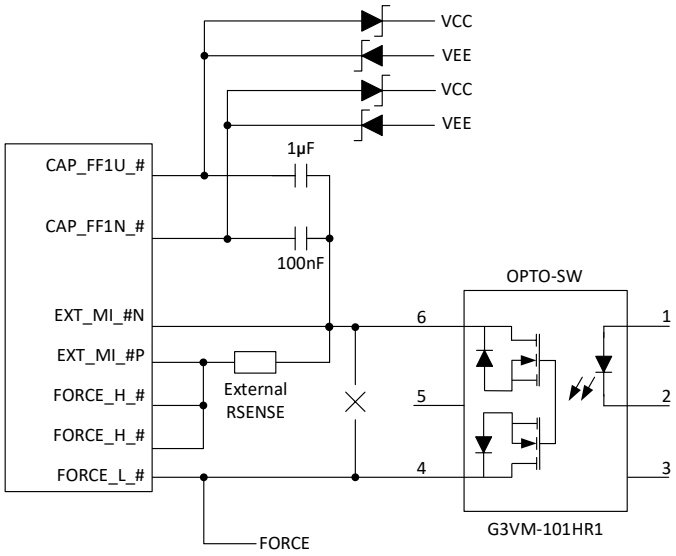

FIGURE 7: FEED FORWARD CLAMPING DIODES AND OPTIONAL OPTO-SW

TABLE 8: RECOMMENDED COMP AND FF CAP VALUES

	Compensation Capacitance						Feed-Forward Capacitance					
	2µA	20µA	200µA	2mA	20mA	200mA	2µA	20µA	200µA	2mA	20mA	200mA
FV	47nf	47nf	33pf	33pf	33pf	33pf	0nf	0nf	100nf	1µf	1µf	1µf
FI	47nf	47nf	220pf	33pf	33pf	33pf	0nf	0nf	100nf	1µf	1µf	1µf

6 Conclusion

6.1 Additional Support

For any additional support, please refer to the Datasheet, EVM Guide, or Calibration Guide. If you require applications support, please reach out by email to support@elevatesemi.com or submit a question on Zendesk.