

Vesuvius EVM Getting Started

Rev A2: 06/26/17



This document contains information on a product under development and the material is subject to change.

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1 Introduction

Congratulations on your purchase of an Elevate Semiconductor Vesuvius evaluation system. You will find that it serves as an invaluable development platform to help get your product to market in the shortest possible time. The Vesuvius and Graphical User Interface (GUI) allow the customer to demonstrate and evaluate the Vesuvius performance and functionality.

This document provides the instructions to install, setup, and operate the Vesuvius EVM. Refer to the *Elevate Semiconductor EVM User's Guide* for a detailed description of the EVM system.

1.1 Unpacking - Vesuvius EVM Contents

Please check the contents of the Vesuvius EVM shipping carton to make sure you have received all of the items listed in Table 1. The system is already configured for the best setup, except for connections to the power supply, PC controller, and test equipment.

Table 1: Vesuvius EVM Contents

Qty	Description
1 ea.	Vesuvius EVM System (3 boards: Motherboard, FVMI Board, Vesuvius Loadboard)
1 ea.	Vesuvius EVM Getting Started (this document)
1 ea.	EVM Contents List
1 ea.	Elevate Semiconductor User Interface Program Installation Flash Drive
1 ea.	USB A/B Cable

1.2 Recommended Test and Measurement Setup

1.2.1 Power Supply

Table 2 provides the required power supplies and current rating. The power supplies are connected using standard banana plugs. The customer needs to provide the power supply cables and supplies.

It is recommended to use a triple supply to control the EVM supplies. This allows the 3 EVM supplies to be turned on at the same time. However, if this is not feasible, then the supplies should be enabled in the following sequence. Power down should be performed in the reverse order.

1. +20V
2. -15V
3. +5V

The Vesuvius VCCO and VEE are gated using an Opto-FET switch on the loadboard so it is safe to set and enable the Vesuvius supplies before powering up the EVM and running the software.

Table 2: Power Supply Requirements

Module	Supply	Current Rating
Motherboard	+20V	0.5 A
Motherboard	+5V ⁽¹⁾	0.5 A
Motherboard	-15V	0.5 A
Vesuvius VCCO	+5V ^(2, 3)	5.0 A ⁽⁴⁾
Vesuvius VEE	-3V ^(2, 3)	5.0 A ⁽⁴⁾

Notes:

- 1) The EVM +5V could also be used as the Vesuvius VCCO
- 2) Once the EVM operation is verified, the customer can adjust the VCCO, VEE supplies
- 3) Make sure the external supplies do not violate the ABS max section on the datasheet.
- 4) The VCCO and VEE current 4A requirements are required if all 8 channels are operating at maximum current load. If using a sub-set of channels then a smaller (i.e. 1 Amp) supply could be adequate. The program does not have the ability to measure the VCCO and VEE currents

1.2.2 PC Controller

To use the Vesuvius EVM User Interface Program (UIP), a PC with the following configuration is required:

- Windows 2007, Windows 2008, Windows 2010
- USB Port (a USB cable is provided)

1.2.3 DMM or Source Measurement Unit

- Voltage and/or Current Meter
- Voltage and/or Current Source

1.3 Software Installation

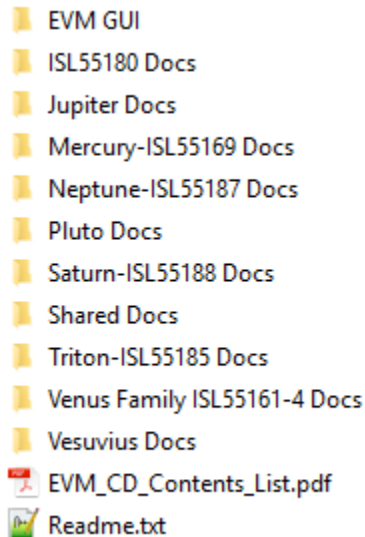
There are 2 steps to install the Vesuvius EVM demonstration program.

1. Install the Vesuvius EVM UIP from the Flash Drive.
2. Install the USB driver.

Figure 1 illustrates the default directory structure. The user may change the <root dir> during the installation.

Figure 1: Installation Directory Structure

<Root Dir>:\ElevATE Semi



1.3.1 Vesuvius EVM UIP Installation

To install the Vesuvius EVM software package, run the SETUP program on the distribution Flash Drive and follow the prompts. The **ElevATE.exe** executable will be installed in the **EVM GUI** sub-directory. In addition, a short cut will be installed onto the desktop and in the **Start->Programs** folder. The **Start->Programs** folder also contains links to the different EVM User's Guide, and documentation folders.

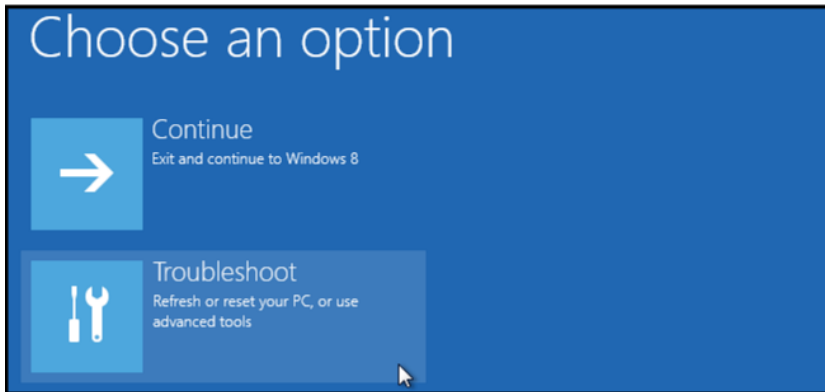
1.3.2 USB Device Driver Installation

Follow section 1.3.2.1 for installation instructions on the Windows 10/8 operating systems, section 1.3.2.2 for instructions for Windows 7, or section 1.3.2.3 for Windows XP

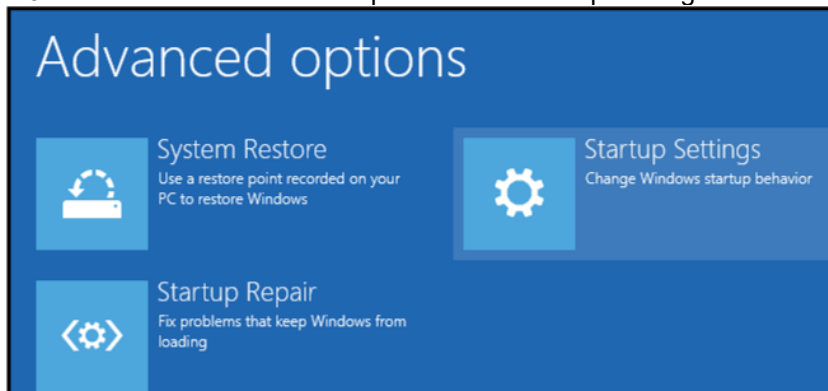
1.3.2.1 Window 10/8

To install the USB driver on Windows 10/8, the Driver Signature Verification needs to be disabled. This is accomplished using the following method.

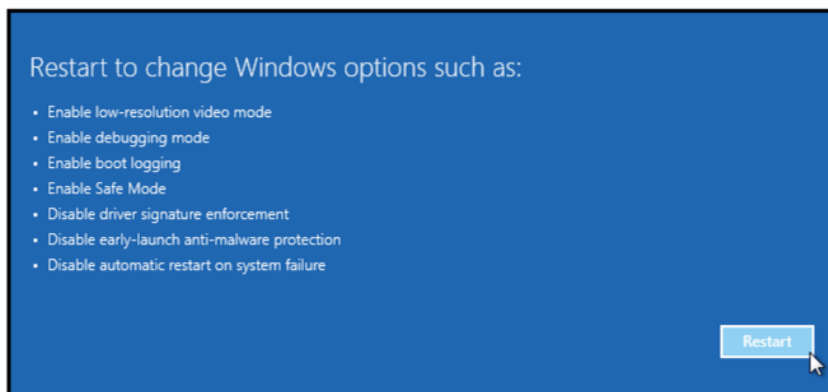
- 1.3.2.1.1 Enter the Troubleshoot menu. Click "Restart" from the power options menu and hold down the "Shift" key at the same time. Once the computer has rebooted, you will be able to choose the Troubleshoot option.



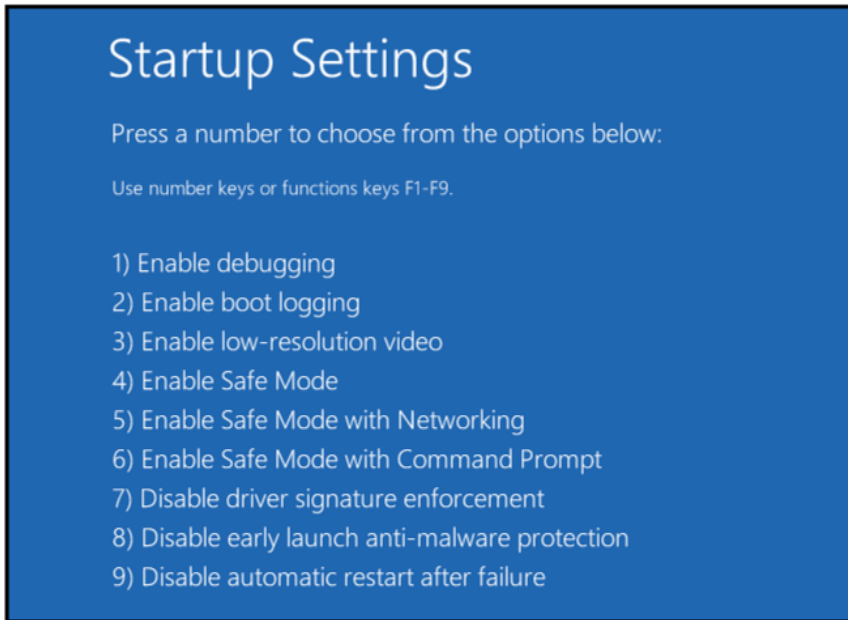
1.3.2.1.2 Select “Advanced options” and “Startup Settings”.



1.3.2.1.3 You need to restart your computer one last time to modify boot time configuration settings.



1.3.2.1.4 You will be given a list of startup settings, including “Disable driver signature enforcement”. To choose the setting, you need to press the “F7” key. This will disable the driver signature enforcement until the computer is rebooted.

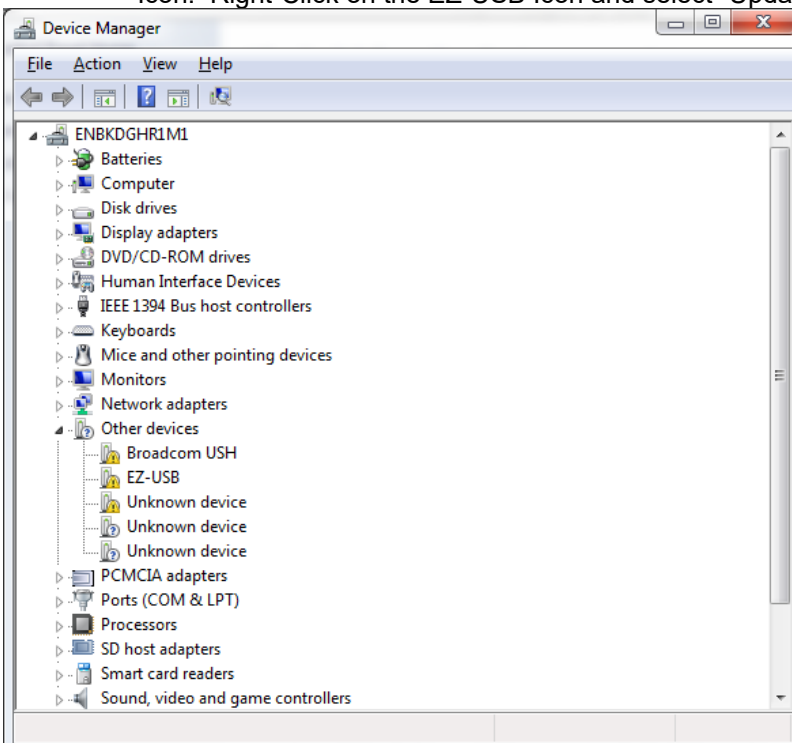


1.3.2.1.5 Continue with section 1.3.2.2 to finish installation of USB driver except choose the windows 10 or windows 8 option.

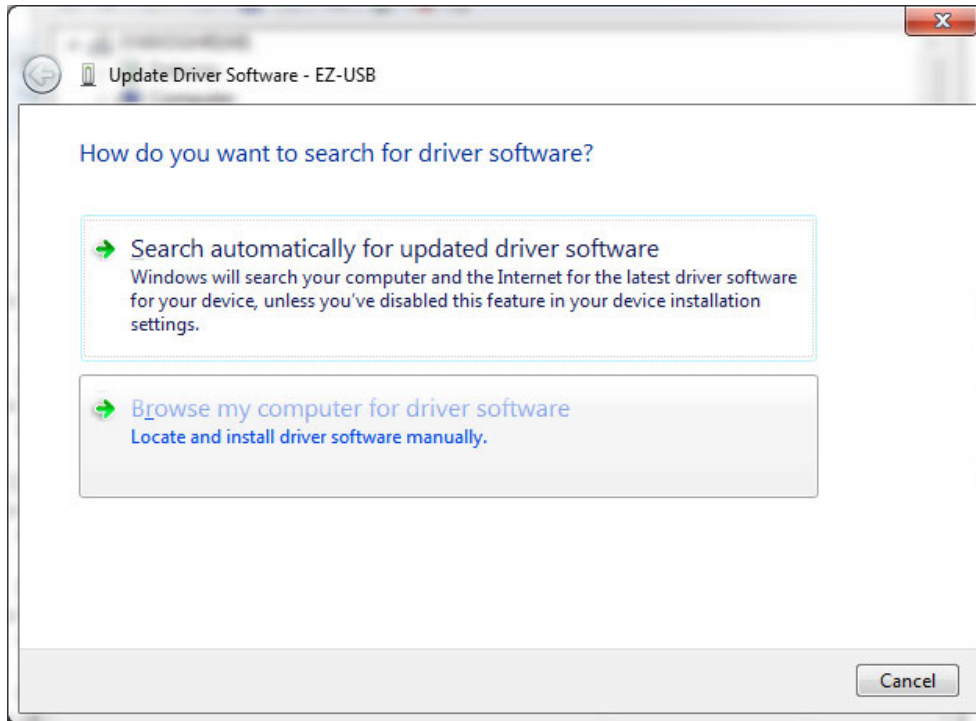
1.3.2.2 Windows 7

To install the USB device driver on a Windows 7 system, connect the USB port using the included USB A/B cable. The USB port does not need any external power or need to be connected to any other board for the device driver installation.

1.3.2.2.1 After connecting the USB cable from the PC to the “USB FX2 to Parallel” board, navigate to the Device Manager screen on your computer and look for the EZ-USB icon. Right-Click on the EZ-USB icon and select “Update Drive Software...”



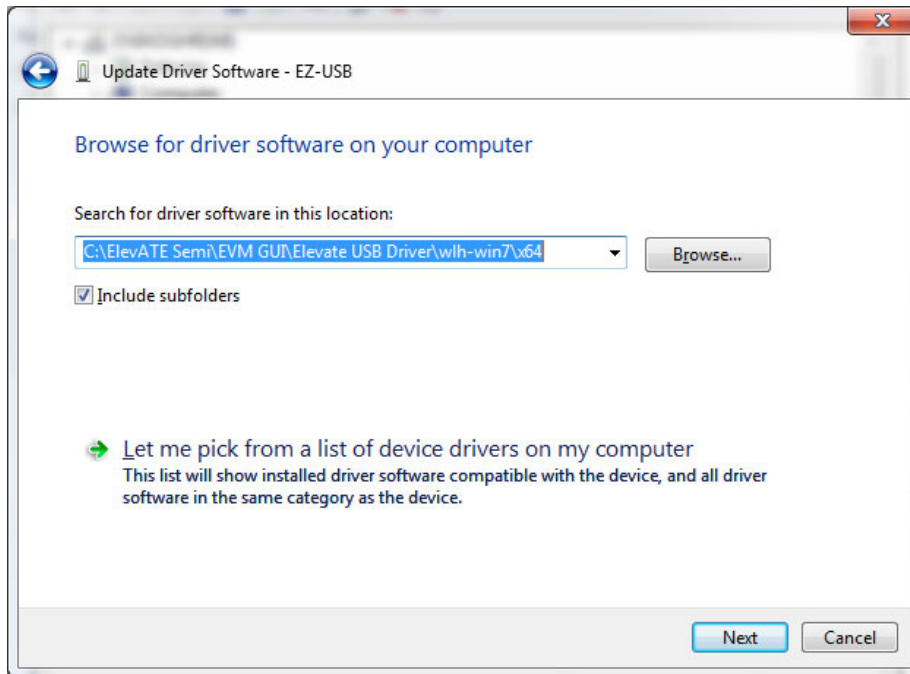
1.3.2.2.2 Select “Browse my computer for driver software”.



1.3.2.2.3 Install driver from the newly installed folder on your computer:

Windows 7: `\\ElevATE Semi\EVM GUI\Elevate USB Driver\wlh-win7\`(x64 or x86)
Select x64 for a 64-bit system.
Select x86 32-bit system.

Select “Next”. The USB driver will be installed.



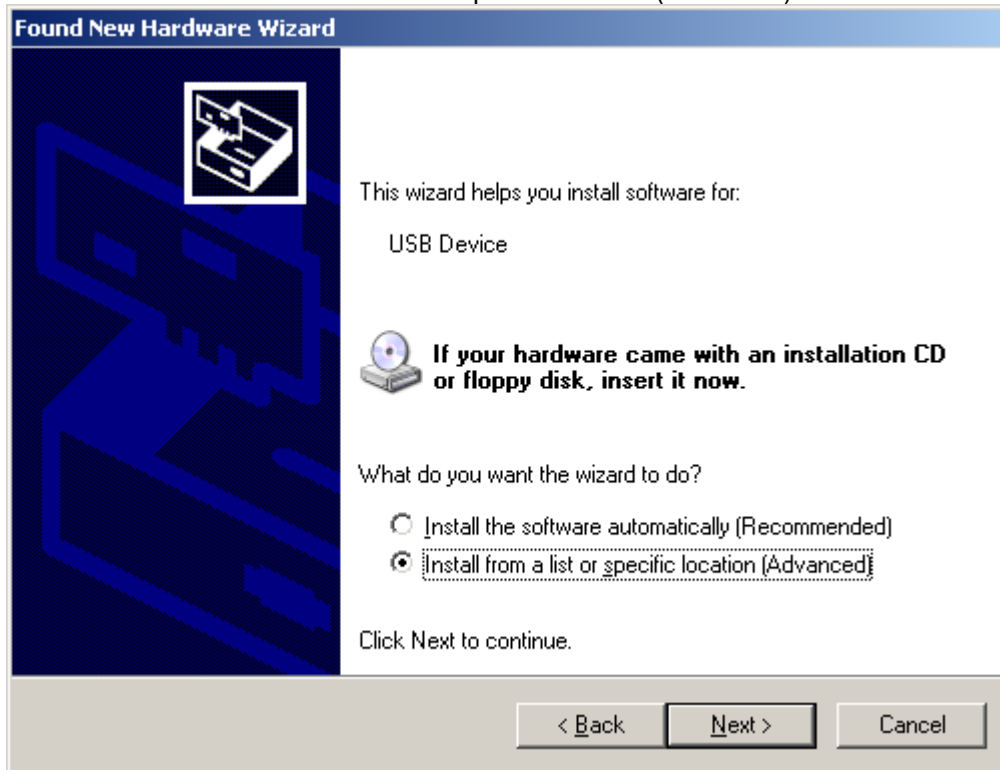
1.3.2.3 Windows XP

To install the USB device driver on a Windows XP system, connect the USB port using the included USB A/B cable. The USB port does not need any external power or need to be connected to any other board for the device driver installation.

1.3.2.3.1 After connecting the USB cable from the PC to the USB port, the following window appears. Select “No, not this time” and click Next.



1.3.2.3.2 Choose “Install from a list or specific location (Advanced)” and click Next.



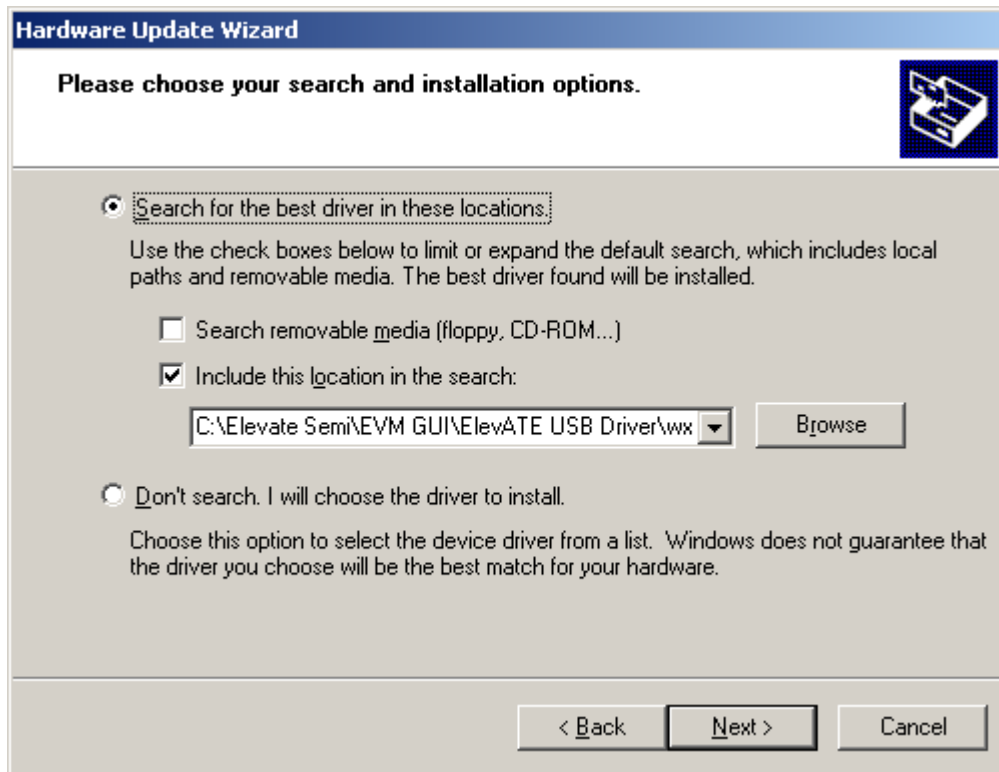
1.3.2.3.3 Select the top radio button, and check “Include this location in the search.” Type the following path into the text box.

Windows XP: **\\ElevATE Semi\EVM GUI\Elevate USB Driver\wxp**(x64 or x86)

Select x64 for a 64-bit system.

Select x86 32-bit system.

Select “Next”. The USB driver will be installed.



1.3.3 Reboot Machine

After the Vesuvius EVM and USB software is installed, it may be required to re-boot the machine.

1.3.4 Launching the Elevate Semiconductor Program

The user can launch the Elevate Semiconductor GUI from the **Desktop**, **Start->Programs** folder, or *Elevate SemiEVM GUI* sub-directory.

1.3.5 Software Un-Installation

The Elevate Semiconductor demonstration program may be un-installed using the **Add/Remove Program** from the Windows Control Panel.

2 Getting Started

The Vesuvius is shipped in a pre-configured state that allows a customer to evaluate the DPS Force Voltage/Measure Current (FV/MI), Ganging and other features.

Note: Any external equipment providing digital signals into the Vesuvius device should only be enabled after the Vesuvius is enabled. Also, the external equipment should be disabled prior to disabling the Vesuvius.

2.1 Caution

The Vesuvius DUT Power Supply (DPS) is capable of delivering several amps of current. Configuring the Vesuvius device and EVM into an extremely high power condition could cause permanent damage to the Vesuvius device, EVM components, and/or external equipment.

2.2 Quick Start Instructions

2.2.1 Default Power Supply Option

1. Disable external power supply
2. Connect the power supplies cables (not provided) from the power supply to the Elevate Semiconductor EVM Motherboard and Vesuvius loadboard; refer to Figure 3.
3. Connect the USB cable (provided) from the PC to the USB port.
4. Connect the EVM to any external equipment; refer to Section 2.3. Verify any external equipment is disabled prior to connecting to the EVM board.
5. Setup Motherboard Jumpers; refer to Section 2.4
6. Ensure Vesuvius Loadboard Jumpers E2 – E10 and E14 are shorting pins 1 and 2 (towards back of board).
7. Set external power supply voltages and current limits.
8. Enable external power supply.
9. Run the Elevate Semiconductor GUI software.
10. At the Force Voltage – Measure Current dialog box (refer to Figure 2 below):
 - a. Select the **EVM Setup** option based on the desired configuration, see Section 2.3
 - b. Select the **Enable Supplies** check box
 - c. Hit the **Apply** button to power up the Vesuvius device.
 - d. The software will also measure the current consumption. Figure 2 illustrates the expected current readings.
11. At this point, the Vesuvius should be outputting the desired signal.

Figure 2: Expected Current Readings

Force Voltage - Measure Current (FVMI) Configuration
✕

Revision
Vesuvius Rev 1
LB SN = 103
FVMI SN = 303

Reset
 Must issue whenever power is cycled on board. Will put system into default state.

PLL Freq (MHz)
PLL_CK
CLK_REF

PLL Present

Device Options
EVM Setup Calibrate DAC Calibrate Levels
Only applied when supplies transition to Enabled state

Enable Supplies

Power Amplifiers	Desired Voltage	Meas Voltage	Current (mA)	Power (mW)
Ch 1 (VCCO PS) (+0.0 to +13.0)	<input type="text" value="5.000"/>	<input type="text" value="5.000"/>	<input type="text" value="3.0"/>	<input type="text" value="15.0"/>
Chan 2 (VCC) (+3.3 to +15.0)	<input type="text" value="13.000"/>	<input type="text" value="13.000"/>	<input type="text" value="103.6"/>	<input type="text" value="1346.9"/>
Chan 3 (VDD) (0.0 to +5.0)	<input type="text" value="3.300"/>	<input type="text" value="3.298"/>	<input type="text" value="67.5"/>	<input type="text" value="222.7"/>
Chan 4 (VEE) (-5.0 to +0.0)	<input type="text" value="-3.000"/>	<input type="text" value="-3.000"/>	<input type="text" value="106.0"/>	<input type="text" value="318.0"/>
Chan 5 (VOH) (+0.0 to +3.3)	<input type="text" value="3.300"/>	<input type="text" value="3.299"/>	<input type="text" value="0.4"/>	<input type="text" value="1.4"/>
Chan 6 (VF) (-10.0 to +15.0)	<input type="text" value="0.000"/>	<input type="text" value="0.000"/>	<input type="text" value="0.0"/>	<input type="text" value="0.0"/>
Chan 7 (VREF) (+2.5 to +3.5)	<input type="text" value="3.000"/>	<input type="text" value="3.000"/>	<input type="text" value="0.0"/>	<input type="text" value="0.0"/>

Europa/Switcher EVM

VCCOB (Ch3-0)

VCCOA (Ch7-4)

SYNC (kHz)

FSEL (divider)

Enable Switcher (Must Remove E4 and E5)

Total

Perform Range Check
 Servo Supplies

The **Reset System** will put the EVM and Vesuvius device into the default state. The **Reset System** should be issued whenever the power supply is powered OFF then ON. The **Reset System** is automatically performed when the program is initially launched.

2.3 Default Configuration Setup Options

The EVM has several default options for configuring for device and loadboard.

Table 3: Vesuvius Default Configuration Options

Mode	See Section #	Brief Description
Hardware Reset	N/A	All registers default to the hardware default state.
Three-State (High-Z)	N/A	Puts DPS in three-state (high-Z). Opens all switches.
FV/MI	2.3.2 (default)	All Channels configured in FV/MI mode with I-Clamps disabled. VFA = 3.0V, IR5, Sel-FB = SENSE, Con-FS = 1 Ch#0 FORCE and SENSE connected to TEST_NODE
FI/MV		Channel 0 configured in FI/MV mode with the Voltage Clamps enable. VFI = 51mA, IR5, Ch#0 FORCE connected to TEST_NODE. 2 Ohm resistor connected to test node. VCH = 3.0V. VCL = -1.0V.
Ch#0/1 Ganging	2.3.4	All Channels (except Ch#1) configured in FV/MI mode with I-Clamps disabled. Ch#1 configured into FV-Slave mode Ch#0 VFA = 3.0V, IR5, Sel-FB = SENSE, Con-FS = 1 Ch#0 FORCE and SENSE connected to TEST_NODE Ch#1 FORCE connected to TEST_NODE
Ch#0-7 Ganging	2.3.4	Ch#0 configured in FV/MI mode with I-Clamps disabled. Channels#1-7 configured into FV-Slave mode Ch#0 VFA = 3.0V, IR5, Sel-FB = SENSE, Con-FS = 1 Ch#0 FORCE and SENSE connected to TEST_NODE Channel#1-7 FORCE connected to TEST_NODE
Gang Mode With Slave Device		Dut 1 Ch#0 configured in FV/MI mode with I-Clamps disabled. Channels#1-7 configured into FV-Slave mode. Dut 2 Ch#0-7 configured in FV-Slave mode. Ch#0 VFA = 3.0V, IR5, Sel-FB = SENSE, Con-FS = 1 Ch#0 FORCE and SENSE connected to TEST_NODE Channel#1-7 FORCE connected to TEST_NODE

2.3.1 Remote Kelvin Sense

Caution should be used when configuring the feedback (SENSE) path to ensure the DPS does not become open loop. The software defaults the CPU-Sel-FB = 2 (SENSE) and Con-FS# = 1 (closed) to ensure the loop is closed. After connecting any external equipment to the FORCE/SENSE SMAs (or TEST_NODE), the user can then set Con-FS#=0 (open) to provide remote Kelvin sensing.

2.3.2 FV/MI Configuration

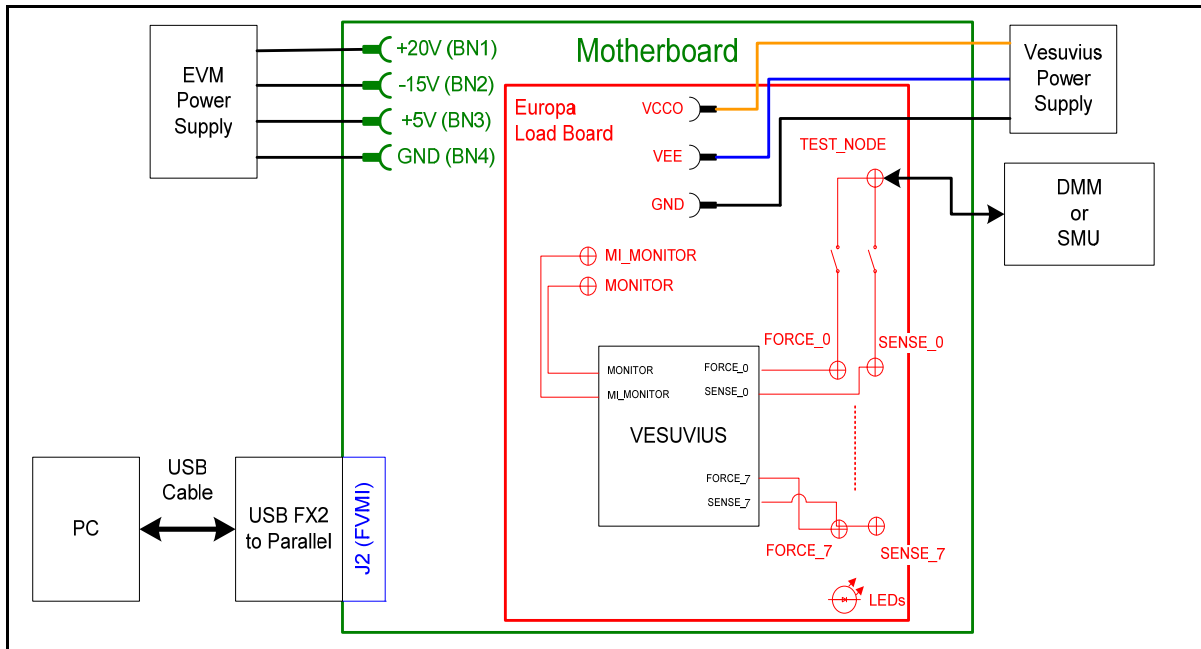
Figure 3 illustrates the recommended configuration for FV/MI (Force Voltage/Measure Current). After the configuration is completed, use the **Vesuvius->Master->Channel#0->Levels** dialog box to change the Vesuvius output levels. Use the **Vesuvius Loadboard** dialog box to connect other channels to the TEST_NODE.

Both MI_MONITOR and MONITOR are configured to output Ch0/Ch1 MI-S

If using an external source measurement unit (SMU), the SMU should be configured in the opposite mode as Vesuvius.

Vesuvius	SMU
FV/MI	FI/MV
FI/MV	FV/MI

Figure 3: Vesuvius EVM FV/MI Simplified Block Diagram



2.3.3 FI/MV Configuration

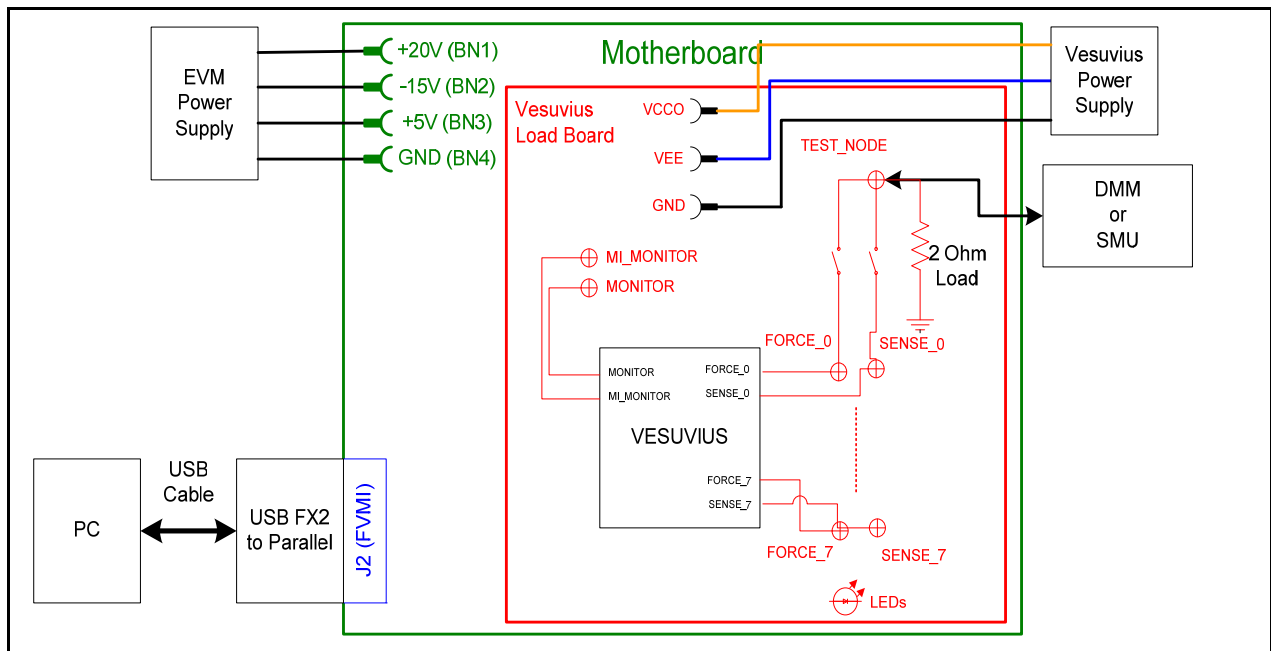
Figure 4 Illustrates the recommended configuration for FI/MV (Force Current/Measure Voltage). After the configuration is completed, use the **Vesuvius->Master->Channel#0->Levels** dialog box to change the Vesuvius output levels. Use the **Vesuvius Loadboard** dialog box to connect or disconnect resistors and capacitors to the FORCE output.

The MONITOR is configured to measure the voltage between the FORCE output and GROUND. This voltage is used for the Voltage Clamps (VCH/VCL)

If using an external source measurement unit (SMU), the SMU should be configured in the opposite mode as Vesuvius.

Vesuvius	SMU
FV/MI	FI/MV
FI/MV	FV/MI

Figure 4: Vesuvius EVM FI/MV Simplified Block Diagram



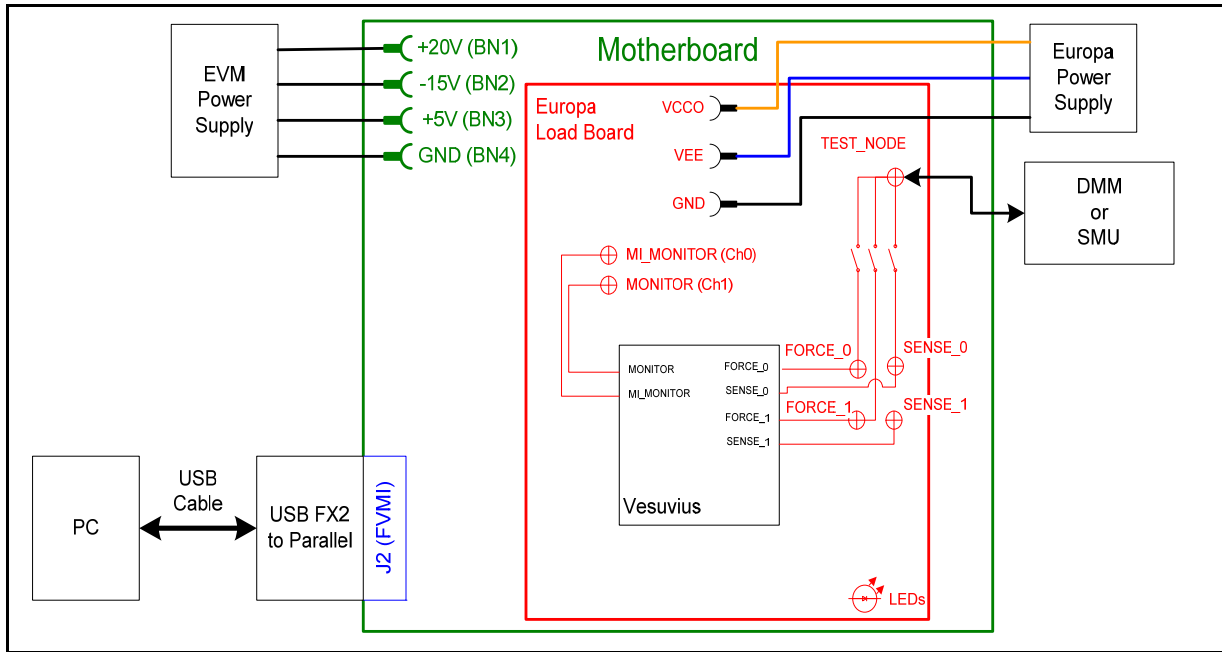
2.3.4 Channel#0 and Channel#1 Ganging (Merging) Configuration

5 illustrates the recommended configuration for the ganging application. Channel#0 is configured in FV mode (Master) in Remote Sense while Channel#1 is configured in FV (Slave) mode. Both Channel#0 and Channel#1 FORCE pins are connected to the TEST_NODE SMA. Channel#0 SENSE is also connected to TEST_NODE which provides the remote Kelvin Sense return path.

The MI_MONITOR is configured to output the Channel#0 MI-S. The MONITOR is configured to output the Channel#1 MI-S.

Channels 2-7 are configured in FV/MI mode.

Figure 5: Vesuvius EVM Ganging Configuration Simplified Block Diagram



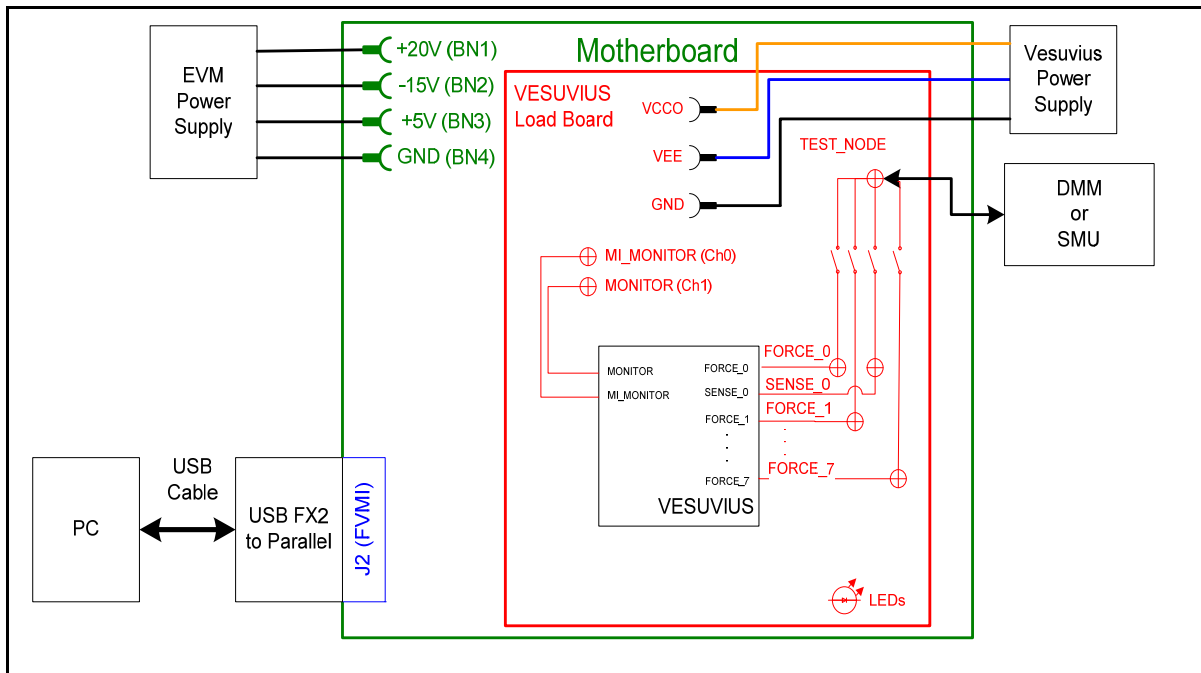
2.3.5 All channels in Ganged (Merging) Configuration

5 illustrates the recommended configuration for the ganging application of all channels. Channel#0 is configured in FV mode (Master) in Remote Sense while Channels#1-7 are configured in FV (Slave) mode. Channel#0-7 FORCE pins are connected to the TEST_NODE SMA. Channel#0 SENSE is also connected to TEST_NODE which provides the remote Kelvin Sense return path.

The MI_MONITOR is configured to output the Channel#0 MI-S. The MONITOR is configured to output the Channel#1 MI-S.

Channels 2-7 are configured in FV/MI mode.

Figure 6: Vesuvius EVM All Channels Ganging Configuration Simplified Block Diagram



2.4 Motherboard Jumper and SMA Definition

Table 4 lists the Motherboard Jumper/SMA definitions for the Vesuvius EVM.

Table 4: Motherboard SMA and Jumper Definitions (Vesuvius Input Signals)

TC#	Jumper	Usage	Configuration
TC30	E12	PLL_CK (Fsync)	Short Pin 1 & 2. towards back of board
TC29	E11	PLL_CK* (Fsync)	Short Pin 1 & 2. towards back of board
TC28	E14	TJ (V)	Short Pin 2 & 3. towards front of board
TC27	E15	EXT_MON_OE	Short Pin 1 & 2. towards back of board
TC26	E2	EN	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC25	E10	SLAVE_RESET	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC24	E9	SLAVE_STB	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC23	E8		Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC22	E7	DIG_BANK_SEL	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC21	E1	SDI_RCK	Short Pin 1 & 2. towards back of board
TC20	E6	DATA_3/DATA_7	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC19	E5	DATA_2/DATA_6	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC18	E4	DATA_1/DATA_5	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC17	E3	DATA_0/DATA_4	Short Pin 1 & 2: source from latch Short Pin 2 & 3: source from SMA
TC16	E13	N/A	Don't care
TC15	E20	N/A	Don't care

The following table defines the Vesuvius output signals. These are always present at the motherboard SMAs.

Table 5: Motherboard SMA Definitions (Vesuvius Output Signals)

TC#	MB EVM
TC14	OT*
TC13	ALARM*
TC12	Unused
TC11	GANG_IN_SLAVE
TC10	CPU_CK
TC9	GANG7_OUT
TC8	GANG5_OUT
TC6	GANG3_OUT
TC5	GANG1_OUT
TC4	RESET
TC3	CPU_STB
TC2	CPU_SDIO

2.5 Vesuvius Loadboard Jumper Definitions

Table 4 lists the Vesuvius Loadboard Jumper definitions.

Table 6: Vesuvius Loadboard Jumper Definitions

Jumper	Description	Default Configuration
E1	Connect VFORCE	Installed
E2/4/5/6/9	VCCO Select	Pin 1 & 2. Select BN1
E3/7/8/10/14	VEE Select	Pin 1 & 2. Select BN2
E16/17/18	Dynamic load configuration	Not Installed
E19/20/21/22	Gang1_OUT Master to Gang#_IN Slave	Not Installed
J21	Slave FORCE_0-FORCE_7 Connected to Gang Force Node	Not Installed
J7	Master FORCE_0-FORCE_7 and SENSE_0-SENSE_7 Connected to Gang Force Node	Not Installed
J12	Slave Device Measurement Points	Do Not Install

2.6 Vesuvius EVM Menu and Dialog Boxes

6 illustrates the Vesuvius EVM menu options that provide access to the Vesuvius dialog boxes. For each Vesuvius register, there is a control field allowing the customer to have full control over the Vesuvius device. These screen shots show the default *FV/MI* configuration.

Figure 7: Device Configuration Menu Options

```

Elevate Evaluation Program
File Edit View EVM Config Venus Pluto Mercury Neptune Jupiter Saturn Triton ISL55180 Vesuvius Window Test Help Burn-In FX2 to Parallel

MV Path=0: MV.gain = 1.333942 ; MV.offset = 1.4980
MV Path=1: Volt(0.5) = 0.7325, 0.4658
MV Path=1: Volt(3.5) = 2.2425, 3.4856
MV Path=1: MV.gain = 0.500030 ; MV.offset = 0.4996
MV Path=2: Volt(-1.0) = 0.7380, -1.0437
MV Path=2: Volt(5.0) = 2.2498, 4.9948
MV Path=2: MV.gain = 0.250365 ; MV.offset = 0.9993
MV Path=3: Volt(-1.0) = 0.6186, -1.0438
MV Path=3: Volt(11.0) = 2.1309, 11.0258
MV Path=3: MV.gain = 0.125298 ; MV.offset = 0.7494
Calibrating DAC#0...
mv1=-0.0191, mv2=4.0267, span=4.0459, lsb_step=0.123mV
Bit D13: Code=0 ; MV1=-1.0300 ; MV2 = -1.0304 ; Step = -0.57mV ; low=-8 ; high=8
Bit D13: Code=4 ; MV1=-1.0302 ; MV2 = -1.0300 ; Step = 0.10mV ; low=0 ; high=8
Bit D13: Code=2 ; MV1=-1.0298 ; MV2 = -1.0307 ; Step = -1.02mV ; low=0 ; high=4
Bit D13: Code=3 ; MV1=-1.0300 ; MV2 = -1.0302 ; Step = -0.35mV ; low=2 ; high=4
Dev0, Ch#0, Dac#0, CalBit D13: code=4
Bit D14: Code=0 ; MV1=-0.0180 ; MV2 = -0.0194 ; Step = -1.47mV ; low=-16 ; high=16
Bit D14: Code=8 ; MV1=-0.0187 ; MV2 = -0.0185 ; Step = 0.10mV ; low=0 ; high=16
Bit D14: Code=4 ; MV1=-0.0180 ; MV2 = -0.0191 ; Step = -1.24mV ; low=0 ; high=8
Bit D14: Code=6 ; MV1=-0.0182 ; MV2 = -0.0185 ; Step = -0.35mV ; low=4 ; high=8
Bit D14: Code=7 ; MV1=-0.0182 ; MV2 = -0.0185 ; Step = -0.35mV ; low=6 ; high=8
Dev0, Ch#0, Dac#0, CalBit D14: code=8
Bit D15: Code=0 ; MV1=2.0073 ; MV2 = 2.0008 ; Step = -6.62mV ; low=-32 ; high=32
Bit D15: Code=16 ; MV1=2.0055 ; MV2 = 2.0021 ; Step = -3.48mV ; low=0 ; high=32
Bit D15: Code=24 ; MV1=2.0046 ; MV2 = 2.0032 ; Step = -1.47mV ; low=16 ; high=32
Bit D15: Code=28 ; MV1=2.0041 ; MV2 = 2.0037 ; Step = -0.57mV ; low=24 ; high=32
Bit D15: Code=30 ; MV1=2.0041 ; MV2 = 2.0039 ; Step = -0.35mV ; low=28 ; high=32
Bit D15: Code=31 ; MV1=2.0037 ; MV2 = 2.0035 ; Step = -0.35mV ; low=30 ; high=32]
Dev0, Ch#0, Dac#0, CalBit D15: code=30
Dac0, Seg0: Volt(-0.8208) = -0.8754
Dac0, Seg0: Volt(-0.4752) = -0.5042
VR2) Dac0, Seg0: Offset.gain = 1.074172 ; Offset.offset = 0.0063
Dac0, Seg1: Volt(-0.3888) = -0.4104
Dac0, Seg1: Volt(-0.0432) = -0.0410
VR2) Dac0, Seg1: Offset.gain = 1.068989 ; Offset.offset = 0.0052
Dac0, Seg2: Volt(0.0432) = 0.0551
Dac0, Seg2: Volt(0.3888) = 0.4256
VR2) Dac0, Seg2: Offset.gain = 1.072228 ; Offset.offset = 0.0088
Dac0, Seg3: Volt(0.4752) = 0.5185
Dac0, Seg3: Volt(0.8208) = 0.8879
VR2) Dac0, Seg3: Offset.gain = 1.068989 ; Offset.offset = 0.0105
Dac0, Seg0: Volt(5.0500) = 5.2263

```

Ready NUM

Figure 8: Vesuvius Configuration Dialog Box

Vesuvius (Dev=0) Channel#0 Configuration

Forcing Path

FI/FV* Voltage

F# Select ForceA

(Sel-RT-D# & CPU-D#)

Sel-VForce FV (F# Select)

Feedback / Measure Path

Tight-Loop* FB#

Sel-V-FB SENSE

Sel-Diag Tj-Sensor

Sel-MU-Pos MI-S

Sel-MU-Neg FI-Zero

Current Clamps and Alarms

I-Cl-En

Sel-MI4 MI-IR5

Sel-MI-Cl MI-IR4/5

Sel-Cl-Al RT-Cl

Cl-Al-En CPU-OV/OI-En

I-Al-Reset

Parallel Write

Apply

Refresh

Cancel

EN Control

Sel-Rt-EN CPU-EN

CPU-EN Low High

Sel-DPS-EN EN & Alarm

Measurement Unit (Central Reg)

MUR MI (Av=1.33,Os=1.5)

Sel-MU Chan 0

Sel-Cent-MI Chan 0

Sel-Mon-OE CPU-Mon-OE

Sel-MI-OE CPU-Mon-OE

CPU_Mon-OE

CPU-MI-Mon-OE

Kelvin Alarms

Kelvin-Th 0.175V (0)

RT-Kel-Al

CPU-Kel-Al-En

Sel-Kel-Al Kel-Al-Reset

Switch Matrix

Con-FS

Con-EF-F

Con-ES-F

Con-ES-S

Con-EF-ES

Compensation

Con-Cap-0 Con-Cap-3A

Con-Cap-1 Con-Cap-4B

Con-Cap-2

Dis-Res-0 Con-Res-2

Con-Res-1 Con-Res-3

Measurement Unit (Per Channel)

MUR# MI (Av=1.33,Os=1.5)

Sel-Mon-OE# CPU-Mon-OE

CPU_Mon-OE#

TJ and OT Alarm (Central Reg)

Cpu-Tj-En Gbl-CPU-OT-Dis

Sel-OT-Alarm RT-OT

CPU-OT CPU-OT-Dis#

OT-Flag-Reset

Per Channel Readback

RT-Kel-Al L-Kel-Al

OI-Snk OI-Src

RT-OI-Snk RT-OI-Src

L-OI-Snk L-OI-Src

Chan-Alarm DPS-En

Sel-FV0 Sel-FV1

L-OT-Al RT-OT-Al

Central Level (Central Reg)

Sel-Rt-Cent CPU-Cent-D

CPU-Cent-D ForceA0

Central ALARM (Central Reg)

CPU-Alarm CPU-Alarm-En

Central Readback

L-OT RT-OT

OT-Alarm

Ganging

Sel-G-Out FV

Figure 9: Vesuvius DC Levels Dialog Box

Vesuvius (Dev=0) Channel#0 DC Levels
✕

Central Calibration

Av (Gain)

Offset (mV)

Volt Step

FI Step

ICL Step

Mode and Ranges

FV Mode FVR

IR0 (2.56uA) IR3 (2.56mA)

IR1 (25.6uA) IR4 (25.6mA)

IR2 (256uA) IR5 (512mA)

CMRR-Adj Code (+/-127)

Parallel Write

Apply

Refresh

Cancel

DC Value

ForceA-FV

ForceB-FV

ForceA-FI

ForceB-FI

ICH

ICL

VCH

VCL

Offset Correction

VFA-FV

VFB-FV

VFA-FI

VFB-FI

ICH

ICL

VCH

VCL

Gain Correction

VFA-FV

VFB-FV

VFA-FI

VFB-FI

ICH

ICL

VCH

VCL

VR1 = -2.00V to +6.00V 8V = +/- 0.432V Range = 0.75 to 1.25

VR2 = -2.0V to +14.0V 16V = +/- 0.864V

ICL = (-0.0 to +1.5)*Imax IR = +/- 0.054*1.5*Imax

Note: Parallel Write does not write Offset/Gain values to all channels

Calibrate

Figure 10: Vesuvius DAC Configuration Dialog Box

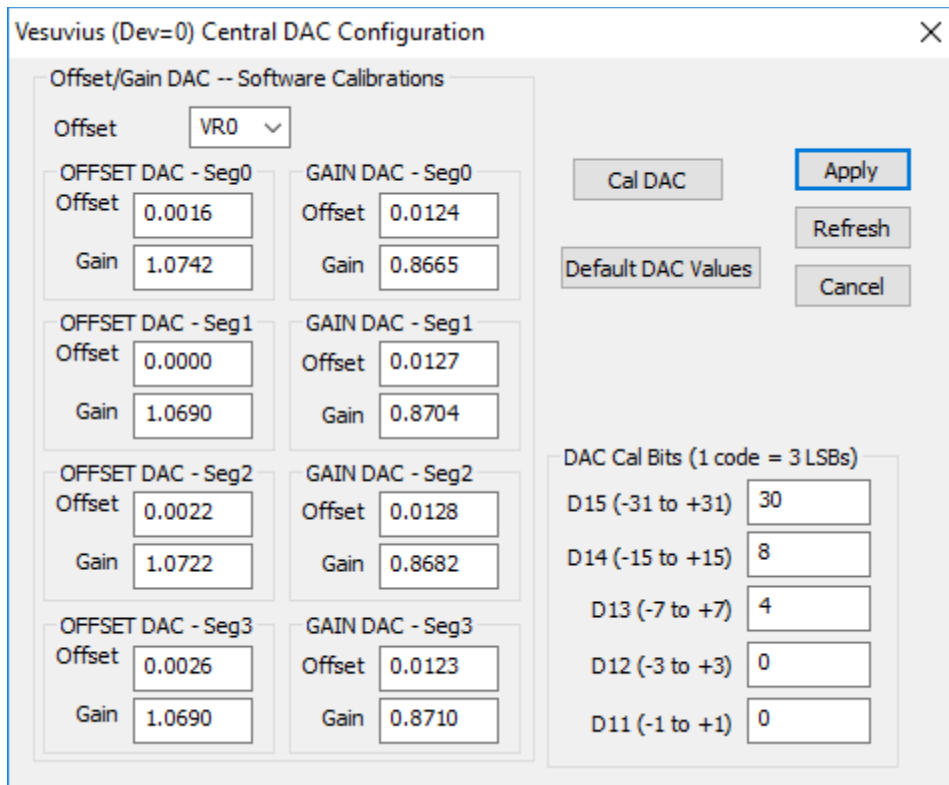
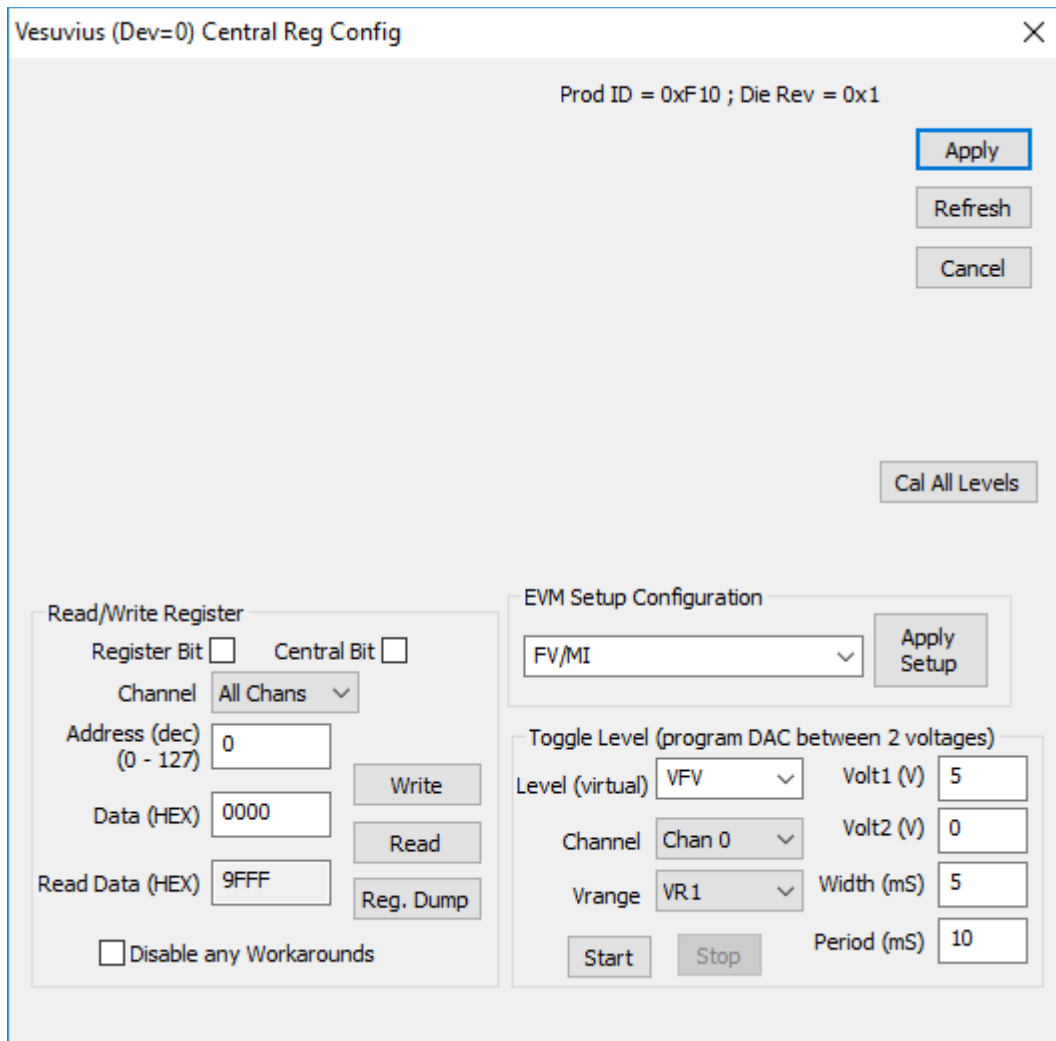


Figure 11: Vesuvius Central Register Dialog Box



3 Vesuvius EVM Loadboard Detailed Description

Error! Reference source not found. illustrates the Vesuvius EVM EVM loadboard. Almost all of the circuitry is used to test, validate and demonstrate in the bench. Besides decoupling caps, the only external components required are the 10K resistor connected to REXT and the CAP_A, CAP_B, & CAP_VDD compensation caps.

Figure 12: Vesuvius EVM Detailed Block Diagram

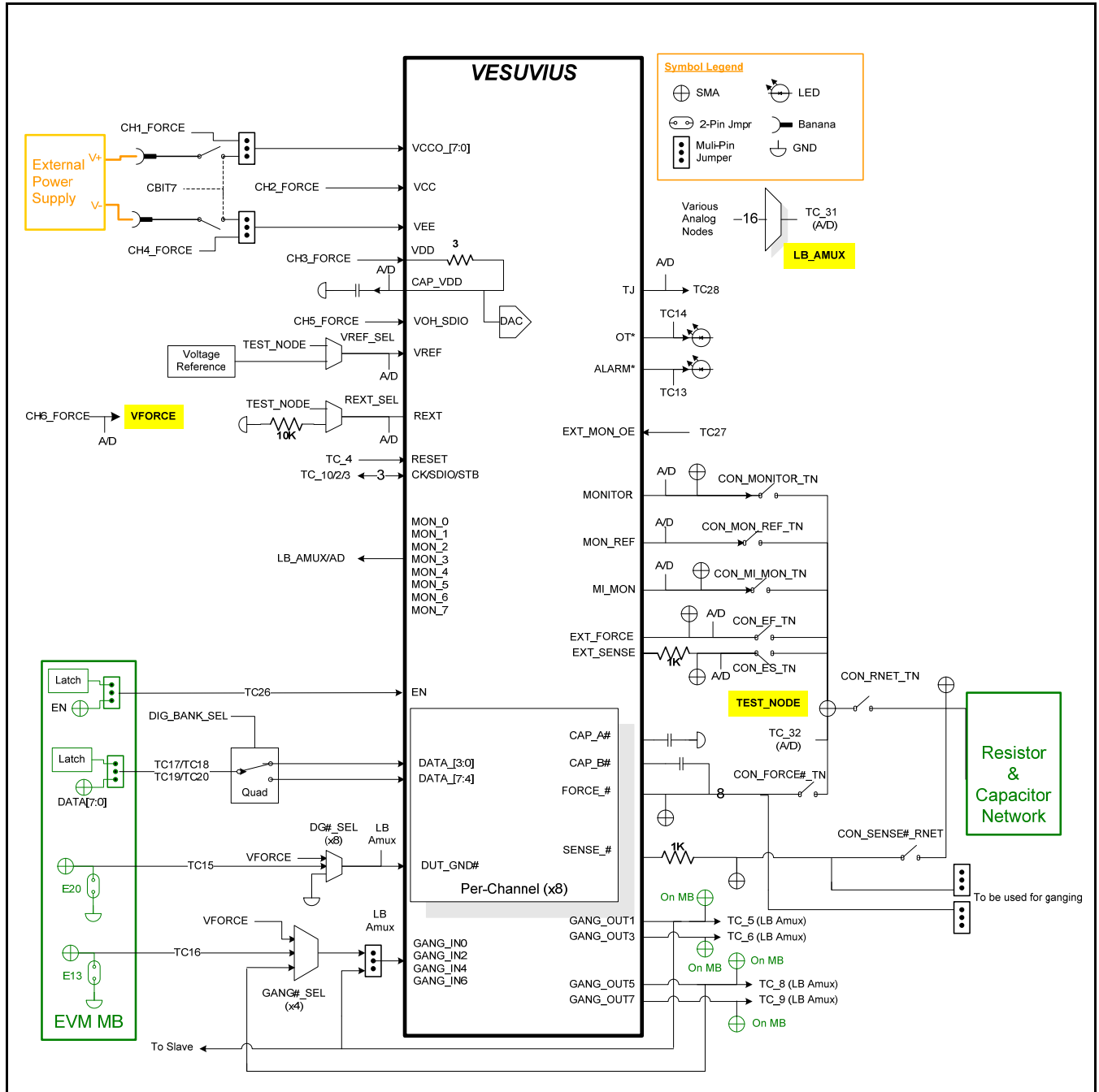
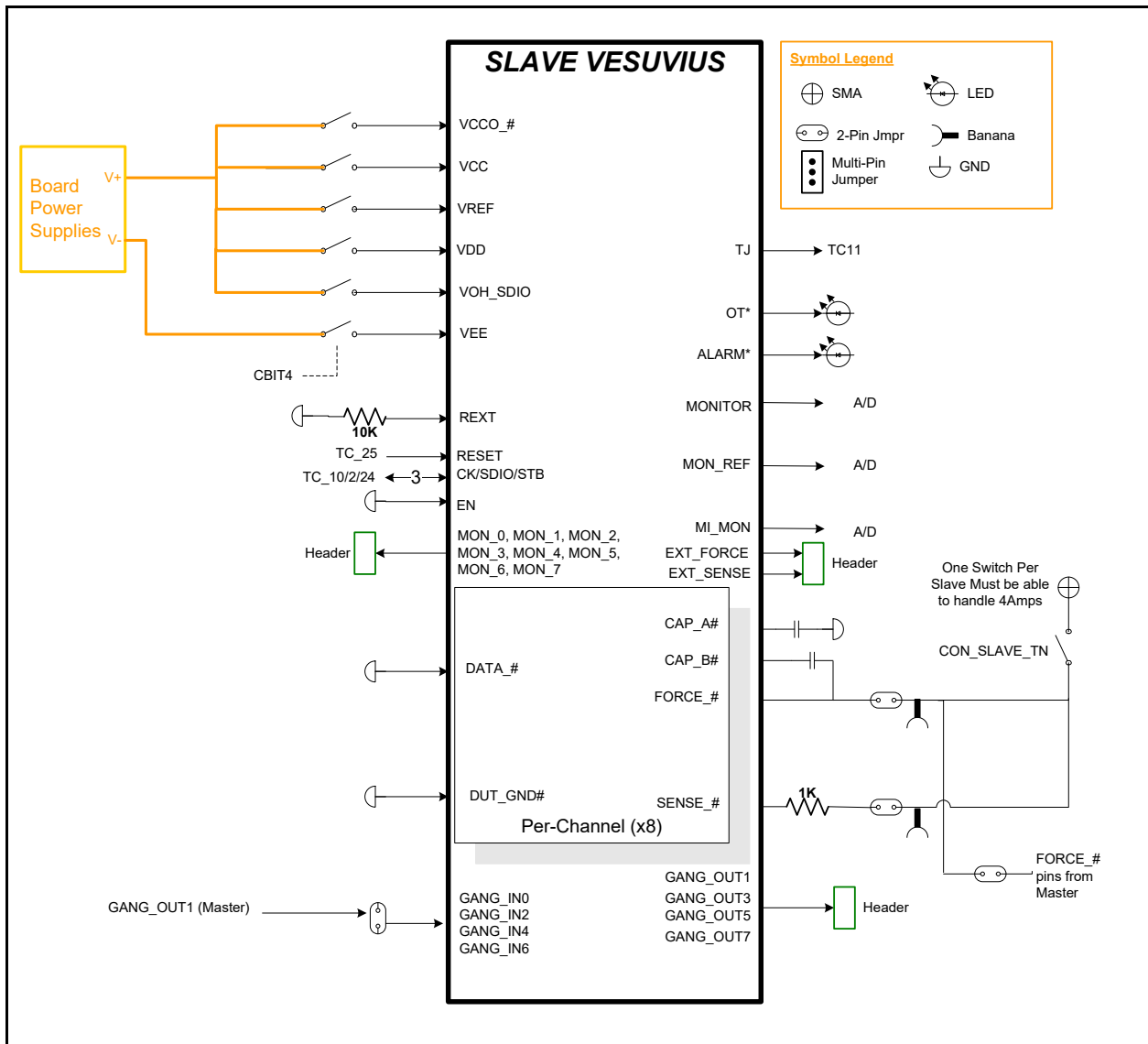


Figure 13: Vesuvius Slave Detailed Block Diagram



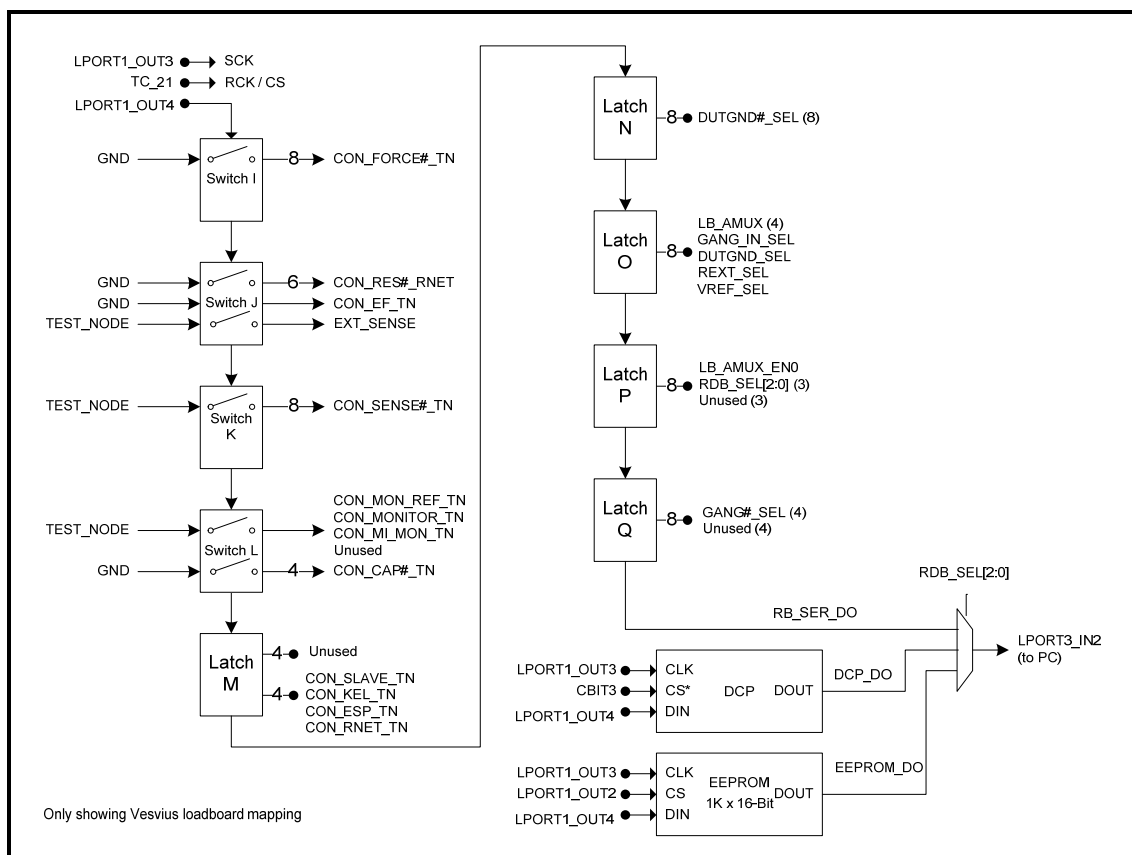
3.1 Vesuvius EVM Loadboard Controller

Error! Reference source not found. illustrates the Vesuvius EVM controller section. The Vesuvius EVM loadboard contains nine 8-bit latches (registers), a 16K EEPROM, and a Digitally Controlled Potentiometer (DCP). The Cbit1 to CBit7 are also used to control various relays, the C-Bit# are open-drain outputs used to control relays. The C-Bits originate from the Octal FVMI board.

The latches are daisy chained together using the SDI_SCK/RCK/CS signals originating from the Motherboard. The EEPROM is controlled by the LPORT1_OUT[4:2] signals originating from the motherboard. The DCP is controlled by LPORT1_OUT4/2 and LB_DATA3 signals originating from the motherboard.

The loadboard latches are labeled STB_I to STB_Q. This was named as an extension to the REG_A to REG_H Octal FVMI / Motherboard registers.

Figure 14: Controller Section Detailed Block Diagram



4 Document Revision History

Revision	Date	Description
A01	2/13/17	Initial Draft.
A02	6/26/17	Added Gang device to loadboard.