Pluto/Pluto2 Quick Start Application Note

Rev A02: 05/20/2013

This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

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1 Introduction

This document describes the steps to perform an initial system check-out of the Pluto/Pluto2 device.

These instructions assume the customer system can set the Pluto/Pluto2 supplies, has a mechanism to read/write registers, has the ability to measure voltages (either using an external DMM or system resource), provide a simple DATA stream, and so on.

Important Note: The steps described below illustrate a cause and effect to demonstrate how to interface with the device. In a normal application; sequencing, calibration and other factors may require the registers to be written in a different order. Please refer to the Planet ATE Software Driver documentation for details.

1.1 Reset State

Whenever a Hardware or Software reset is issued, the device is configured into the following state.

Note: The examples rely on the default (reset) configuration to demonstrate the minimum register transactions to achieve the desired configuration. In a customer application, a Reset should only be issued on first power-on. When reconfiguring the device for different modes, the application should only change the pertinent registers. There are some registers that only need to be set one time after power on; otherwise if the Reset was issued while reconfiguring for a different mode, the reset could cause unexpected results.

- RAM – Unknown at power ON. Left unchanged if reset issued from a previous configuration
- Registers – all registers are initialized to '0'; which implies:
  - PMU Block
    - PMU is in Hi-Z mode (Con-PMU=0)
    - Tight loop
    - FV op-amp input sourced from FV DAC
    - Data/En sourced from CPU control
    - All switches and IR open
    - Voltage Range 0
    - Monitor is in Hi-Z
  - Comparator Blocks
    - COMP pins sourced from measurement unit (V-mu)
    - Voltage Range 0
  - Central Registers
    - Vmid = 1.5V; which allows for -0.5V to 3.5V in VR0
    - DAC Cal Bits uncal'ed
    - Ganging disabled

1.2 Set Pluto/Pluto2 Supplies

The first step is to apply the appropriate voltage. After power is applied, it is recommended to toggle the hardware reset (active high) on Pluto/Pluto2 device or issue the Software Reset (register 0xC001).

Verify the voltage at the Pluto/Pluto2 pins or within close proximity to ensure there are no IR drops. In addition, the customer should verify the approximate current flow for each supply.

Note: In most systems, it may not be possible to measure the supply currents.

Table 1: Power-ON Current Values

Supply	Voltage (V)	Approximate Current (mA)	
		Pluto	Pluto2
VCC (1)	12.5	225	60
VEE (1)	-3.5	225	65
VDD	3.3	90	60
VREF	3.0	0	0
VOH (2)	3.3	0	0
VOL (2)	0.0	0	0

Notes:

1) VCC and VEE supply voltages are application dependant
2) The VOH and VOL should have minimal current since the COMP pins are in a static state.

1.3 Register/RAM Access (CPU Port Transactions)

The following steps perform simple register/RAM access (write/read) to verify to CPU port is functioning.

1.3.1 Read Die ID Register

Read the Die ID registers (address = 0xC07F); Table 2 lists the expected return values for different silicon revisions.

Table 2: Die ID Register Values

Rev	Pluto (HEX)	Rev	Pluto2 (HEX)
9	0x0199	1	0x01A1
#	0x019#	#	0x01A#

1.3.2 Register Access

Follow Table 3 to verify the basic ability to write/read registers. The following bullet items highlight some key aspects of a register access:

- Address bit D15 (Register Bit) must be '1' to access a register
- Address bit D14 (Central Bit) is used to distinguish between Per-Chan and Central Registers
- WE bit must be '1' for the corresponding Data Group bits to be written
- WE bits (typically) read back '0'
- Writing to Undefined Data bits has no effect
- Undefined Data bits (typically) read back '0'
- A RESET sets all registers to a default value of '0000' (except Read-Only registers)
- Refer to the CPU Protocol Timing diagram for details

Table 3: Write/Read Registers

Description	Address (HEX)	Write Data (HEX)	Read Data (HEX)
Ch#0: Set IR5	0x8001	0x0120	0x0020
Ch#0: Set FV Vrange = VR1	0x8004	0x0028	0x0008
Central: Enable MONITOR, source from Chan#5	0xC000	0x003D	0x0015
Ch#7: Set IR4	0x8381	0x0110	0x0010
Central Reg: Software RESET	0xC001	0x0000 <don't care>	0x0000 (all registers)

1.3.3 RAM Access

Follow Table 3 to verify the basic ability to write/read RAM. The following bullet items highlight some key aspects of a RAM access:

- The Read-back Data matches the Written Data
- Address bit D15 (Register Bit) must be '0' to access the RAM
- A RESET does NOT set the RAM contents to a default value. They are left unchanged
- A RAM read-back requires 2 additional clock cycles
- Refer to the CPU Protocol Timing diagram for details

Table 4: Write/Read Registers

Description	Address (HEX)	Data (HEX)	Read Data (HEX)
Ch#0: FV Value DAC	0x0004	0xFFFF	0xFFFF
Ch#0: FV Offset DAC	0x0024	0xAAAA	0xAAAA
Ch#0: FV Gain DAC	0x0044	0x5555	0x5555
Ch#5: CVA Value DAC	0x0282	0xABCD	0xABCD
Parallel Write: DVL Offset DAC (need to set 'Parallel Load' bit)	0x0021	0x1234	0x1234 (read on all chans)

1.4 PMU Force Voltage / Measure Current (FV/MI) Mode

The following steps are used to output the FV voltage on the FORCE_0 pin. The Current (MI) is measured via the MONITOR pin. An external 1K resistor from FORCE_0 to GND will be needed to provide a load.

The CPU-Data/En register control bits are used to set the PMU state.

Notes:
1) The 'Output Voltage' is the approximate voltage since these are un-calibrated settings.
2) MI measured using Central MONITOR. Per-Chan MON# is always enabled
3) MI Voltage is defined as +/-1V for +/-Imax
4) For IR5 (Imax=2mA), internal Rsense = 250Ω, Con-PMU = 20Ω, and Con-IR switch = 130. These will cause voltage divider effect depending on feedback point.
5) Use different Rload for different Current Ranges (IR)

Table 5: Set PMU FV Levels

Description	Address (HEX)	Data (HEX)	FORCE Output Voltage	Central MONITOR Output Voltage
Software Reset	0xC001	0x0000	High-Z	High-Z
Ch#0: Set FV = 1.0V (default VR0)	0x0004	0x5FFF	High-Z	High-Z
Ch#0: Set FV Offset = 0.0	0x0024	0x7FFF	High-Z	High-Z
Ch#0: Set FV Gain = 1.0	0x0044	0x7FFF	High-Z	High-Z
Ch#0: Set IR5	0x8001	0x0120	High-Z	High-Z
Ch#0: Connect PMU (CPU-PMU-Con=1)	0x8000	0x0A00	1.0	High-Z
Ch#0: Set Con-FS=1	0x8003	0x1800	1.0	High-Z
Ch#0: Set measure path to MI	0x8002	0x000C	1.0	High-Z
Central: Enable MONITOR, source from Chan#0	0xC000	0x0038	1.0	0V (0mA)
Connect 1K from FORCE to GND	n/a	n/a	0.8V	0.4V (800uA)
Ch#0: Set Feedback=PMU_F (Loop=1)	0x8002	0x0030	0.98V	0.49V (0.98mA)
Ch#0: Set Feedback=SENSE (Local-Sense*=1)	0x8002	0x00C0	1.0V	0.5V (1.0mA)
Ch#0: Set Voltage Range 1 (VR1)	0x8004	0x0028	2.0V	1.0V (2.0mA)

1.4.1 Measure Junction Temperature

The following steps show how to measure and calculate the junction temperature using the internal temperature sensors.

Tj = (Va – Vb) * 1637 – 221

The measured temperature will be dependant on if there is a heat sink and/or air-flow present.

Table 6: Measure Junction Temperature

Description	Address (HEX)	Data (HEX)	MONITOR Output
Central: Enable MONITOR, source from Chan#0	0xC000	0x0038	Unknown, depends on measure path
Ch#0: Set Sel-Diag mux to source from Va-Tj (code 10)	0x8003	0x007A	Measure Va (expect ~2.3V)
Ch#0: Set Sel-Diag mux to source from Va-Tj (code 11)	0x8003	0x007B	Measure Vb (expect ~2.1V)
Apply above formula			

1.5 Elevate Software Driver and Documentation

At this point, the customer has demonstrated the basic ability to configure the device, set some levels, make some measurements, and output a driver waveform. This should imply the Pluto/Pluto2 device has been properly designed and assembled into the customer system.

The next step is to integrate the Planet ATE software driver (reference/example code) which allows the customer to:

- Configure the device for different modes
- Perform DC calibration
- Set Levels as a function of voltage rather than HEX codes
- Set Deskews
- Configure the PMU for different modes; including proper sequencing
- And more

2 Document Revision History

Revision	Date	Description
A01	05/27/2009	Initial Draft
A02	05/20/2013	Change to Elevate Semiconductor format