SOC 8-Channel DPS

ISL55180

ISL55180 is a highly integrated System-on-a-Chip (SOC) Device Under Test (DUT) power supply solution incorporating 8 independent DUT Power Supply (DPS) units.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per channel basis.

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

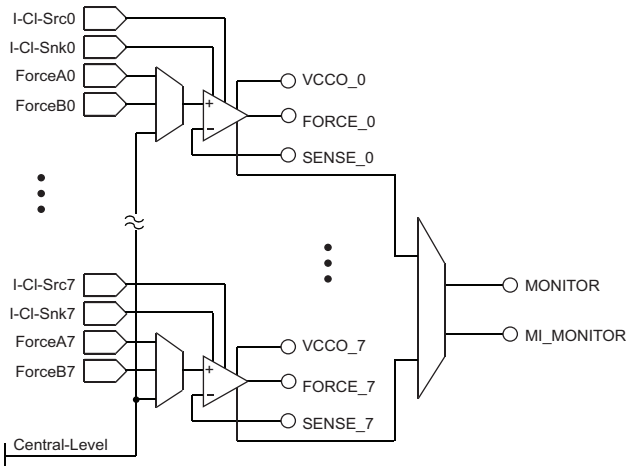
An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses.

Real time control is accomplished via the central EN and DATA_# pins. Real time observation is accomplished via the central monitor.

Applications

- Automated Test Equipment
- Logic/ASIC Verifiers
- Instrumentation

Block Diagram



Features

- Per Channel DPS
  - FV, FI, MV, MI, HiZ Capability
  - 16V Measure Voltage Input Compliance Range
  - 2 Force Voltage Ranges (8V, 16V)
  - 3 Measure Voltage Ranges (4V, 8V, 16V)
  - 6 Current Ranges: (256mA, 25.6mA, 2.56mA, 256µA, 25.6µA, 2.56µA)
  - Programmable Current Clamps
- Power Management
  - Independent Output Buffer Power Supply (VCCO)
  - Ability to Exceed VCCO in Lower Current Ranges
- Flexible Ganging Capability
  - No Restrictions on Maximum # DPS Units
- Protection
  - On-Chip Junction Temperature Monitor
  - Over-Temperature Shut Down per Chip
  - Kelvin Connection Sensing/Alarm per Channel
  - Over-Current Sensing/Alarm per Channel
- Global External Force/Sense Connectable to any Channel
- Monitor
  - One General Purpose Central Monitor per Chip
    - Scaling and Shifting Capability
    - HiZ Capability
  - One Dedicated Measure Current Monitor per Chip
    - HiZ Capability
- 3-Bit Serial CPU Port
- On-Chip DAC to Generate DC Levels
  - 2 Independent FV Levels/Channel
  - Central Resource Mode w/16 Selectable Levels
  - Independent Source and Sink Clamp Levels/Channel
  - 16 bits/Level
  - On-Chip Offset and Gain Correction per Level
- Package/Power Dissipation
  - Pb-Free (RoHS Compliant)
  - 128 Lead, 14mmx20mm, LQFP w/Exp Heat Slug
  - Pdq 115mW/Channel; Pdq 920mW/Chip

Block Diagram

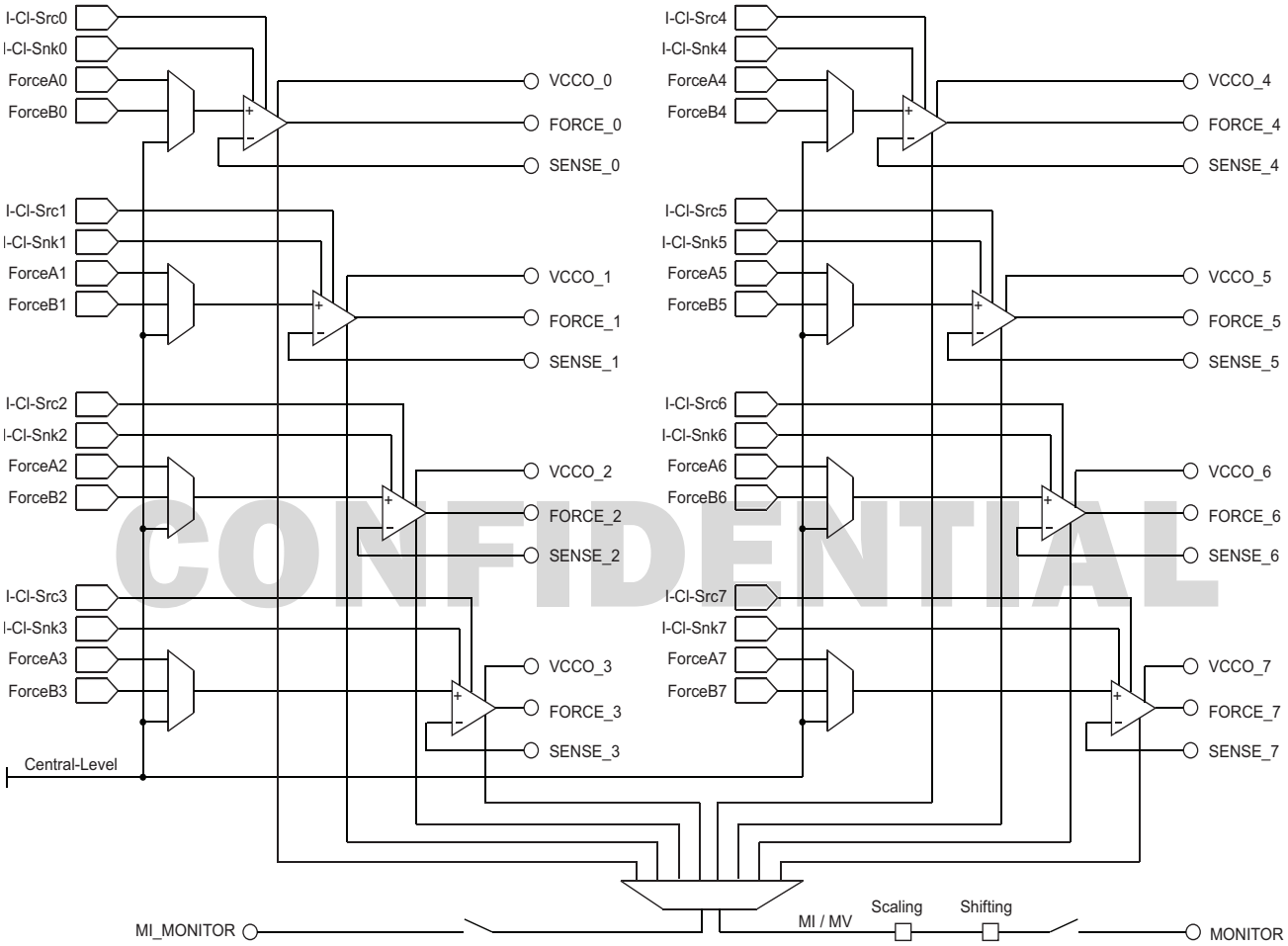


Table of Contents

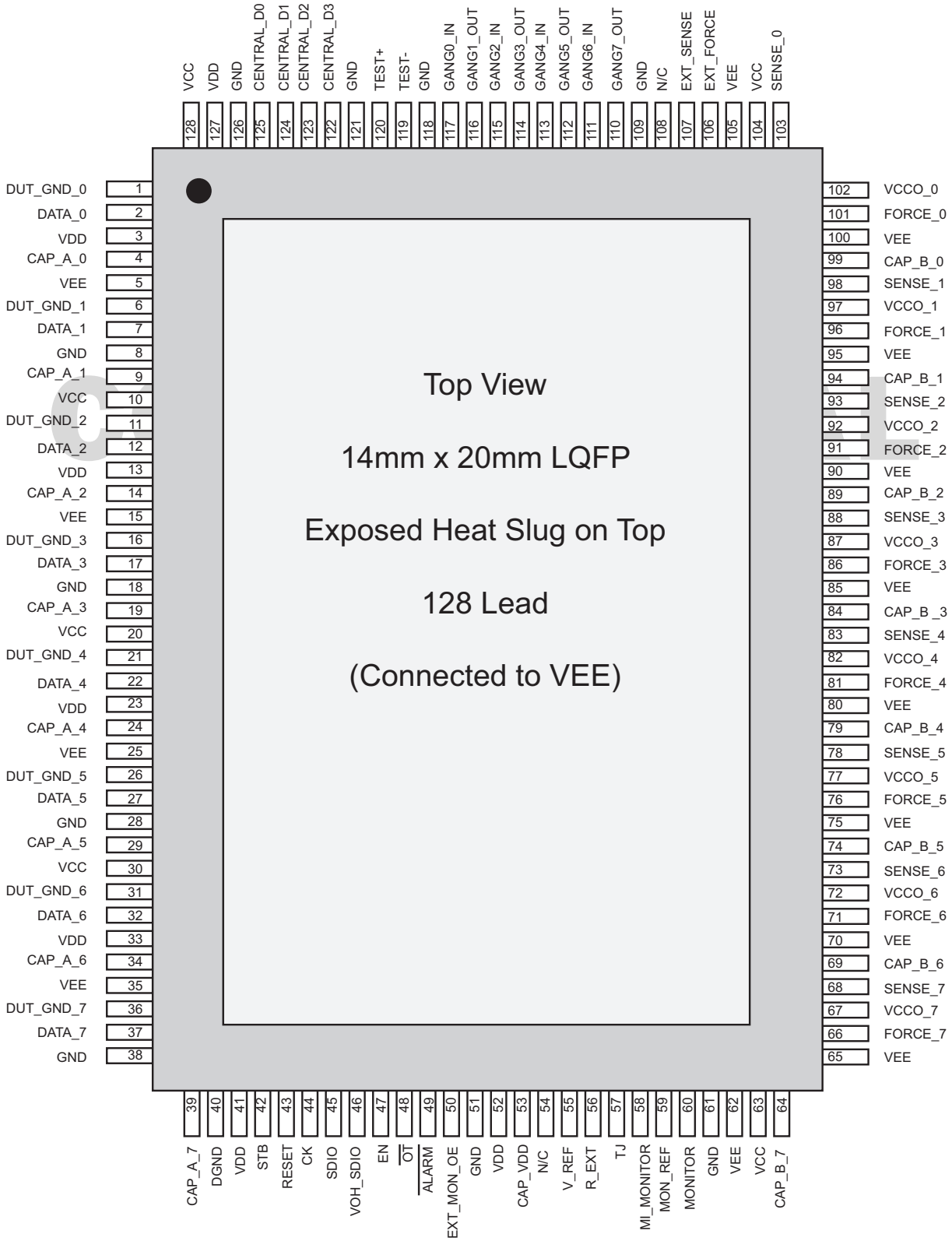
Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
101, 103, 1	FORCE_0, SENSE_0, DUT_GND_0	Channel 0 force, sense, and DUT ground pins.
2	DATA_0	Channel 0 data input pin.
102	VCCO_0	Positive analog supply for the Channel 0 output stage.
4, 99	CAP_A_0, CAP _B_0	Channel 0 op amp compensation capacitor pins.
96, 98, 6	FORCE_1, SENSE_1, DUT_GND_1	Channel 1 force, sense, and DUT ground pins.
7	DATA_1	Channel 1 data input pin.
97	VCCO_1	Positive analog supply for the Channel 1 output stage.
9, 94	CAP_A_1, CAP_B_1	Channel 1 op amp compensation capacitor pins.
91, 93, 11	FORCE_2, SENSE_2, DUT_GND_2	Channel 2 force, sense, and DUT ground pins.
12	DATA_2	Channel 2 data input pin.
92	VCCO_2	Positive analog supply for the Channel 2 output stage.
14, 89	CAP_A_2, CAP_B_2	Channel 2 op amp compensation capacitor pins.
86, 88, 16	FORCE_3, SENSE_3, DUT_GND_3	Channel 3 force, sense, and DUT ground pins.
17	DATA_3	Channel 3 data input pin.
87	VCCO_3	Positive analog supply for the Channel 3 output stage.
19, 84	CAP_A_3, CAP_B_3	Channel 3 op amp compensation capacitor pins.
81, 83, 21	FORCE_4, SENSE_4, DUT_GND_4	Channel 4 force, sense, and DUT ground pins.
22	DATA_4	Channel 4 data input pin.
82	VCCO_4	Positive analog supply for the Channel 4 output stage.
24, 79	CAP_A_4, CAP_B_4	Channel 4 op amp compensation capacitor pins.
76, 78, 26	FORCE_5, SENSE_5, DUT_GND_5	Channel 5 force, sense, and DUT ground pins.
27	DATA_5	Channel 5 data input pin.
77	VCCO_5	Positive analog supply for the Channel 5 output stage.
29, 74	CAP_A_5, CAP_B_5	Channel 5 op amp compensation capacitor pins.
71, 73, 31	FORCE_6, SENSE_6, DUT_GND_6	Channel 6 force, sense, and DUT ground pins.
32	DATA_6	Channel 6 data input pin.
72	VCCO_6	Positive analog supply for the Channel 6 output stage.
34, 69	CAP_A_6, CAP_B_6	Channel 6 op amp compensation capacitor pins.
66, 68, 36	FORCE_7, SENSE_7, DUT_GND_7	Channel 7 force, sense, and DUT ground pins.
37	DATA_7	Channel 7 data input pin.
67	VCCO_7	Positive analog supply for the Channel 7 output stage.
39, 64	CAP_A_7, CAP_B_7	Channel 7 op amp compensation capacitor pins.
55, 56	V_REF, R_EXT	External precision voltage and resistance reference.
57, 48, 49	TJ, $\overline{OT}$, $\overline{ALARM}$	On-chip die temperature monitor, OT flag and alarm outputs.
47	EN	Real time HiZ control pin.
60, 58	MONITOR, MI_MONITOR	Central monitor and measure current monitor analog outputs.
59, 50	MON_REF, EXT_MON_OE	Monitor negative reference output and external HiZ control pins.
44, 45, 42, 43	CK, SDIO, STB, RESET	Serial port control pins.

Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
120, 119	TEST+, TEST-	External test DAC differential inputs.
106, 107	EXT_FORCE, EXT_SENSE	Central external force and sense pins.
117, 116	GANG0_IN, GANG1_OUT	External ganging pins for Channels 0 and 1.
115, 114	GANG2_IN, GANG3_OUT	External ganging pins for Channels 2 and 3.
113, 112	GANG4_IN, GANG5_OUT	External ganging pins for Channels 4 and 5.
111, 110	GANG6_IN, GANG7_OUT	External ganging pins for Channels 6 and 7.
125, 124, 123, 122	CENTRAL_D0, CENTRAL_D1, CENTRAL_D2, CENTRAL_D3	Central DC level real time select pins.
10, 20, 30, 63, 104, 128	VCC	Analog positive power supply.
5, 15, 25, 35, 62, 65, 70, 75, 80, 85, 90, 95, 100, 105	VEE	Analog negative voltage supply
3, 13, 23, 33, 41, 52, 127	VDD	Digital power supply.
8, 18, 28, 38, 51, 61, 109, 118, 121, 126	GND	Chip ground.
40	DGND	Digital ground.
46	VOH_SDIO	Positive supply rail to the SDIO output pin.
53	CAP_VDD	External filter capacitor for VDD.

Pin Configuration



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	VDD – 0.5		+15	V
VCCO_#	–0.5		VCC + 0.5	V
VEE	–5		0.5	V
VDD	–0.5		+5	V
VCC – VEE	–0.5		17.5	V
VDD – VEE		+8		V
Digital Pins				
CK, SDIO, STB, RESET	GND – 0.5V		VDD + 0.5	V
SENSE	GND – 0.5V		VDD + 0.5	V
MONITOR	GND – 0.5V		VDD + 0.5	V
$\overline{\text{ALARM}}$, $\overline{\text{OT}}$	GND – 0.5V		VDD + 0.5	V
CENTRAL_D_#	GND – 0.5V		VDD + 0.5	V
EN	GND – 0.5V		VDD + 0.5	V
DATA_#	GND – 0.5V		VDD + 0.5	V
SDIO Output Current	–20		+20	mA
External References				
R_EXT		10		KΩ
V_REF	GND – 0.5V		VDD + 0.5	V
Analog Pins				
FORCE_#	VEE – 0.5		VCC + 0.5	V
SENSE_#	VEE – 0.5		VCC + 0.5	V
MONITOR	GND – 0.5	20	VDD + 0.5	V
MI_MONITOR	GND – 0.5	20	VDD + 0.5	V
EXT_SENSE	VEE – 0.5		VCC + 0.5	V
EXT_FORCE	VEE – 0.5		VCC + 0.5	V
GANG#_IN	VEE – 0.5		VCC + 0.5	V
GANG#_OUT	VEE – 0.5		VCC + 0.5	V
TEST+, TEST–	GND – 0.5	20	VDD + 0.5	V
TJ	GND – 0.5	20	VDD + 0.5	V
DUT_GND	VEE – 0.5		VCC + 0.5	V
Thermal Information				
Maximum Junction Temperature			150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+8		+14	V
VCCO_#	FORCE_# +0.5		VCC	V
VEE	–4		–2	V
VDD	+3.25		3.45	V
VCC – VEE	+10		+16	V
VCCO_# – VEE	+6		+16	V
VDD – VEE	+.525		+7.4	V
Digital Pins				
CK, SDIO, STB, RESET	GND		VDD	V
EXT_MON_OE	GND		VDD	V
EN	GND		VDD	V
DATA_#	GND		VDD	V
CENTRAL_D_#	GND		VDD	V
$\overline{\text{ALARM}}$, $\overline{\text{OT}}$	GND		VDD	V
External References				
V_REF	+2.99		3.01	V
R_EXT	10KΩ ± 0.1% tempco = 25ppm			
Analog Pins				
FORCE_# (HiZ Compliance)	VEE		VCC	V
IR0 - IR5 (FV Mode# = 0) FORCE_# (Active, FV, I_{OUT} = 0) FORCE_# (Active, FV, $\pm I_{MAX}$)	 VEE + 1.5 to Min of ((VCCO – 0.15), (VCC – 1.0)) VEE + 3.0 to Min of ((VCCO – 0.5), (VCC – 2.5))			 V V
IR0 - IR4 (FV Mode# = 1) FORCE_# (Active, FV, I_{OUT} = 0) FORCE_# (Active, FV, $\pm I_{MAX}$)	 VEE + 1.5 VEE + 2.0		 VCC – 1.0 VCC – 1.5	 V V
IR5 (FV Mode# = 1) FORCE_# (Active, FV, $\pm I_{MAX}$)	N/A		N/A	N/A
SENSE_#	VEE		VCC	V
MONITOR	GND		VDD	V
MI_MONITOR	GND		VDD	V
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V
GANG#_IN, GANG#_OUT	VEE + 1.5V		VCC - 1.5V	V
TEST+, TEST–	GND		VDD	V
TJ	GND		VDD	V
Miscellaneous				
Junction Temperature	+25		100	°C
CPU Port CK Frequency	10		25	MHz
Capacitive Load at DOUT_# (IR0 - IR5)	0		50	µF

DC Characteristics

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supply Current

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd (TYP) mW/Chip
NO LOAD, FV-Mode# = 0							
11100	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, FV-Mode = 0, IR5, FV = +3V		74	140	mA	925
11200	ICC_O			2	35	mA	8.5
11300	IEE		–160	–63		mA	220.5
11400	IDD			60	90	mA	207
11500	IOH_SDIO		–2.5		2.5	mA	0
NO LOAD, FV-Mode = 1							
11110	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, FV-Mode = 1, IR4, FV = +3V		75	140	mA	937.5
11210	ICC_O			1	3	mA	4.25
11310	IEE		–160	–63		mA	220.5
11410	IDD			62	90	mA	214
11510	IOH_SDIO		–2.5		2.5	mA	0
$+I_{MAX}$, FV-Mode = 0							
11120	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, $+I_{MAX}$, IR5, FV-Mode = 0, FV = +3V		120	190	mA	1362
11220	ICC_O			2	3	A	2500
11320	IEE		–160	–63		mA	220.5
11420	IDD			60	90	mA	207
11520	IOH_SDIO		–2.5		+2.5	mA	0
$+I_{MAX}$, FV-Mode = 1							
11130	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V VDD = +3.45V, $+I_{MAX}$, IR4, FV-Mode = 1, FV = +8V		120	170	mA	1132
11230	ICC_O			1	3	mA	4.25
11330	IEE		–160	–63		mA	220.5
11430	IDD			62	90	mA	214
11530	IOH_SDIO		–2.5		2.5	mA	0
$-I_{MAX}$, FV-Mode = 0							
11120	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, $-I_{MAX}$, IR5, FV-Mode = 0, FV = +3V		74	140	mA	925
11220	ICC_O			2	35	mA	8.5
11320	IEE		–3	–2		A	1300
11420	IDD			60	90	mA	207
11520	IOH_SDIO		–2.5		+2.5	mA	0
$-I_{MAX}$, FV-Mode = 1							
11130	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V VDD = +3.45V, $-I_{MAX}$, IR4, FV-Mode = 1, FV = +8V		75	140	mA	925
11230	ICC_O			1	3	mA	4.25
11330	IEE		–360	–205		mA	1332
11430	IDD			62	90	mA	214
11530	IOH_SDIO		–2.5		2.5	mA	0

NOTE: The total chip power values are based upon typical supply currents and power supply levels indicated in the test conditions. For proper sizing of power supplies in the application, power to the DUT or load being driven the ISL55180 must also be accounted for.

DC Electrical Specifications – Thermal Monitor and Alarm

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TJ, $\overline{OT}$						
10996	TJ HiZ Leakage	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, Tested at 0V and VDD	–500	0	+500	nA
10995	Over-Temperature Threshold	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V		135 ± 15	150	°C
10994	$\overline{OT}$ VOH (HiZ Leakage)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, Tested at 0V and VDD	–100	0	+100	nA
10993	$\overline{OT}$ VOL	VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V, Input current = 2mA			0.4	V

DC Electrical Specifications – CPU Port

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V	1.6			V
17110	VIL	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V			0.8	V
17120	I_{IN} (Input Leakage Current)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, tested at 0V and VDD	–1	0	+1	µA
17200	VOH (SDIO Only)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V, VOH_SDIO = VDD, I_{LOAD} = 8mA	2.4			V
17210	VOL (SDIO Only)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V, VOH_SDIO = VDD, I_{LOAD} = 8mA			0.8	V

DC Electrical Specifications – Digital Inputs

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
EN, CENTRAL_D_<3:0>, DATA_#						
13260	VIH	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V	2.0			V
13261	VIL	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V			0.8	V
13262	I_{IN} (Input Leakage Current) (HiZ)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, tested at 0V and VDD	–1	0	+1	µA

DC Electrical Specifications –Digital Outputs

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ALARM						
13360	VOL (Sinking 2mA)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V			0.4	V
13361	VOH (HiZ Leakage)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, tested at 0V and VDD	–100		+100	nA

DC Electrical Specifications – Analog Pins

VCC = +12.5V, VCCO_# = 4.25V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage/Input Currents						
10999	V_REF Input Current		–1		+1	µA
10998	DUT_GND Input Current	Tested at –1V, 0V and +1V	–15		+15	nA
10700	EXT_FORCE, EXT_SENSE in HiZ	Tested at 0V, VCC, VEE	–15		+15	nA
10800	GANG#_IN Input Current	Tested at VCC + 0.5V, VEE - 1.5V	–1		+1	µA
10801	GANG#_OUT HiZ Leakage Current	Tested VCC – 1.5V, VEE + 1.5V, Sel-G#-OUT and Sel-G(#–1)– OUT = 1	–1		+1	µA
20210	CAP_B_# Leakage Current		–100		+100	nA
20560	CAP_VDD Leakage Current	Not production tested.	–15		+15	µA

Level DAC Calibration

All DC tests are performed after the DAC is first calibrated.The upper 5 bits of the DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carry error as small as possible.

DC Electrical Specifications – DAC Calibration

VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
16510	Level DAC D15 Step Error	(DAC @ 8000 - DAC @ 7FFF)/(8000 – 7FFF) – DAC LSB; VR0, Code 8000 – Code 7FFF – LSB; VR0	-2		+2	mV
16520	Level DAC D14 Step Error	(DAC @ 7000 - DAC @ 3000)/(7000 – 3000) – DAC LSB; VR0, Code 4000 – Code 3FFF – LSB; VR0	-2		+2	mV
16530	Level DAC D13 Step Error	(DAC @ 7000 - DAC @ 5000)/(7000 – 5000) – DAC LSB; VR0, Code 6000 – Code 5FFF – LSB; VR0	-2		+2	mV
16540	Level DAC D12 Step Error	(DAC @ 7000 - DAC @ 6000)/(7000 – 6000) – DAC LSB; VR0, Code 7000 – Code 6FFF – LSB; VR0	-2		+2	mV
16550	Level DAC D11 Step Error	(DAC @ 7800 - DAC @ 7000)/(7800 – 7000) – DAC LSB; VR0, Code 7800 – Code 77FF – LSB; VR0	-2		+2	mV
16560	LSB Step Error	8V Range, FV-Mode = 1, Post auto calibration		124		µV

There are 3 on-chip internal DACs used for:

1. DC Level
2. DC Level Offset Correction
3. DC Level Gain Correction

DAC testing is performed post DAC Cal Bit Calibration.

DC Electrical Specifications – DAC

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LEVEL DAC TEST						
16100	Span	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Span = DAC(FFFF) – DAC(0000), Notes 1, 2	7.5	8.0	9.5	V
16110	Linearity Error	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 3	–2	1	+2	mV
16120	Bit Test Error	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 4	–2	0.5	+2	mV
16190	Droop Test	Notes 1, 5	–1		+1	mV/ms
16400	DAC Noise	FV = 0V, Measured at FORCE_0, RMS measurement, Note 1			+1.0	mV
OFFSET DAC TEST						
16200	+ Adjustment Range	Level and Gain DACs both programmed to mid scale (Code 7FFF), Code 0000, FFFF relative to mid scale (7FFF), Notes 1, 2	+4.5	+5.4	+6.6	% of Span
16210	- Adjustment Range	Level and Gain DACs both programmed to mid scale (Code 7FFF), Code 0000, FFFF relative to mid scale (7FFF), Notes 1, 2	–6.6	-5.4	–4.5	% of Span
16220	Linearity Error	Level and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 3	–3	1.5	+3	mV
16230	Bit Test Error	Level and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 4	–2	1.5	+2	mV
GAIN DAC TEST						
16300	+ Adjustment Range	Level DAC = FFFF, Offset DAC = 7FFF, Code 0000, FFFF relative to mid scale (7FFF), Notes 2, 6	1.18	1.25	1.30	V/V
16300	- Adjustment Range	Level DAC = FFFF, Offset DAC = 7FFF, Code 0000, FFFF relative to mid scale (7FFF), Notes 2, 6	0.7	0.75	0.81	V/V
16310	Linearity Error	Level DAC = FFFF, Offset DAC = 7FFF, Notes 2, 3, 6	–2	0.5	+4	mV/V
16320	Bit Test Error	Level DAC = FFFF, Offset DAC = 7FFF, Notes 2, 4, 6	–2	0.5	+2	mV/V
16330	DUT_GND Error	DUT_GND forced to ±1V. Measured at the FORCE pin, Note 6	–5		+5	mV

NOTES:

1. VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.3V
2. DAC tests performed using the DPS in FV mode and the MONITOR output. 8V Range, FV-Mode = 1.
3. Linearity Test - 17 equal spaced codes relative to a straight line determined by 1/8 and 7/8 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, **DFFF**, EFFF, FFFF. (Calibration points in **bold**.)
4. Bit Test - Walking 1 and walking 0 to determine the correct bit weight 1's: 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0008, 0004, 0002, 00010's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
5. CPU CK turned off. 66ms delay between measurements. Each DC level on the chip checked one at a time.
6. VCC = +12.9V, VCCO_# = +4V, VEE = –2.9V, VDD = +3.2V.

Force Voltage

Channel Configuration:

1. Feedback# = SENSE_#

The sequence of events performed for FV Testing is:

1. Program VF#
2. Force current at FORCE_# w/external resource
3. Measure the voltage at FORCE_#.

FV tests:

1. Tested in all current ranges.

DC Electrical Specifications – Force Voltage

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV (POST CALIBRATION)						
14200	Output Force Error	VCC =+ 12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V, FV_MODE = 0 (8V range), Calibration points: 0V, 3V No-Load Test Points: –2V, +1V, +3.75V Full-Load Test Points ($\pm I_{MAX}$): 0V, 3.5V	–5		+5	mV
14201	Output Force Error	VCC =+ 12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V, FV_MODE = 1 (16V range), Calibration points: 0V, 10V No-Load Test Points: –2V, +5V, +12V Full-Load Test Points ($\pm I_{MAX}$): –1.5V, 11V	–10		+10	mV
FV TEMPERATURE COEFFICIENT						
	8V Range	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0		60		µV/°C
	16V Range	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0		200		µV/°C
HIZ LEAKAGE						
14090	FORCE_#, SENSE_#	VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, Tested at 0V, VCC, VEE + 0.5V	–5	< 0.1	+5	nA
CAPACITANCE						
	FORCE_# Capacitance	VCC = +12.5V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, HiZ		400		pF
	SENSE_# Capacitance	VCC = +12.5V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, HiZ		15		pF
PROTECTION						
14091	Short Circuit Current	VCC = +12.5V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, IR5, FV-Mode = 0, FV = +3V, output shorted to ground	500	575	700	mA

DC Electrical Specifications – PPMU - Measure Current

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MI (POST CALIBRATION)						
14100	Measure Current Error	TPMI (See Tables 1 and 2), IR0	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	nA
14101	Measure Current Error	TPMI (See Tables 1 and 2), IR1	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	nA
14102	Measure Current Error	TPMI (See Tables 1 and 2), IR2	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	µA
14103A	Measure Current Error	TPMI (See Tables 1 and 2), IR3, IOUT > ±256µA	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	µA
14103B	Measure Current Error	TPMI (See Tables 1 and 2), IR3, –256µA ≤ IOUT ≤ 256µA	–1.25%FS		+1.25%FS	µA
14104	Measure Current Error	TPMI (See Tables 1 and 2), IR4, IOUT > ±2.56mA	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	µA
14104B	Measure Current Error	TPMI (See Tables 1 and 2), IR4, –2.56mA ≤ IOUT ≤2.56mA	–1.25%FS		+1.25%FS	mA
14105	Measure Current Error	TPMI (See Tables 1 and 2), IR5, IOUT > ±25.6mA	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	mA
14105B	Measure Current Error	TPMI (See Tables 1 and 2), IR5, –25.6mA ≤ IOUT ≤25.6mA	–1.25%FS		+1.25%FS	mA
	MI Temperature Coefficient	IR0		±0.231		nA/°C
	MI Temperature Coefficient	IR1		±2.33		nA/°C
	MI Temperature Coefficient	IR2		±32.1		nA/°C
	MI Temperature Coefficient	IR3		±0.388		µA/°C
	MI Temperature Coefficient	IR4		±4.375		µA/°C
	MI Temperature Coefficient	IR5		±50.6		µA/°C
Common Mode Error (CME)						
14140	Common Mode Error	VCC = +12.9V, VCCO_# =+ 4V, VEE = –2.9V, VDD = +3.2V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V	–0.0125		+0.0125	%FS Current/V

TABLE 1. OUTPUT SOURCING

RANGE	CAL POINTS	TPMI
IR0 - IR2 FV-Mode = 1, BBias = 0 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/+0.2 • Imax +5V/+0.8 • Imax	+5V/+Imax +5V/(+Imax/2) +5V/0
IR4 FV-Mode = 1, BBias= 1 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/+0.95 • Imax +5V/+0.40 • Imax +5V/+0.30 • Imax +5V/+0.12 • Imax	+5V/+Imax +5V/(+Imax/2) +5V/0
IR5 FV-Mode = 0, BBias= 1 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/+0.2 • Imax +2.5V/+0.8 • Imax	+2.5V/+Imax +2.5V/(+Imax/2) +2.5V/0
IR4 FV-Mode = 0, BBias = 1 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/+0.95 • Imax +2.5V/+0.40 • Imax +2.5V/+0.30 • Imax +2.5V/+0.12 • Imax	+2.5V/+Imax +2.5V/(+Imax/2) +2.5V/0
IR3 FV-Mode = 1, BBias = 0 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/+0.95 • Imax +5V/+0.40 • Imax +5V/+0.30 • Imax +5V/+0.12 • Imax	+5V/+Imax +5V/(+Imax/2) +5V/0
IR3 FV-Mode = 0, BBias= 0 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/+0.95 • Imax +2.5V/+0.40 • Imax +2.5V/+0.30 • Imax +2.5V/+0.12 • Imax	+2.5V/+Imax +2.5V/(+Imax/2) +2.5V/0

TABLE 2. OUTPUT SINKING

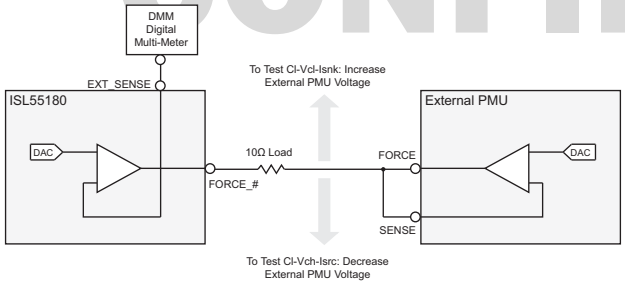
RANGE	CAL POINTS	TPMI
IR0 - IR2 FV-Mode = 1, BBias = 0 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/–0.2 • Imax +5V/-0.8 • Imax	+5V/–Imax +5V/(–Imax/2) +5V/0
IR4 FV-Mode = 1, BBias= 1 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/–0.95 • Imax +5V/–0.40 • Imax +5V/–0.30 • Imax +5V/–0.12 • Imax	+5V/–Imax +5V/(–Imax/2) +5V/0
IR5 FV-Mode = 0, BBias= 1 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/–0.2 • Imax +2.5V/–0.8 • Imax	+2.5V/–Imax +2.5V/(–Imax/2) +2.5V/0
IR4 FV-Mode = 0, BBias = 1 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/–0.95 • Imax +2.5V/–0.40 • Imax +2.5V/–0.30 • Imax +2.5V/–0.12 • Imax	+2.5V/–Imax +2.5V/(–Imax/2) +2.5V/0
IR3 FV-Mode = 1, BBias = 0 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/–0.95 • Imax +5V/–0.40 • Imax +5V/–0.30 • Imax +5V/–0.12 • Imax	+5V/–Imax +5V/(–Imax/2) +5V/0
IR3 FV-Mode = 0, BBias= 0 VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/–0.95 • Imax +2.5V/–0.40 • Imax +2.5V/–0.30 • Imax +2.5V/–0.12 • Imax	+2.5V/–Imax +2.5V/(–Imax/2) +2.5V/0

Current Clamps

Current clamps are tested in IR5 only.

The sequence of events to test the Source Current Clamps is as follows (this list is not an all-inclusive setup list). Please also refer to the figure below:

1. Program I-Cl-Src<15:0> to Test Point/Calibration Point.
2. Set I-Cl-En# = 1.
3. Set proper path to so that: Feedback# = Force_#.
4. Set Con-ES-F# = 1.
5. Set ForceA#<15:0> = 2V.
6. Measure Voltage at EXT_SENSE pin. (Initial FV Level)
7. Connect 10Ω load from FORCE_# on ISL55180 to External PMU.
8. Set External PMU voltage = 2V.
9. Decrease External PMU voltage until voltage measured at EXT_SENSE moves from the initial FV Level by the following amount: 15mV> (Initial FV Level - Measured FV Level) >5mV.
10. Use External PMU to measure current sourced by ISL55180.



The sequence of events to test the Sink Current Clamps is as follows (this list is not an all-inclusive setup list). Please also refer to the figure below:

1. Program I-Cl-Snk<15:0> to Test Point/Calibration Point.
2. Set I-Cl-En# = 1.
3. Set proper path to so that: Feedback# = Force_#.
4. Set Con-ES-F# = 1.
5. Set ForceA#<15:0> = 2V.
6. Measure Voltage at EXT_SENSE pin. (Initial FV Level)
7. Connect 10Ω load from FORCE_# on ISL55180 to External PMU.
8. Set External PMU voltage = 2V.
9. Increase External PMU voltage until voltage measured at EXT_SENSE moves from the initial FV Level by the following amount: 15mV> (Initial FV Level - Measured FV Level) >5mV.
10. Use External PMU to measure current sunk by ISL55180.

TABLE 3.

LEVEL	CAL POINTS	TP0	TP1
I-Cl-Src	+96mA +288mA	+72mA +144mA +240mA	+312mA +384mA
I-Cl-Snk	−96mA −288mA	−72mA −144mA −240mA	−312mA −384mA

DC Electrical Specifications – Current Clamps

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TP0 Test Points						
14500	Source Clamp Error	VCC = +12.9V, VCCO_# = +4V, VEE = −2.9V, VDD = +3.2V, VOH_SDIO = VDD, DUT_GND = 0V (See Table 3)	−1.0		+1.0	%FS
14520	Sink Clamp Error	VCC = +12.9V, VCCO_# = 4V, VEE = −2.9V, VDD = +3.2V, VOH_SDIO = VDD, DUT_GND = 0V (See Table 3)	−1.0		+1.0	%FS
TP1 Test Points						
14530	Source Clamp Error	VCC = +12V, VCCO_# = 6V, VEE = −4V, VDD = +3.45V, VOH_SDIO = VDD, DUT_GND_# = 0V (See Table 3)	−2.0		+2.0	%FS
14540	Sink Clamp Error	VCC = +12.9V, VCCO_# = 4V, VEE = −2.9V, VDD = +3.2V, VOH_SDIO = VDD, DUT_GND = 0V (See Table 3)	−2.0		+2.0	%FS

Measure Voltage – Central Monitor

The sequence of events performed for testing the MONITOR is:

1.Program Channel 0 in FV to the desired voltage (IR3, I_{LOAD} = 0)

2.Measure the voltage at FORCE_0

3.Measure the voltage at MONITOR

4.Calculate the difference to determine the error.

TABLE 4.

MV RANGE	MV CAL POINTS	MV TEST POINTS
4V	+0.5V +3.5V	0V 2V 4V
8V	–1V +5V	–2V +2V +6V
16V	–1V +11V	–2V +5V +12V

DC Electrical Specifications– Measure Voltage - Central Monitor

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Monitor Measure Voltage Error						
14800	4V Range	Note 1, Table 4	–2	1	+2	mV
14801	8V Range	Note 1, Table 4	–3		+3	mV
14802	16V Range	Note 1, Table 4	–6		+6	mV
MV Temperature Coefficient						
14820	4V Range	Note 1, Table 4		50		µV/°C
14821	8V Range	Note 1, Table 4		100		µV/°C
14822	16V Range	Note 1, Table 4		150		µV/°C
Uncalibrated Monitor MV Offset						
14830	4V Range	Note 1, Table 4	0.475		0.525	V
14831	8V Range	Note 1, Table 4	0.95		1.05	V
14832	16V Range	Note 1, Table 4	0.72		0.78	V
Uncalibrated Monitor MV Gain						
14840	4V Range	Note 1 Table 4	0.47		0.53	V/V
14841	8V Range	Note 1, Table 4	0.235		0.265	V/V
14842	16V Range	Note 1, Table 4	0.115		1.135	V/V
Output Impedance and Leakage						
19112	MONITOR Output Impedance	Tested at +2.5V, IOUT = 0µA/+100µA and 0µA/–100µA; Note 1, Table 4	75		150	Ω
14710	MONITOR HiZ Leakage Current	VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, tested at MONITOR = 0V	–10	< 0.1	+10	nA
14711	MON_REF Output Impedance	VCC = +17V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V	75		150	Ω
14712	MON_REF HiZ Leakage	VCC = +13.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V	–10	< 0.1	+10	nA
14713	MI_MONITOR Output Impedance	Note 1	100		175	Ω
14714	MI_MONITOR HiZ Leakage	VCC = +13.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V	–10	< 0.1	+10	nA
14715	MONITOR Short Circuit Current	IR5, FV-Mode = 0, FV = +3V, output shorted to ground; Note 1	5	10	15	mA
14716	MI_MONITOR Short Circuit Current	IR5, FV-Mode = 0, FV = +3V, output shorted to ground; Note 1	5	10	15	mA

NOTES:
1. VCC = +12V, VCCO_# = +6V, VEE = –4V, VDD = +3.3V.

DC Electrical Specifications – Switch Resistance Values

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
On-Chip Switches						
19200	Tj-En		100		175	kΩ
19210	Con-ES-F#		0.75		1.65	kΩ
19220	Con-EF-F#		11		35	Ω
19230	Con-ES-S#		1.75		3	kΩ
19240	Con-FS#		0.75		1.25	kΩ
19250	Con-EF-ES#	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V, VOH-SDIO = VDD, V_REF = +3V, DUT_GND = 0	0.75		1.65	kΩ

DC Electrical Specifications – Kelvin Alarms

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Kelvin Alarm High and Low						
14400	Gain	All codes tested vs their nominal program values	150	150	300	mV/code
14410	Offset	All codes tested vs their nominal program values	150	150	300	mV
14420	Linearity Error	All codes tested vs their nominal program values	-100		+100	mV
14430	Hysteresis	Not production tested.	10	40	100	mV

DC Electrical Specifications – Central Level Gain and Offset

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain Test						
16390	MaximumGain	AV#<7:0> = 7F Hex; Note 1	960		985	mV/V
16391	Minimum Gain	AV#<7:0> = FF Hex; Note 1	1010		1050	mV/V
16392	Linearity	Note 2		0.25		mV/V
16393	Bit Test	Note 3		0.25		mV
16295	Resolution	Note 4		185		µV/V
	Span	(AV Gain Max) – Av Gain Min)		90		mV
Offset Test						
16290	Maximum Offset	OS#<15:0> = FF Hex; Note 1	–100		–60	mV
16291	Minimum Offset	OS#<15:0> = 7F Hex; Note 1	60		100	mV
16292	Linearity	Note 5		0.05		mV
16294	Span Test	(OS Max) – (OS Min)		170		mV
	Resolution	Note 6		650		µV

NOTES:

1. Central DAC tests performed in FV mode tested and at Force A at 2V.
2. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and7/8 codes: 7F, 6F, 5F, 4F, 3F, 2F, 1F, 0F, 8F, 9F, AF, BF, CF, DF, EF, FF. Actual measurement vs. straight line determined by the calibration points.
3. B it Test - Walking 1 and walking 0 to determine the bit weight. 1's - 40, 20, 10, 08, 04, 02, 01, C0, A0, 90, 88, 84, 82, 81. 0's - 3F, 5F, 6F, 77, 7B, 7D, 7E, BF, DF, EF, F7, FB, FD, FE. Actual measurement vs. straight line determined by the calibration points.
4. Gain Resolution Test: (AV-Gain<4C> – AV-Gain <CC>/ 152..
5. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 codes: 0000, 0FFF, 1FFF, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, DFFF, EFFF, FFFF. Actual measurement vs. straight line determined by the calibration points.
6. Offset resolution test –(Offset at level <4C> – Level <CC> / 152.

DC Electrical Specifications – ESP

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Compensation Range	Sel-MI4# = 0		4.5		Ω
	Resolution			18		mΩ/code
	Linearity			50		mΩ
	Compensation Range	Sel-MI4# = 1		45		Ω
	Resolution			180		mΩ/code
	Linearity			5		mΩ

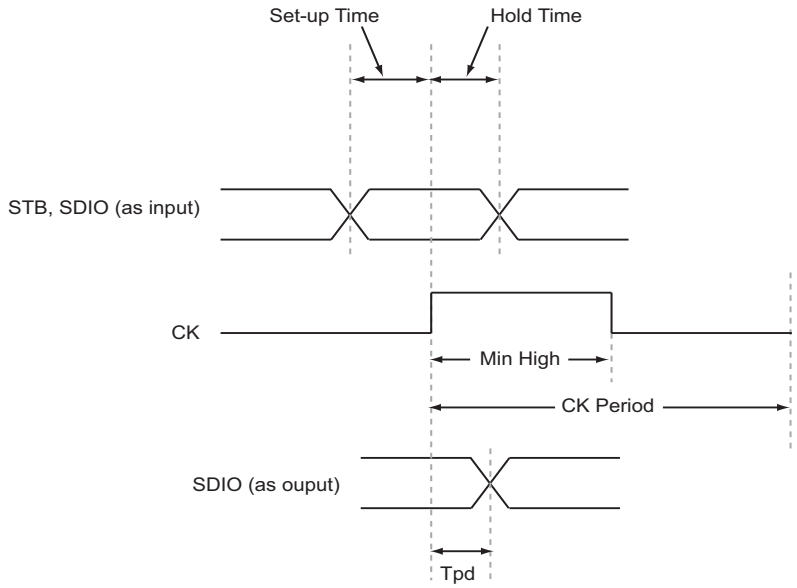
AC Characteristics

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications– CPU Port

VCC = +13V, VCC0_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Setup Time SDIO to Rising CK STB to Rising CK		 10 10			 ns ns
	Hold Time SDIO to Rising CK STB to Rising CK		 10 10			 ns ns
27140	CK Minimum Pulse Width High		20			ns
27150	CK Minimum Pulse Width Low		20			ns
27160	CK Period		40		100	ns
27180	**Propagation Delay** Rising CK to SDIO Out				15	ns
27170	Reset Minimum Pulse Width		100			ns



AC Electrical Specifications – DPS

VCC +13V, VCCO_# = +5V, VEE = –3V, VDD = +3.30V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Settling times measured from 50% of final value to within 2% of final value. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV SETTLING TIME						
	IR0			8		µs
	IR1 - IR5	0V to 3V step using DATA_# pin to switch between ForceA# and ForceB#. Con-Cap# = 0, Con-Res# = 0. Bbias# = 1. Resistive Load = 0Ω. Capacative Load = 10nF.		5		µs
MV SETTLING TIME						
	4V Range	MV		3		µs
	8V Range	MV		3		µs
	16V Range	MV		3		µs
MI SETTLING TIME						
	IR0	FV Mode. Load step from 0 to +Imax. Capacative Load = 1nF. Con-Cap#<0,1,2> = 1. Con-Res# = 0. Bbias = 0.		130		µs
	IR1			65		µs
	IR2			35		µs
	IR3	FV Mode. Load step from 0 to +Imax. Capacative Load = 10nF. Con-Cap# = 0. Con-Res# = 0. Bbias = 0.		9		µs
	IR4			5		µs
	IR5			5		µs

Chip Overview

ISL55180 is a highly integrated SOC DUT power supply solution incorporating 8 independent DPS units.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per channel basis.

CPU Control

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses.

Real Time Control

Real time control is accomplished via the central EN and DATA_# pins. Real time observation is accomplished via the central monitor.

Analog References

All on chip analog levels are related to off-chip precision voltage and resistance references:

- V_REF
- R_EXT

These external references are used to provide accurate and stable analog circuit performance with minimal variation over time, temperature, supply voltage, part-to-part, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

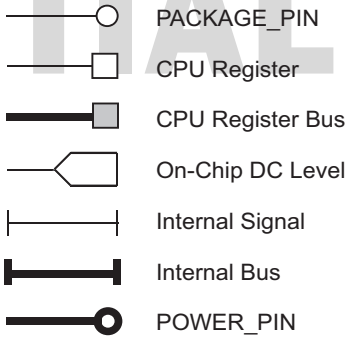
1. All capital letters (i.e. FORCE_0, CK, SDIO)
2. Underscores for clarity (i.e. SENSE_0)
3. Shown next to an I/O circle in any schematic

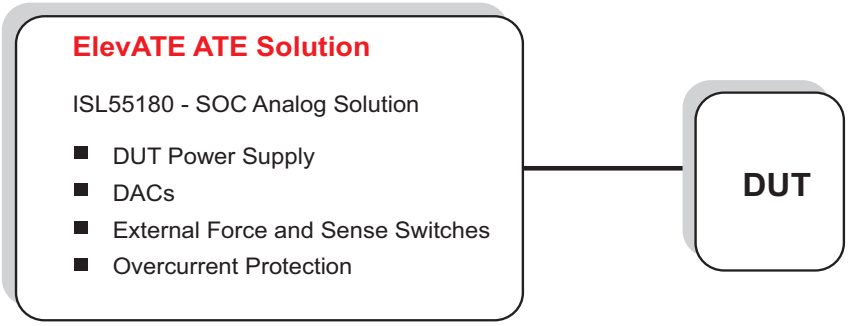
CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1. The first letter in a word is always a capital letter
2. Subsequent letters within the same word are small
3. Dashes *(but never an underscore)* for clarity
4. NOT shown with an I/O circle in any schematic

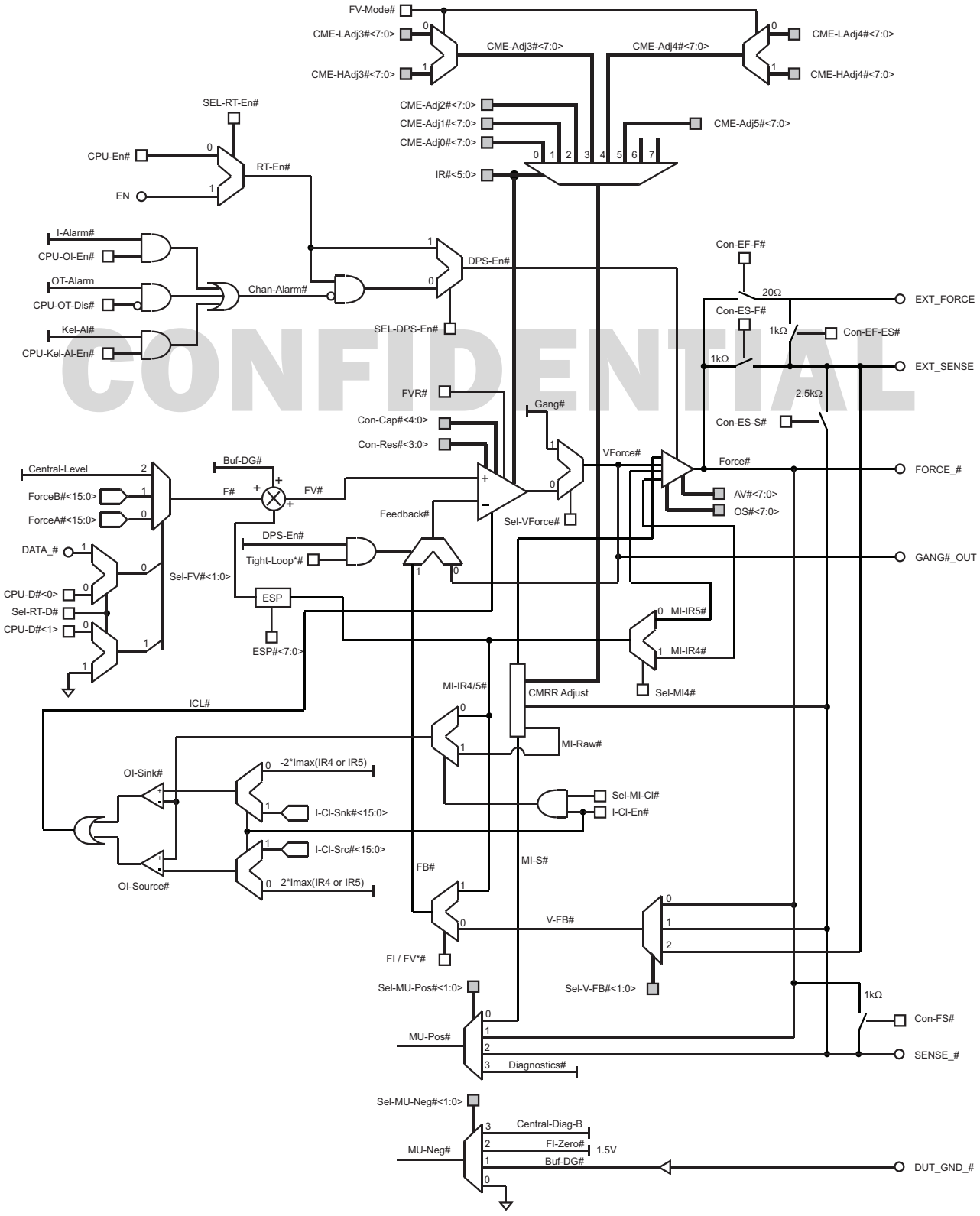
Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.



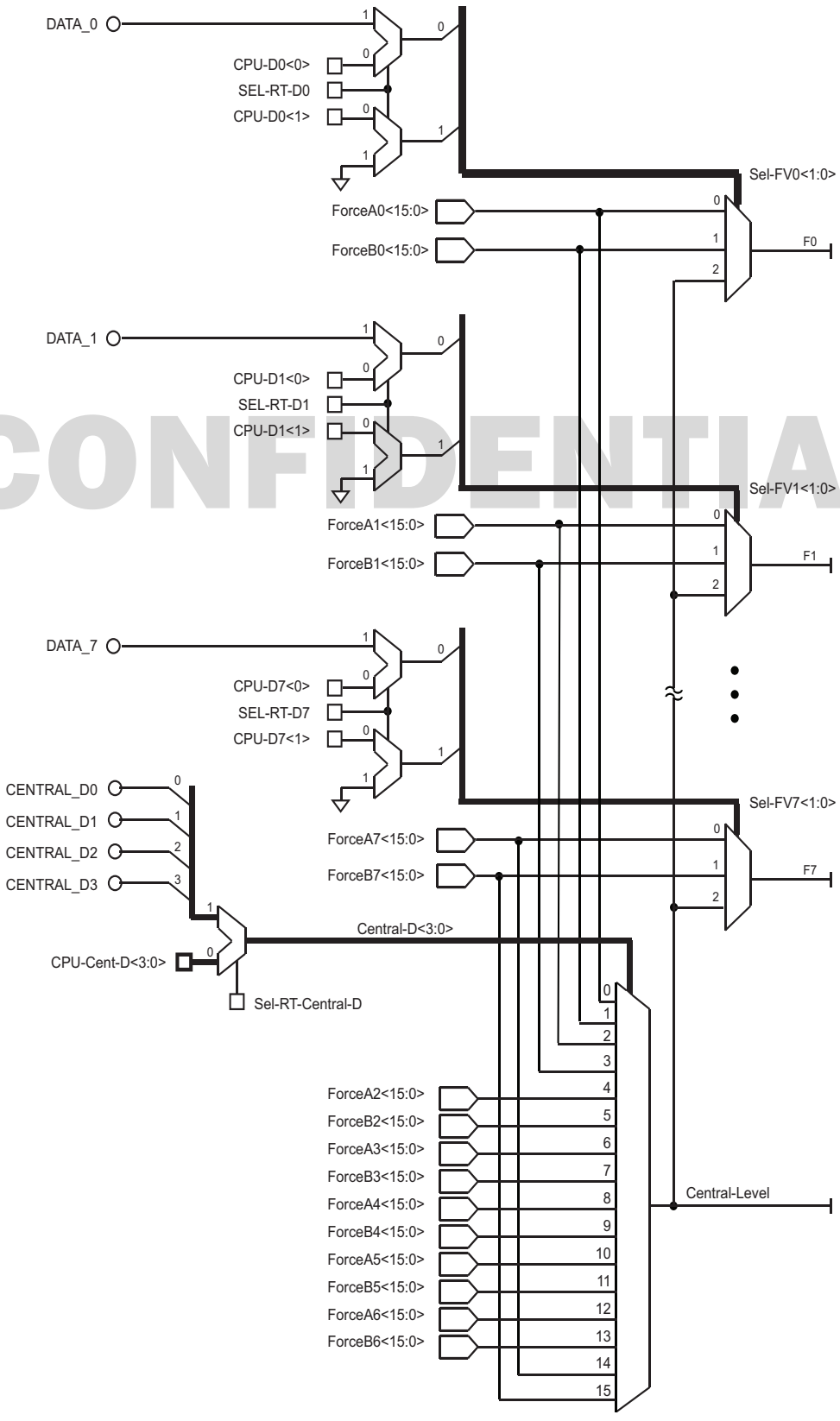


Block Diagrams

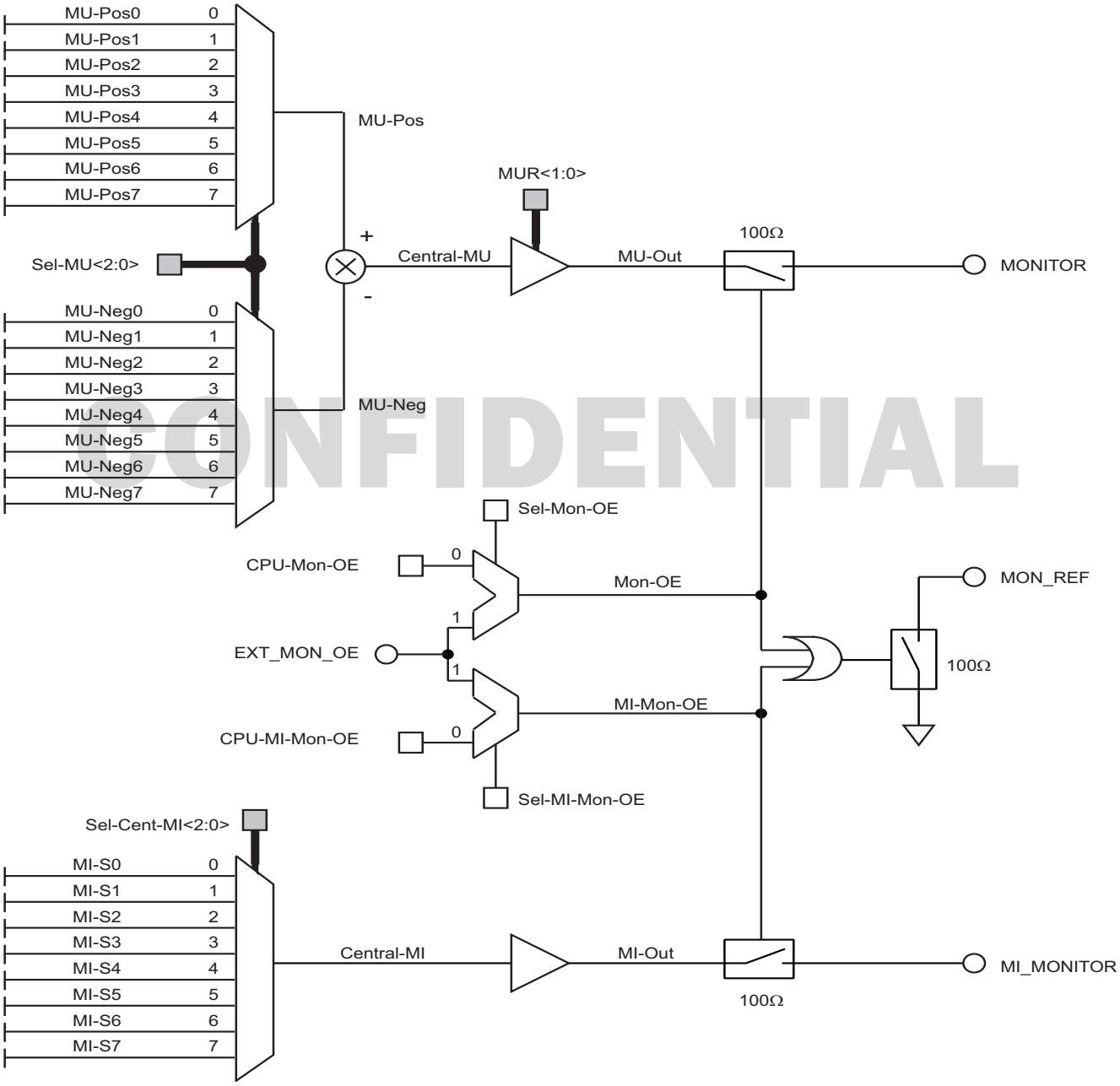
Per Channel Diagram



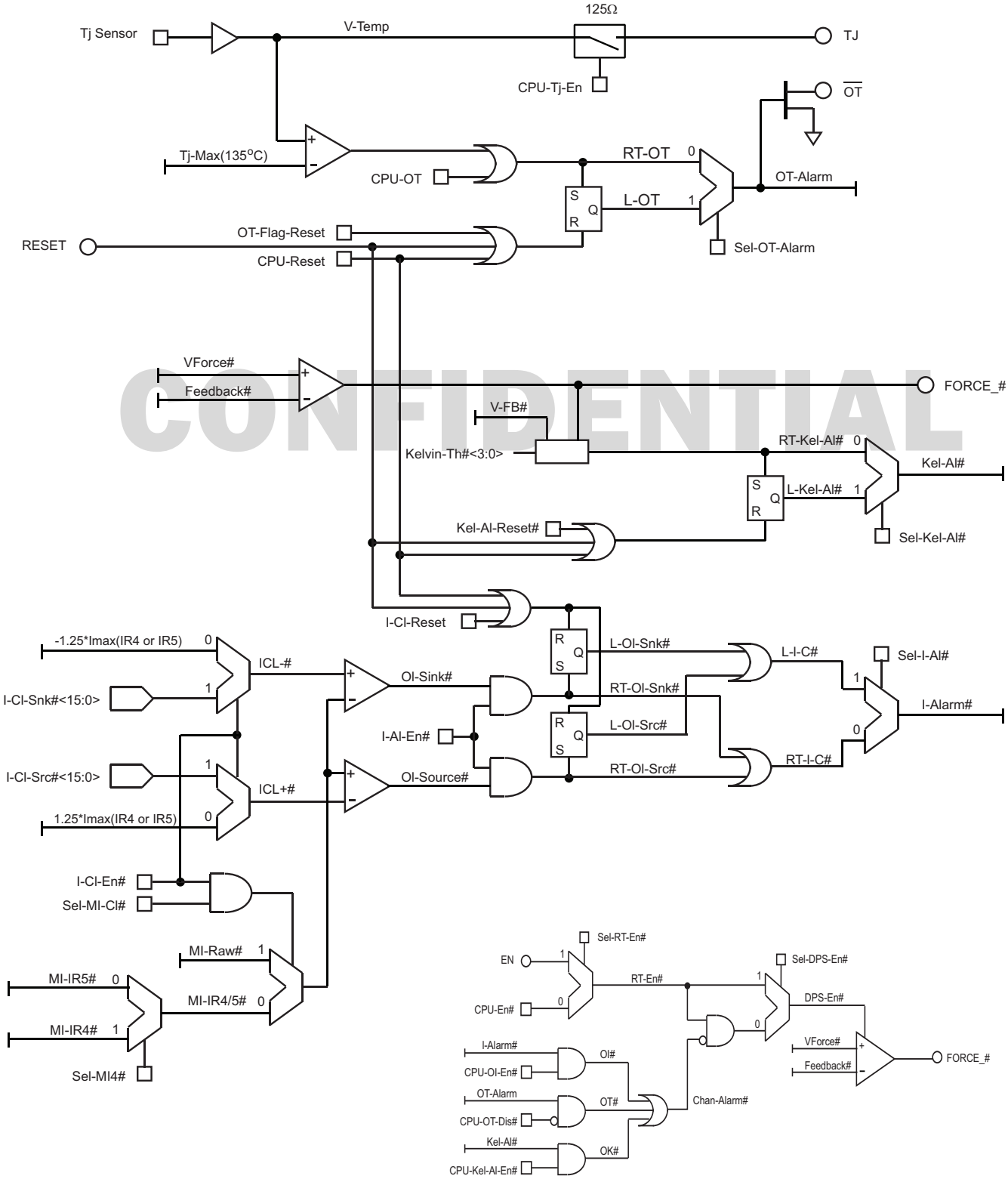
Central Resource vs. Channel Mode



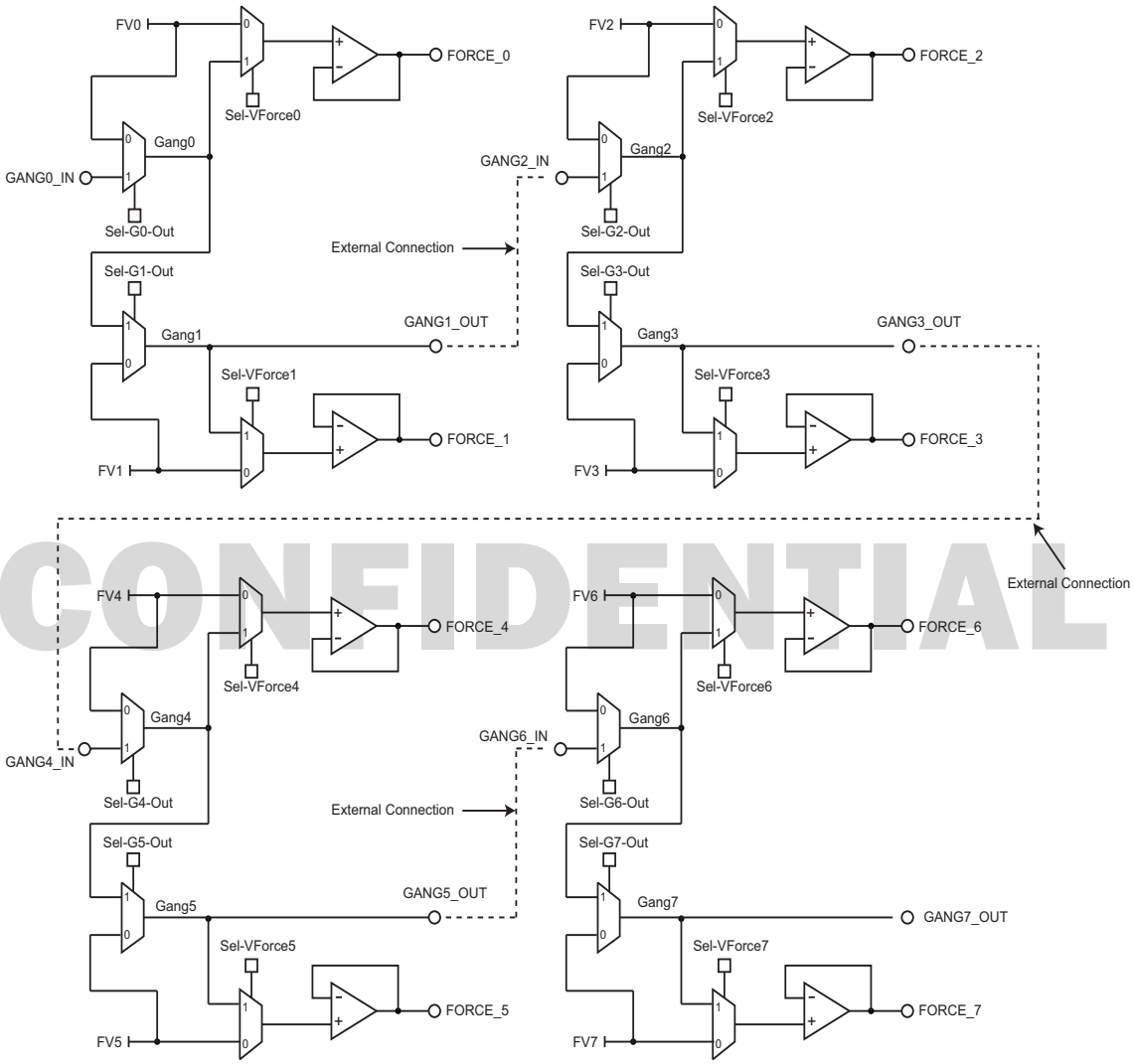
Measurement Unit



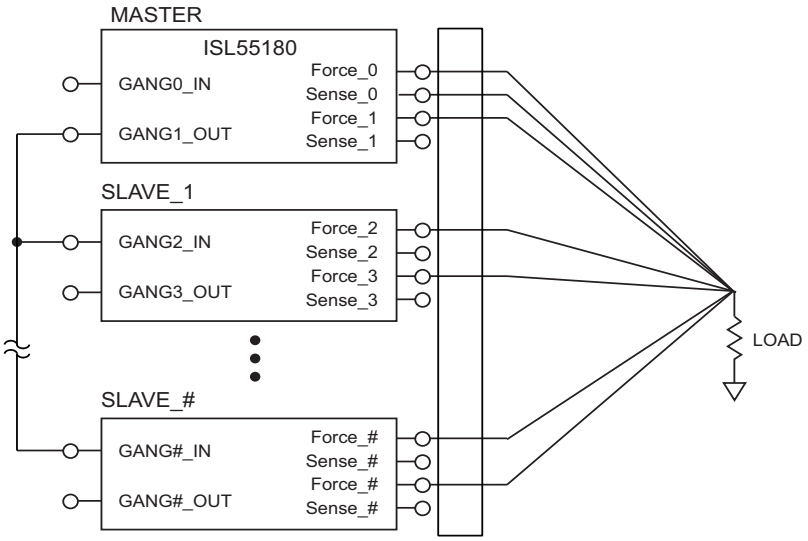
OI, OT and Kelvin Alarm



Serial Ganging with One Chip



Ganging Across Multiple ISL55180's



Overview

Each channel is independent and has the ability to:

Force:

- Force Voltage (FV)
- Force Current (FI)
- Go into a HiZ state

Measure:

- Measure Voltage (MV)
- Measure Current (MI)

Gang:

- Gang with other channels for extended current capability

There are no restrictions between which parameter is being forced and which is being measured.

Mode Selection

The CPU port establishes the operating mode of the chip.

TABLE 5. FORCE MODE

Sel-VForce#	MODE	VForce#	FI/FV*#	I-Clamp-EN#
0	FV	FV#	0	0, 1
1	Gang	Gang#	0	N/A
0	FI	FV#	0	1
0	Not Supported	FV#, Gang#	1	0,1

Current Ranges

The CPU port selects the current range. Each range is set independently, allowing flexibility in “make-before-break” options.

TABLE 6. CURRENT RANGES

RANGE	IR#<5:0>	IMAX
IR0	000001	±2.56µA
IR1	000010	±25.6µA
IR2	000100	±256µA
IR3	001000	±2.56mA
IR4	010000	±25.6mA
IR5	100000	±256mA

There is a transfer function between the current at the force pin and the voltage measuring the current at the MONITOR or MI_MONITOR pin. It is important to note that Imax (maximum current) is not the maximum current that the DPS can output at each current range. Imax is the full-scale current that can be measured in each current range.

TABLE 7. MEASURE CURRENT

CURRENT @ FORCE_#	MI# (Measure Current)
+Imax	+2.033V V(MI(+Imax))
0	+1.5V MI-Zero#
-Imax	+0.967V V(MI(-Imax))

High Impedance

Each channel may be placed in a HiZ state where it maintains an extremely low leakage as long as the FORCE_# output pin remains between the analog power supply rails.

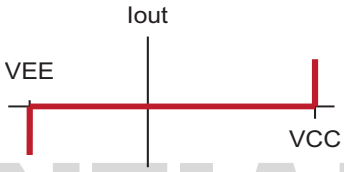


FIGURE 1. LEAKAGE CURRENT ACROSS VOLTAGE RANGE

TABLE 8. HIZ MODE SELECTION

DPS-En#	CHANNEL # DPS STATUS
0	HiZ
1	Active

TABLE 9. HIZ MODE CONTROL

Sel-RT-En#	Sel-DPS-En#	DPS-En#
0	1	CPU-En#
1	1	EN
X	0	RT-En# • $\overline{\text{Chan-Alarm\#}}$

HiZ can be controlled by the CPU port, an external real time input pin, or alarm signal. The EN pin is common for all channels. The alarm signal is unique for each channel. The CPU port exercises enable control on a per channel basis.

Channel Alarm

Each channel may be placed into HiZ based upon:

- an overcurrent situation
- an over-temperature situation
- a Kelvin alarm

OI# = I-Alarm# • CPU-OI-En#

OT# = OT-Alarm • CPU-OT-Dis#

OK# = Kel-AI# • CPU-Kel-AI-En#

Chan-Alarm# = OI# + OT# + OK#

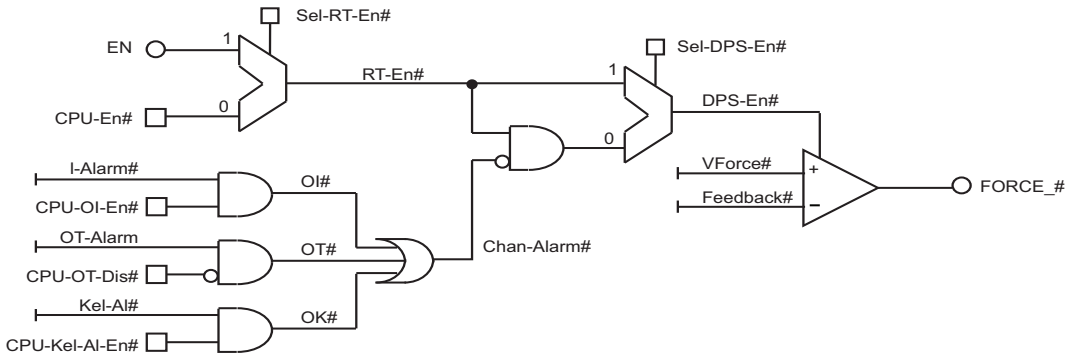


FIGURE 2. DPS FORCING CIRCUITRY

Force Voltage

The CPU port can place the DPS in FV mode. In FV mode, the voltage at FORCE_# is offset by and will track any changes in DUT_GND#.

The resulting forcing voltage is FV# = F# + Buf-DG# + ESP#

TABLE 10. DPS MODE CONTROL

Sel-VForce#	DPS MODE
0	FV
1	Gang

Forcing Op Amp Input Source

The ISL55180 supports a wide variety of inputs that are used to drive the main forcing op amp. This selection can be made by the CPU Port or by an external real-time pin which controls the Sel-FV#<1:0> bits. Sel-FV#<1:0> can also be read back through the CPU Port.

TABLE 11. DAC LEVEL SELECTION

Sel-RT-D#	Sel-FV#<1:0>
0	CPU-D#<1:0>
1	<0, DATA_#>

TABLE 12. DAC LEVEL ROUTING

Sel-FV#<1:0>	MODE	F#
00	Per Channel	ForceA#<15:0>
01	Per Channel	ForceB#<15:0>
10	Central Resource	Central-Level
11	External Resource	Ext-DAC (Test+/Test–)

Per Channel Mode

In per-channel mode, each channel has two independent levels, ForceA# and ForceB#, that may be selected as the input to the forcing op amp.

The ForceA#/ForceB# selection may be made by the CPU port or by an external real-time pin.

Central Resource Mode

In central resource mode, each channel may select any of the 16 levels on the chip as the input to the forcing op amp.

The central level is selected from all of the per-channel DC levels.

TABLE 13. CENTRAL DAC LEVEL SELECTION

Central-D<3:0>	Central-Level
0000	ForceA0
0001	ForceB0
0010	ForceA1
0011	ForceB1
•	•
1110	ForceA7
1111	ForceB7

The central DC level selection can be made by the CPU port or by external real-time pins.

TABLE 14. CENTRAL DAC LEVEL OPTIONS

Sel-RT-Central-D	Central-D<3:0>
0	CPU-Cent-D<3:0>
1	CENTRAL_D<3:0>

External Resource Mode

In external resource mode, the forcing op amp may be driven by an external differential DAC. This would typically be used in applications where extremely precise levels are required. The TEST+ and TEST- pins are used as differential inputs which are then combined into a single-ended input into the main forcing op amp. The Central Level Offset and Gain calibration registers may be used to calibrate out any errors introduced by the main forcing op amp. The input operating voltage range for the TEST+/TEST- pins are limited to VDD and GND.

FORCE# output is dependent on the FVR# (Voltage Range Selection) bit, and the differential voltage between TEST+ and TEST-. To maintain proper functionality, the common mode

voltage should also be approximately 1.875V. The transfer function is shown below.

TABLE 15.

((TEST+)–(TEST–))	Recommended TEST+ Voltage	Recommended TEST– Voltage	FORCE# Voltage (FVR#=0)	FORCE# Voltage (FVR#=1)
–1.65V	1.05V	2.70V	–2V	–2V
0V	1.875V	1.875V	+2V (=VMID)	+6V(=VMID)
1.65V	2.70V	1.05V	+6V	+14V

Central Level Calibration

Each channel has a separate offset and gain correction that is independent from the gain and offset associated with each DC level. This additional calibration path allows for accurate outputs when in the central resource mode.

TABLE 16. CENTRAL DAC OFFSET CALIBRATION REGISTERS

OS#<7:0>	CH# OFFSET (16V)	CH# OFFSET (8V)
11111111	–160mV	–80mV
11111110	–158.74mV	–79.37mV
•	•	•
10000000	0mV	0mV
00000000	0mV	0mV
•	•	•
01111110	+158.74mV	+79.37mV
01111111	+160mV	+80mV
Resolution	1.26mV	0.63mV

TABLE 17. CENTRAL DAC GAIN CALIBRATION REGISTERS

AV#<7:0>	GAIN ADJ (16V)	GAIN ADJ (8V)
11111111	.9492	.9746
11111110	.9496	.9748
•	•	•
10000001	.9996	.9996
10000000	1.000	1.000
00000000	1.0000	1.0000
00000001	1.0004	1.0002
•	•	•
01111110	1.0504	1.0252
01111111	1.0508	1.0254
Resolution	400µV/V/Code	200µV/V/Code

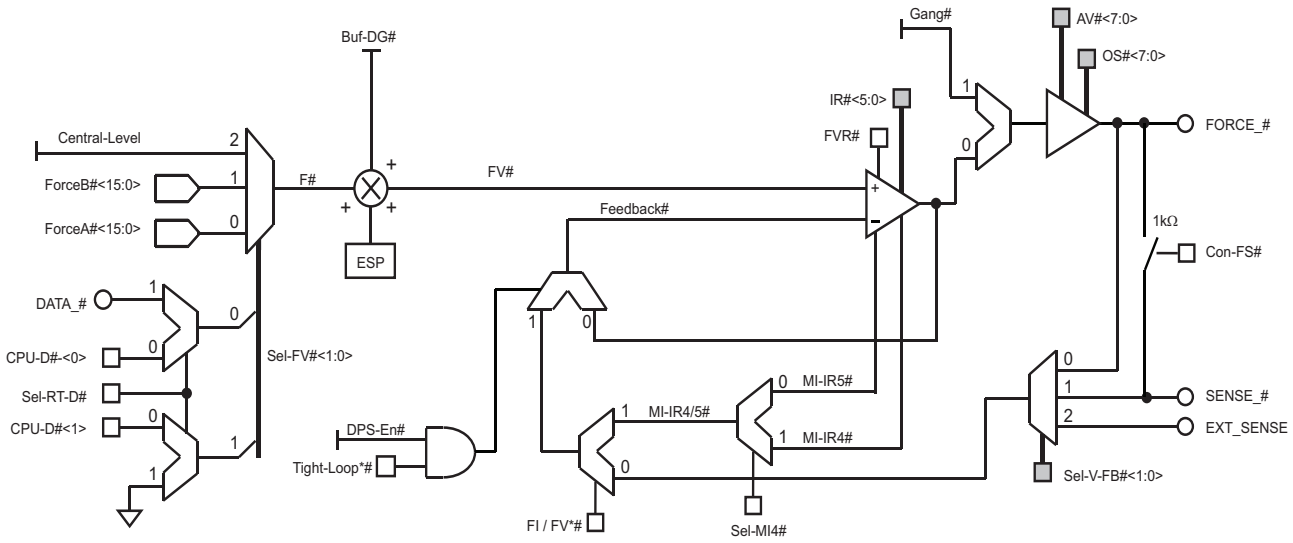


FIGURE 3. DPS CHANNEL USING CENTRAL LEVEL

FV Mode

The CPU port can establish the force voltage mode of the DPS on a per-channel basis.

TABLE 18. FV MODE SELECTION

FV-MODE#	DPS MODE
0	High Current (uses VCCO_#)
1	Low Current (uses VCC)

In the high curent range, the DPS supports all current ranges. In the low current range, the DPS supports all but the highest current range but over a wider voltage range (patented).

TABLE 19. FV MODE VS IRANGE SELECTION

FV-MODE#	I RANGE	Iout = ±Imax	Iout = 0
0	IR0 to IR5	VEE +3.0 to min of (VCCO – 0.5) or (VCC – 2.5)	VEE + 1.5 to min of (VCCO – 0.15) or (VCC – 1.0)
1	IR0 to IR4	(VEE + 2.0V) to (VCC – 1.5)	VEE + 1.5 to VCC – 1.0
1	IR5	N/A	N/A

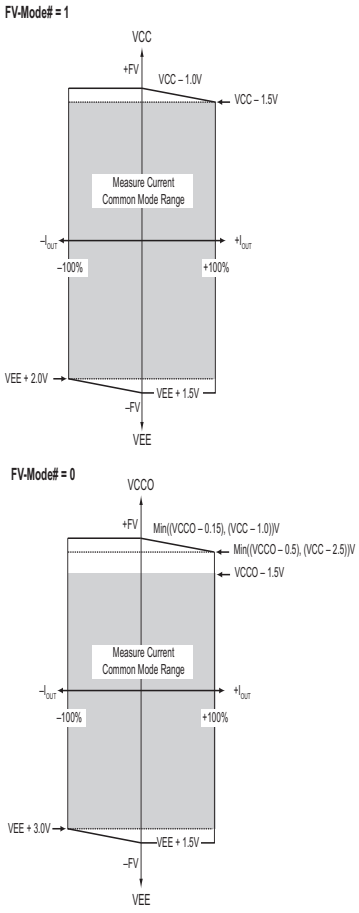


FIGURE 4.

VCCO_#

VCCO_# is the per-channel positive power supply of the output stage for high current operation. In order to minimize power consumption in high current, low voltage applications, VCCO_# should be as low as possible while still maintaining adequate headroom.

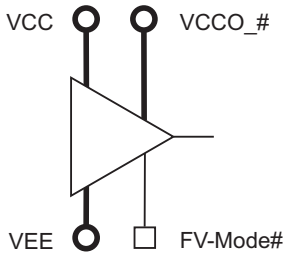


FIGURE 5. EACH DPS CHANNEL HAS A DEDICATED SUPPLY INPUT PIN, VCCO_#

BBIAS

The ISL55180 is a multi-stage output DPS consisting of a low current and a high current stage. Using the CPU port, the BBias# bit can control the turn-on point for the high current output stage. Under normal usage (BBias# = 0), the high current stage will start to automatically turn on when the low current stage reaches between 0.5mA to 1.0mA. With the BBias# bit set high, the second stage is turned on under all conditions. This will lower the AC output impedance, thus improving the load transient response when going from a low current state to a high current state.

NOTE: The output is virtually glitchless when switching from BBias# = 0 to BBias# = 1 or BBias# = 1 to BBias# = 0 and takes approximately 50µs. Setting BBias# = 1 also adds approximately 3mA to the VCCO+# supply per channel.

TABLE 20. BBIAS RECOMMENDED MEASURE CURRENT RANGES

BBias#	Output	Recommended Measure Current Ranges
0	High current stage becomes Active when low current stage reaches 0.5mA to 1.0mA	IR0, IR1, IR2, IR3, IR4, IR5
1	High current and low current stage Active at all times	IR4, IR5

Measure current can be performed in IR4 and IR5 with BBias# set to 0 or 1, although the user should calibrate and measure with the same BBias# setting.

VOLTAGE FEEDBACK OPTIONS

There are multiple voltage feedback nodes to the inverting input of the forcing op amp. The forcing op amp is automatically protected against going open loop when the DPS goes into HiZ. The default condition upon power-up or chip reset is tight loop.

TABLE 21. VOLTAGE FEEDBACK OPTIONS

Tight-Loop*#	DPS-En#	Sel-V-FB#<1:0>	FI/FV*#	Feedback#	Mode
0	X	X	X	VForce#	Tight Loop
X	0	X	X	VForce#	Tight Loop
1	1	00	0	FORCE_#	Local Sense
1	1	01	0	SENSE_#	Remote Sense
1	1	10	0	EXT_SENSE	Calibration
1	1	11	0	N/A	N/A

VOLTAGE RANGE SELECTION

The CPU port may select one of two voltage ranges.

TABLE 22. VOLTAGE RANGE SELECTION

FVR#	VOLTAGE RANGE (V)
0	8
1	16

TABLE 23. 8V RANGE DAC MAPPING

8V RANGE	PROGRAMMED DC LEVEL (V)
0000 Hex	-2
FFFF Hex	+6

NOTE: DAC Resolution = 122µV

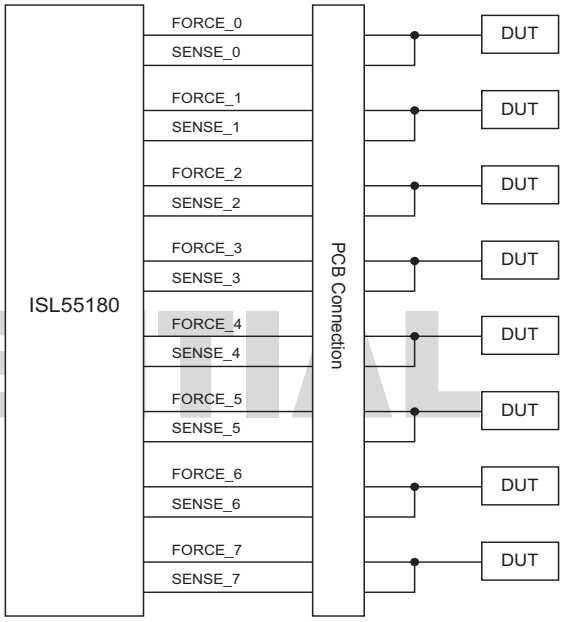
TABLE 24. 16V RANGE DAC MAPPING

16V RANGE	PROGRAMMED DC LEVEL (V)
0000 Hex	-2
FFFF Hex	+14

NOTE: DAC Resolution = 244µV

High Density DPS Connectivity Using “ESP”

The ISL55180 includes a breakthrough feature called “ESP” that enables customers to attain up to 2 times the DPS density through a given PCB connector for extremely high density DPS connectivity. ESP can be used to effectively “**E**liminate the **S**ense **P**in” from DPS Kelvin connections without significantly increasing voltage errors due to series resistance in the DPS output path.



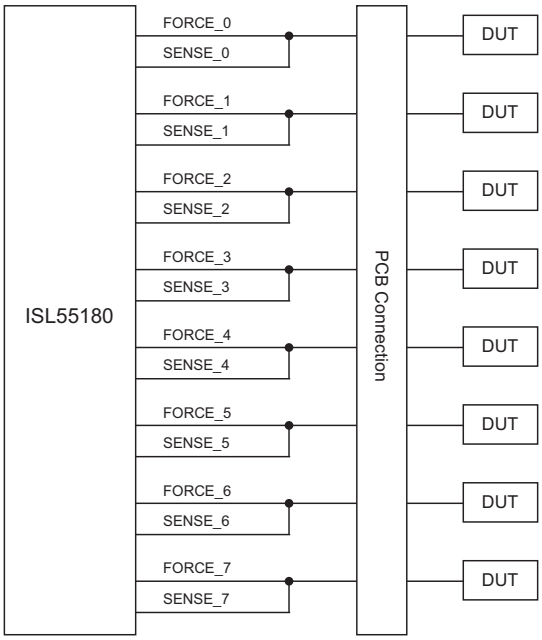


FIGURE 6.

The ISL55180 contains a per-channel, 8-bit register named ESP#. The contents of this register are used to compensate for series resistance between a given DPS FORCE_# pin and the

device under test. Range and effective resolution for ESP is a function of which voltage range is selected as follows:

TABLE 25.

Sel-MI4#	ESP# Compensation Range	Resolution
0	4.5Ω	18mΩ
1	45Ω	180mΩ

TABLE 26.

ESP# Code	ESP# Compensation Value
0000 0000	Zero (Transparent)
1111 1111	Maximum Resistance Compensation

ESP range and resolution is also a function of how many channels are ganged together in parallel. As channels are ganged in parallel, the effective ESP compensation range and resolution is divided by the number of channels being connected in parallel. For example, if 4 DPS channels are ganged and Sel-MI4# = 0 to create a 1 amp supply, the effective ESP compensation range is (4.5/4Ω) and the resolution is (18/4mΩ.).

Current Clamps

Each channel has current clamps that limit the amount of current flow. The current flow is limited internally by reducing the force voltage level until the current is within the programmed levels. There are independent clamps for both sourcing and sinking. The CPU port controls the clamp function.

TABLE 27. CURRENT CLAMPS

I-CL-EN#	CURRENT CLAMPS	CLAMP LEVELS
0	Disabled	±2*Imax(IR4 or IR5)
1	Enabled	I-Cl-Src#/I-Cl-Snk#

Short Circuit Limit

When the current clamps are disabled, the forcing op amp will limit its current flow to 200% Imax of either IR4 or IR5. This selection is made using Sel-MI4#.

Programmable Current Clamps

If the current flow exceeds the clamp limit, the forcing op amp will go into current limit mode.

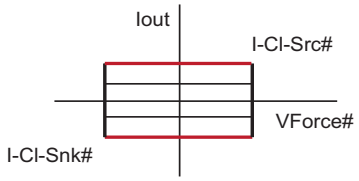


FIGURE 7. CURRENT CLAMP FUNCTIONALITY

The current clamp may be programmed to 150% of the maximum current flow in any range.

TABLE 28. CURRENT CLAMP DAC MAPPING

I-Cl-Src##<15:0> I-Cl-Snk#<15:0>	ICLAMP SOURCE	ICLAMP SINK
FFFF	+1.5 • Imax	-1.5 • Imax
•	•	•
8000	+0.75 • Imax	-0.75 • Imax
•	•	•
0000	0µA	0µA

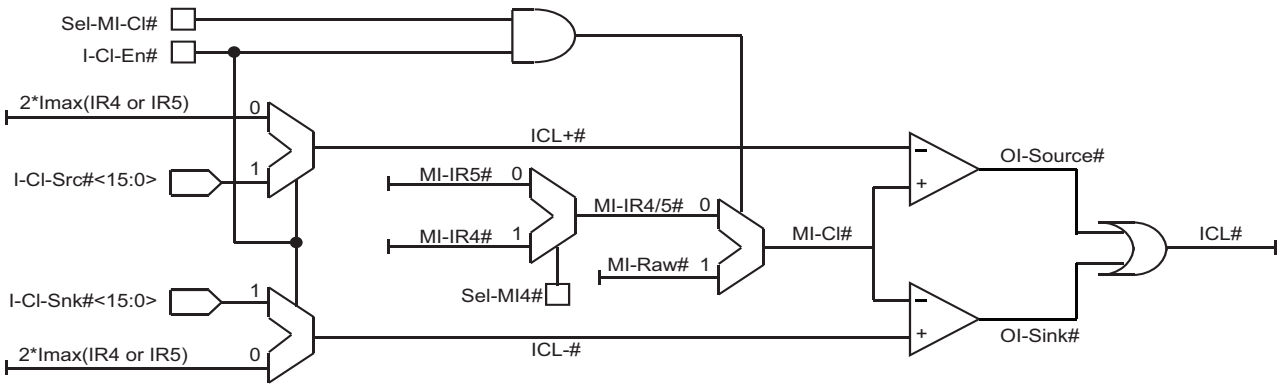


FIGURE 8. CURRENT CLAMPS

Clamp Source

The CPU port selects the signal source for the current clamps.

TABLE 29. CURRENT CLAMP SIGNAL SOURCE SELECTION

I-Cl-En#	Sel-MI-CL#	Sel-MI4#	MI-CL#
0	X	0	MI-IR5#
0	X	1	MI-IR4#
X	0	0	MI-IR5#
X	0	1	MI-IR4#
1	1	X	MI-Raw

MI-Raw# is a voltage that tracks current in the selected MI current range.

If Sel-MI-C# or I-Cl-En# = 0, the current clamps will track either MI-IR4# or MI-IR5# regardless of the MI current range. MI-IR4# or MI-IR5# is chosen using Sel-MI4#. This selection is useful when the clamps are used to protect the DUT and the DPS and when the measured current varies over a wide range. The DPS can measure a small current while still being able to source a large current with protection.

If MI-S# is selected, the current clamps will track the measure current range. This selection is useful when the clamps need to be programmed to a small value or when the DPS is used as a current source in FI mode.

TABLE 30. CURRENT CLAMP RANGES

CURRENT RANGE	ICLAMP RESOLUTION	±ICLAMP MAX
IR0	58.6pA	±3.84µA
IR1*	586pA	±38.4µA
IR2**	5.86nA	±384µA
IR3	58.6nA	±3.84mA
IR4	586nA	±38.4mA
IR5	5.86µA	±384mA

* IR1 not recommended for use due to stability issues.
**Must use CAP_A when using IR2 (set ther Con-Cap# bits to 3).

Force Current

Force Current mode is implemented by placing the part in Force Voltage mode and using the current clamps to set the Force Current value supplied to the DUT. In this situation, the Force Voltage output level is used as a voltage clamp level and protects the DUT from an over-voltage situation.

To configure in Force Current mode, perform the following:

- Disable ISL55180 (put in HiZ)
- Enable current clamps and set Current Clamp Level to Force Current required
- Set the Force Voltage level to the ground reference of the DUT
- Place the part in Force Voltage mode
- Connect Force Output to DUT
- Enable ISL55180
- Place the part in Force Voltage mode
- Set Force Voltage Level to the Voltage Clamp Level required. This wil allow current to flow, which will be limited by the current clamps.

Ganging

Individual DPS units may be ganged with sequential channels in a chain. The first DPS in the string is the master DPS. All subsequent DPS channels are slave units.

To create a high current DPS in FV mode the following steps are taken:

- Select a master DPS and place it in FV mode
- Connect the Gang# signal of the master channel to the input of all slave channels.

NOTE: Connection resistance should be minimized for best AC response.

Master DPS:

- Sel-VForce# = 0 (FV Mode)
- Sel-G#-Out = 0 (Master unit Gang# signal as forcing value)
- All Subsequent Slave Units:
  - Sel-G#-Out = 1 (Master unit Gang# signal as forcing value)
  - Sel-VForce# = 1 (Gang Mode)

NOTE: When ganging from an odd numbered channel to an even numbered channel, an external connection needs to be made as shown in Figure 9.

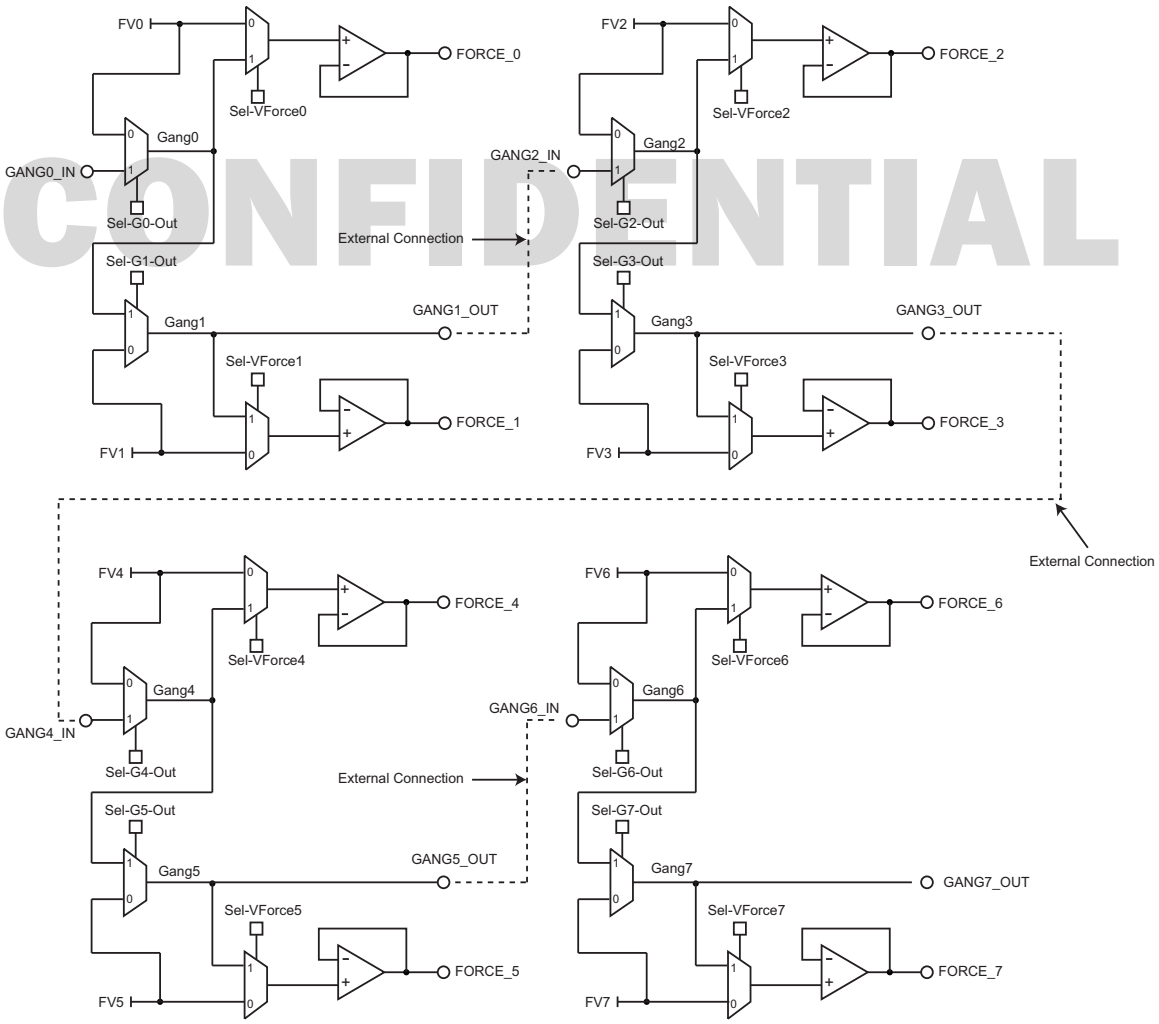


FIGURE 9. GANGING WITH ONE CHIP

Serial Chip-to-Chip Ganging

Ganged DPS strings may extend across multiple chips by connecting the GANG#_OUT pin of one chip to the GANG#_IN pin of the next chip in the chain.

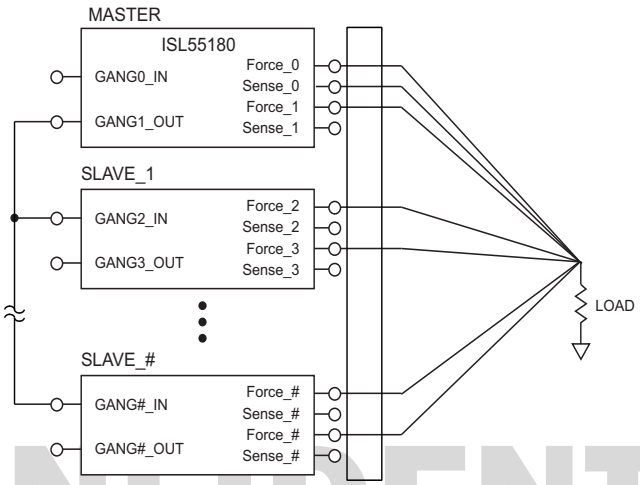


FIGURE 10. GANGING ACROSS MULTIPLE ISL55180's

Measurement Unit

There is a central measurement unit per chip that can track:

- The voltage at FORCE_#
- The voltage at SENSE_#
- The current at FORCE_#
- An internal diagnostic node

The measurement unit output is a voltage that is proportional to the current or voltage of the selected channel.

Measurement Unit Input Sources

Each channel generates a differential analog signal and sends it to the measurement unit. The positive and negative inputs may be selected from several potential sources.

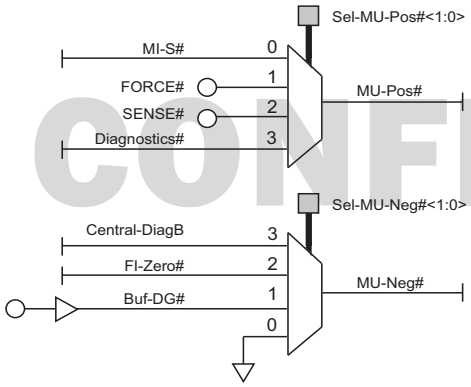


FIGURE 11. MEASUREMENT UNIT

TABLE 31. MEASUREMENT UNIT MODES

	MU-POS#	MU-NEG#	MODE
Sel-MU-Pos#<1:0>			
00	MI-S#		MI
01	FORCE_#		MV
10	SENSE_#		MV
11	Diagnostics#		Test & Cal
Sel-MU-Neg#<1:0>			
00		Chip Ground	Diagnostics
01		Buf-DG#	MV
10		FI-Zero#	MI
11		Central-Diag-B	Diagnostics

Measurement Unit Source Selection

The CPU port selects the channel to be used as the input to the measurement unit.

TABLE 32. MEASUREMENT UNIT SOURCE SELECTION

Sel-MU<2:0>	Central-MU
000	MU-Pos0 – MU-Neg0
001	MU-Pos1 – MU-Neg1
010	MU-Pos2 – MU-Neg2
011	MU-Pos3 – MU-Neg3
100	MU-Pos4 – MU-Neg4
101	MU-Pos5 – MU-Neg5
110	MU-Pos6 – MU-Neg6
111	MU-Pos7 – MU-Neg7

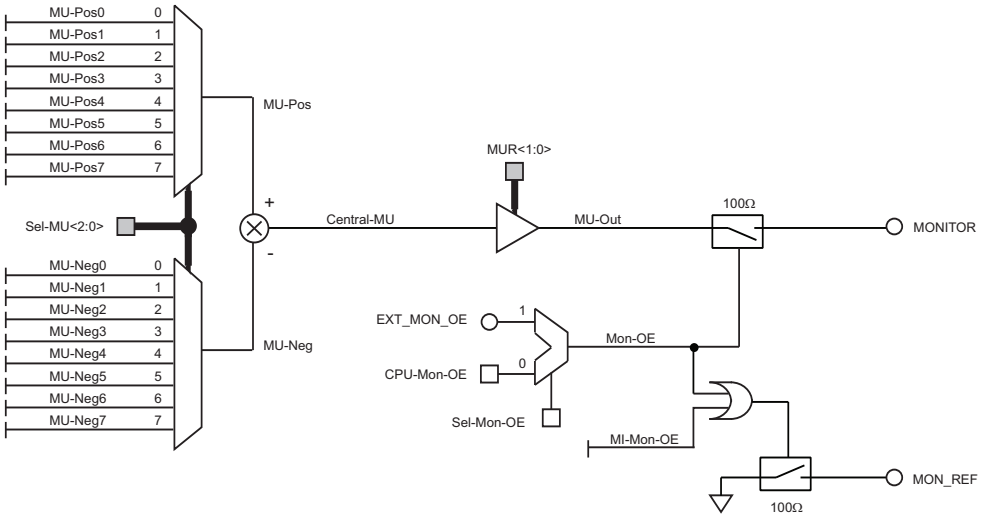


FIGURE 12. MEASUREMENT UNIT TO MONITOR ROUTING

Measure Voltage

The CPU port selects one of three MV ranges or the MI range.

TABLE 33. MV MAPPING

MUR<1:0>	00	01	10	11
Mode	MI	MV	MV	MV
VRange	N/A	4V	8V	16V
Input Range	±1.5 • Imax	0V/+4V	-2V/+6V	-2V/+14V
Monitor	1.5 ±0.8V	+0.5V/+2.5V	+0.5V/+2.5V	+0.5V/+2.5V
Av	1.3	0.5	0.25	0.125
Vos	1.5V	+0.5V	+1.0V	+0.75V

The MV ranges are designed to map the input voltage span to a 1.5V ±1V output voltage at the monitor. This mapping is useful when connecting to an external low voltage, positive input only ADC.

The monitor has the transfer function:

MONITOR = Av • Central-MU + Vos

Measure Current

The DPS supports 6 current ranges per channel, capable of measuring current accurately over the following common mode voltage range, VCM.

FV mode# = 0 (VEE + 3V) ≤ (VCCO – 1.5V)

FV mode# = 1 (VEE + 2V) ≤ (VCC – 1.5V)

TABLE 34. MI MAPPING

RANGE	IR#<5:0>	IMAX
IR0	000001	±2.56µA
IR1	000010	±25.6µA
IR2	000100	±256µA
IR3	001000	±2.56mA
IR4	010000	±25.6mA
IR5	100000	±256mA

The current sense line has the following transfer function.

TABLE 35. MI TRANSFER CHARACTERISTIC

IOUT#	MI-S#
+1.5 • Imax	+2.3V
+Imax	+2.033V
0	+1.5V (MI-Zero#)
-Imax	+0.967V
-1.5 • Imax	+0.7V

FI-Zero# is a per-channel DC reference voltage that corresponds to 0 current flow at the FORCE_# pin. MI-S# is a voltage that tracks the current in any given range. The current may exceed ±Imax and MI-S# will continue to track the current flow until the signal eventually saturates and will no longer accurately track the current flow.

To measure current for the region –10% to +100% of Imax in IR4 and IR5, switching to the next lower current range is recommended. This will provide the best MI performance.

Changing Current Ranges

When measuring current in the highest 5 ranges (IR1 – IR5) the forcing op amp does not react to changing the current range. Changing current ranges in between these selections will not cause any glitch or disturbance at the force output pin.

A small disturbance may be present at the output when changing ranges into or out of IR0.

CME (Common Mode Error) Calibration

The current measure (MI) transfer function will have some small amount of common mode voltage error as the FORCE output varies. Each current range on each channel has its own independent CME adjust code that is automatically selected by the current range selection.

TABLE 36. COMMON MODE ERROR ADJUSTMENT

FV-MODE#	IR#<5:0>	CME-Adj#<7:0>
X	000001	CME-Adj0#<7:0>
X	000010	CME-Adj1#<7:0>
X	000100	CME-Adj2#<7:0>
0	001000	CME-LAdj3#<7:0>
1	001000	CME-HAdj3#<7:0>
0	010000	CME-LAdj4#<7:0>
1	010000	CME-HAdj4#<7:0>
0	100000	CME-Adj5#<7:0>

The CME gain correction is superimposed on the nominal pre-calibration CME error in an effort to cancel each other out.

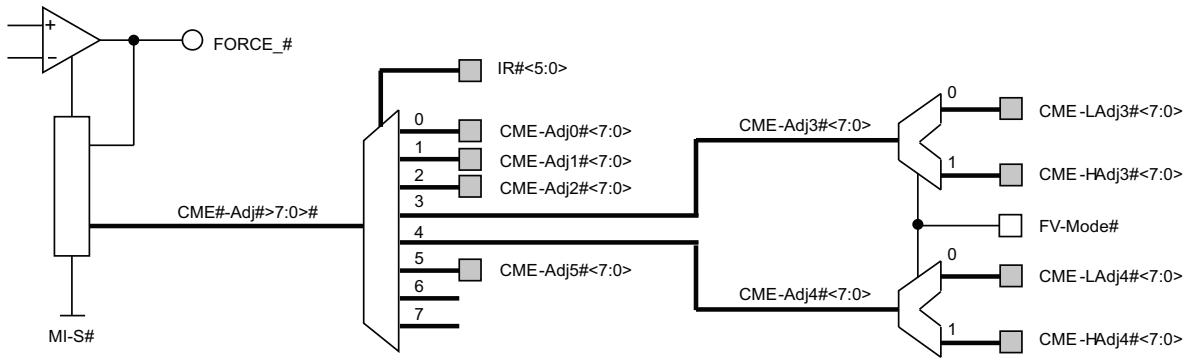


FIGURE 13. COMMON MODE ERROR CORRECTION CIRCUIT

IR3 and IR4

There are two separate ranges for IR3 and IR4; one for high current (FV-Mode = 0) and one for low current (FV-Mode = 1). Each range requires its own CME and MI calibration.

TABLE 37. COMMON MODE ERROR ADJUST RANGE

CME-ADJ#<7> (PARITY)	CME-ADJ#<6:0> (CODE)	CME ADJUSTMENT
0	1111111	1.0082677
0	1111110	1.0082026
•	•	•
0	0000010	1.0001302
0	0000001	1.0000651
0	0000000	1.0000
1	0000000	1.0000
1	0000001	0.9999349
1	0000010	0.9998698
•	•	•
1	1111110	0.9917974
1	1111111	0.9917323

NOTE: Resolution = 0.00651%/V (of Full Scale Current Range)

The default state is 00 Hex, which results in no CME calibration. By setting CME-Adj#<7:0> correctly, the actual transfer function can more closely track the ideal transfer function.

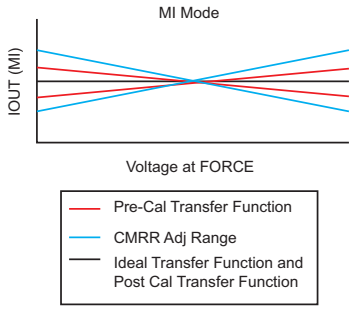


FIGURE 14. COMMON MODE ERROR ADJUSTMENT

Monitor Output Current Limiting

The monitor output is designed to mate directly with an ADC. To prevent damage to the ADC in cases where the monitor voltage exceeds in the input compliance of the ADC the monitor output current is limited to ~20mA.

Monitor High Impedance

The MONITOR output pin may be placed in a HiZ state where it maintains an extremely low leakage between GND and VDD. HiZ is useful to support the ganging of multiple MONITOR pins all connecting to the same external ADC.

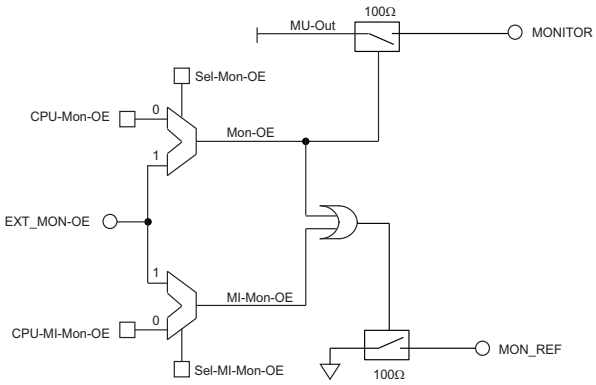


FIGURE 15. MONITOR CIRCUIT

TABLE 38. MONITOR FUNCTIONALITY

Mon-OE	MONITOR
0	HiZ
1	MU-Out

Monitor output enable may be controlled by the CPU port or by a real time monitor output enable pin.

TABLE 39. MONITOR CONTROL

Sel-Mon-OE	Mon-OE
0	CPU-Mon-OE
1	EXT_MON_OE

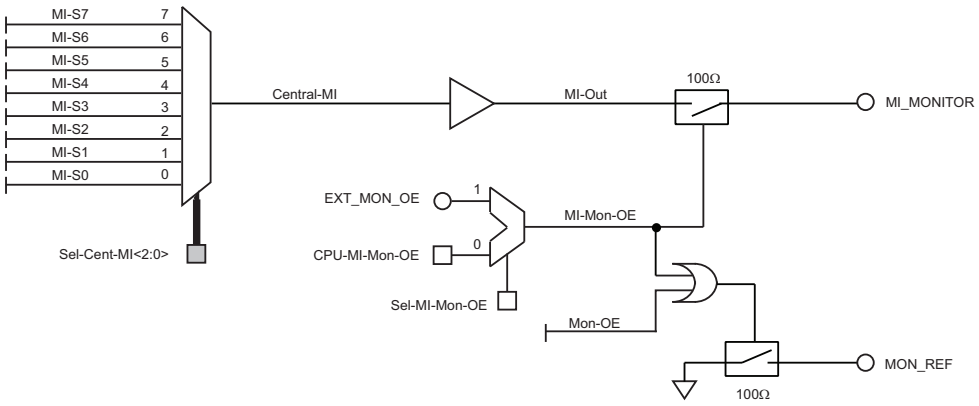


FIGURE 16.

Monitor Reference

MONITOR is always with respect to chip ground. MON_REF is the local chip ground and can be used as the reference signal if the ADC is far away and its ground level is not stable relative to the chip ground.

MON_REF is active whenever the MONITOR or MI_MONITOR is active.

TABLE 40. MONITOR REFERENCE

MI-Mon-OE	Mon-OE	MON_REF
0	0	HiZ
X	1	Active
1	X	Active

Measurement Current Monitor

There is a low voltage central monitor dedicated to the measure current function. The measure current monitor can be used in conjunction with the general-purpose monitor to capture both the voltage and the current at any channel simultaneously.

The CPU selects the source.

TABLE 41. CENTRAL MONITOR SELECTION

Sel-Cent-MI<2:0>	Central-MI
000	MI-S0
001	MI-S1
010	MI-S2
011	MI-S3
100	MI-S4
101	MI-S5
110	MI-S6
111	MI-S7

MI Monitor High Impedance

The MI_MONITOR output pin may be placed in a HiZ state where it maintains an extremely low leakage between the VDD and GND. HiZ is useful to support the ganging of multiple MI_MONITOR pins all connecting to the same external ADC.

FIGURE 17. MONITOR HiZ CURRENT

TABLE 42. MI_MONITOR FUNCTIONALITY

MI-Mon-OE	MI_MONITOR
0	HiZ
1	MI-Out

The measure current monitor output enable may be controlled by the CPU port or by a real time monitor output enable pin.

TABLE 43. MI_MONITOR CONTROL

Sel-MI-Mon-OE	MI-Mon-OE
0	CPU-MI-Mon-OE
1	EXT_MON_OE

MI Monitor Reference

MI_MONITOR is always with respect to chip ground. MON_REF is the local chip ground and can be used as the reference signal if the ADC is far away and its ground level is not stable relative to the chip ground.

MON_REF is active whenever the MONITOR is active.

TABLE 44. MI_MONITOR REFERENCE FUNCTIONALITY

MI-Mon-OE	Mon-OE	MON_REF
0	0	HiZ
X	1	Active
1	X	Active

External Force and Sense

There are external force and external sense pins that bypass the DPS completely and provide direct access to the FORCE and SENSE pins, which is useful for:

- Connecting an external PMU to the DUT
- Direct measurement of the DUT voltage
- DC Calibration

EXT_FORCE

Each channel may be connected to the EXT_FORCE pin through an on-chip switch.

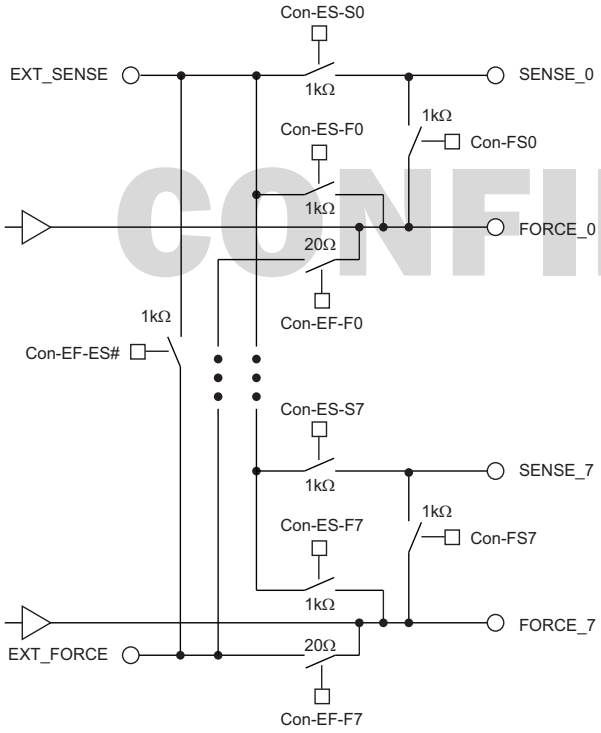


FIGURE 18. EXTERNAL FORCE/SENSE CIRCUITRY

TABLE 45. EXTERNAL FORCE-TO-FORCE SWITCH FUNCTIONALITY

Con-EF-F#	EXT_FORCE to FORCE_#
0	Disconnected
1	Connected

EXT_SENSE

Each channel may have its FORCE_# or SENSE_# pin connected to the EXT_SENSE pin.

TABLE 46. EXTERNAL SENSE-TO-FORCE SWITCH FUNCTIONALITY

Con-ES-F#	EXT_SENSE TO FORCE_#
0	Disconnected
1	Connected

TABLE 47. EXTERNAL SOURCE-TO-SENSE SWITCH FUNCTIONALITY

Con-ES-S#	EXT_SENSE TO SENSE_#
0	Disconnected
1	Connected

EXT_FORCE/EXT_SENSE SWITCH

The CPU port can connect EXT_FORCE and EXT_SENSE together. This connection may be useful for calibration.

TABLE 48. EXTERNAL FORCE TO EXTERNAL SENSE SWITCH FUNCTIONALITY

Con-EF-ES	EXT_FORCE to EXT_SENSE
0	Disconnected
1	Connected

Force/Sense Connect Switch

The CPU port can connect the force and sense pins via an on-chip switch. This connection may be useful for calibration.

TABLE 49. FORCE-TO-SENSE WITCH FUNCTIONALITY

Con-FS#	FORCE_# to SENSE_#
0	Disconnected
1	Connected

Programmable Compensation Network

In order to be stable over a wide range of load conditions, a compensation network is available for each channels output forcing op-amp. The network is shown in Figure 19, and the connections are controlled by the CPU port. The compensation network is not limited to the internal resistor/capacitor network shown, but can be expanded by connecting either an external component or an external network to the CAP_A_# pin.

TABLE 50. COMPENSATION NETWORK VALUES

Component	Value
Cmin	29pF
Con-Cap#<0>	58pF
Con-Cap#<1>	123pF
Con-Cap#<2>	142pF
Con-Res*#<0>	500Ω
Con-Res#<1>	10KΩ
Con-Res#<2>	30KΩ
Con-Res#<3>	90KΩ

The maximum capacitance for which the DPS remains unconditionally stable may be set with the compensation network using both internal and external components. Using the CPU port, the user can connect the compensation network for large capacitance load applications and disconnect it for small load applications. There is a trade-off between stability and transient response performance. The larger the compensation capacitors, the more stable the DPS will be. However, the response and settling times will be slower.

The values of resistor/capacitors components can also be chosen to add a zero to the output transfer function of the main forcing op-amp in order to cancel the dominant output pole created by the load capacitance on the FORCE_# pin and internal resistance of the part. The poles created by several typical bypass capacitors (100nF, 1µF, and 10µF) are used as an example below. After the poles frequencies are calculated, a zero can be introduced based on configuration of the compensation network.

Calculation of Output Poles for Typical Bypass Capacitors

To calculate the output pole the following equation was used:
Pole = 1 / (2*π*R*C)

R = Internal resistance of forcing op-amp (assumed to be 3Ω)

C = Load capacitance at FORCE_# pin

TABLE 51. CALCULATED OUTPUT POLE LOCATIONS

Load Capacitance on FORCE_#	Output Pole (kHz)
100nF	531
1µF	53
10µF	5.3

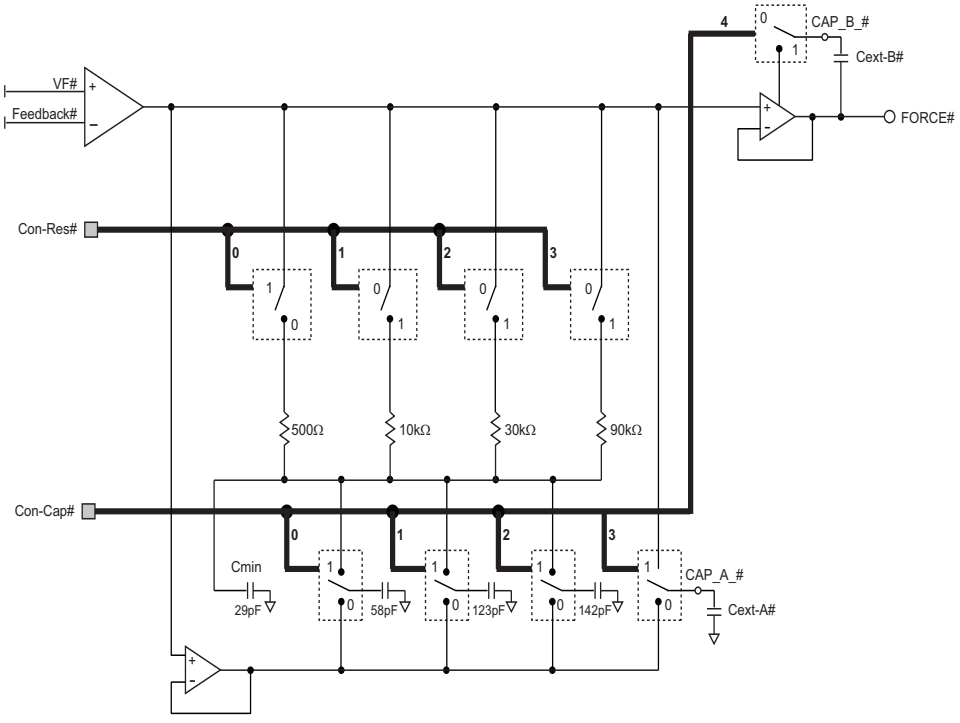


FIGURE 19. PER CHANNEL PROGRAMMABLE COMPENSATION NETWORK

Note: The Con-Res*#<0> bit is active low and therefore to connect this resistor, the bit should be set low. This will ensure that a resistor is connected following a reset.

After calculating the output pole frequency, the user can use the following equation to select the desired compensation network combination to add a zero.

Calculation of Zeros based on Internal Capacitors and Resistors

To calculate zero locations, the following equation was used: Zero = 1 / (2*π*R*C)

R = Total internal compensation resistance chosen using Con-Res#

C = Total internal compensation capacitance chosen using Con-Cap#

Using the example of 100nF in Table 51, an output pole of 531kHz exists. The user would then search for this frequency in Table 52. Based on this frequency, a combination of Con-Cap#<2:0>=0x0 and Con-Res#<3:0> = 0x3 which gives a frequency of 549 kHz, would be chosen. As noted earlier, Table 48 can be expanded with other combinations of components to meet specific needs.

All capacitor connection switches may be opened and closed independently. The addition of a Cext-B# capacitor to the CAP_B_# pin is recommended to improve transient performance in current Range IR0. For stability, CAP_B_# >= Cload/10.

Typical external capacitive values are:

Cext-B# = 100nF

Cext-A# = 4.7nF

However, different capacitor values can be used to trade off stability under a capacitive load vs. settling time.

There is an internal buffer to pre-charge all unconnected compensation capacitors to the Force Voltage output level. This facilitates switching compensation settings with minimal disturbance to the output voltage.

TABLE 52. ZERO LOCATIONS BASED ON INTERNAL CAPACITORS AND RESISTORS (kHz)

Con-Cap#<2>	Con-Cap#<1>	Con-Cap#<0>	Sum of Con-Cap# Capacitors Ccomp(pF)	Con-Res*#<0>=0 Con-Res#<1>=0 Con-Res#<2>=0 Con-Res#<3>=0	Con-Res*#<0>=1 Con-Res#<1>=1 Con-Res#<2>=0 Con-Res#<3>=0	Con-Res*#<0>=1 Con-Res#<1>=0 Con-Res#<2>=1 Con-Res#<3>=0	Con-Res*#<0>=1 Con-Res#<1>=0 Con-Res#<2>=0 Con-Res#<3>=1
0	0	0	29	10982	549	183	61
0	0	1	87	3661	183	61	20
0	1	0	152	1095	105	35	12
0	1	1	210	1517	76	25	8
1	0	0	171	1862	93	31	10
1	0	1	229	1391	70	23	8
1	1	0	294	1083	54	18	6
1	1	1	352	905	45	15	5

NOTE: Ccomp = sum of selected Con-Cap# capacitors. The table above calculates a zero for only one internal resistor selected at a time and using only internal capacitors. Resistors can all be chosen in parallel and external components can be used to add almost endless possibilities to zero locations.

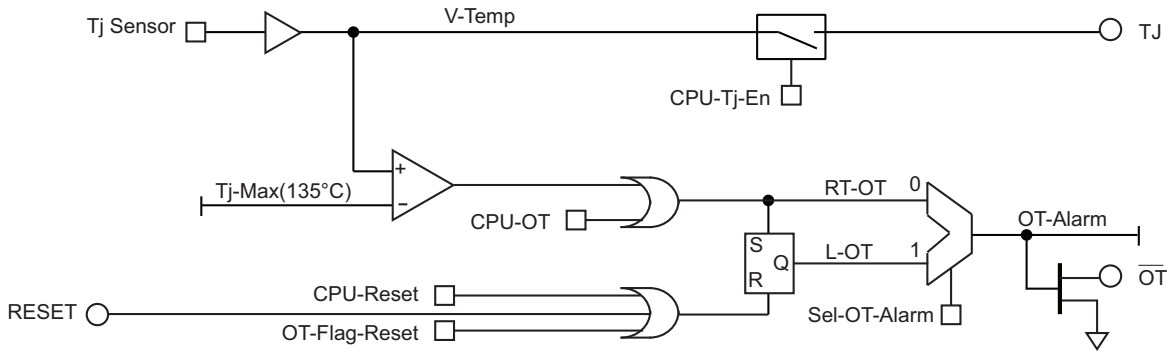


FIGURE 20. OVER-TEMPERATURE ALARM AND THERMAL MONITOR CIRCUITRY

Over-temperature Protection

An on-chip thermal monitor allows the chip to protect itself from an over temperature situation. An on-chip reference establishes the threshold for the over-temperature comparator.

TABLE 53. THERMAL MONITOR FUNCTIONALITY

INPUT CONDITION	OUTPUT CONDITION
V-Temp < Tj-Max (+135°C)	Normal Operation
V-Temp > Tj-Max (+135°C)	OT Fault

Over-temperature Alarm

$\overline{OT}$ is an open drain output that indicates when the junction temperature exceeds +135°C. The CPU port can also directly force the over temperature flag to be active.

The over-temperature alarm can be latched or real time..

TABLE 54. OVER-TEMPERATURE ALARM FUNCTIONALITY

CPU-OT	JUNCTION TEMPERATURE	RT-OT
0	V-Temp < Tj-Max (+135°C)	0
0	V-Temp > Tj-Max (+135°C)	1
1	X	1

TABLE 55. OVER-TEMPERATURE ALARM MODES

Sel-OT-Alarm	OT-Alarm	MODE
0	RT-OT	Real Time
1	L-OT	Latched

Once L-OT is set, it will remain high until cleared by the CPU port or a chip level reset. OT-Flag-Reset and CPU-Reset are write only transactions that generate a one-shot pulse and may not be read back. RT-OT and L-OT may be read back by the CPU port.

TABLE 56. OVER-TEMPERATURE ALARM INDICATOR

OT-Alarm	$\overline{OT}$
0	1 (HiZ)
1	0 (Active - 100Ω to ground)

Temperature Monitor

TJ is a voltage output that tracks the junction temperature.

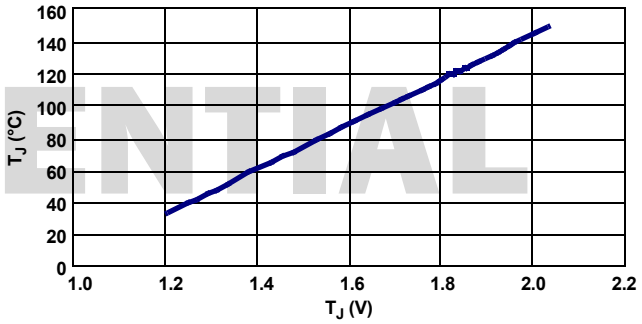


FIGURE 21. THERMAL MONITOR VOLTAGE TO TEMPERATURE MAPPING

TJ has HiZ capability under CPU port control.

TABLE 57. THERMAL MONITOR PIN MODES

CPU-TJ-En	TJ
0	HiZ
1	V-Temp

Overcurrent Alarm

The CPU port controls the current alarm circuitry.

TABLE 58. OVER-CURRENT ALARM FUNCTIONALITY

I-AI-En#	CURRENT ALARMS
0	Alarms Disabled
1	Alarms Enabled

The current alarms can be enabled independently from the current clamps, even though they share a common MI-CI# input and common threshold values.

The current alarm can be latched or be a real time signal.

TABLE 59. OVER-CURRENT ALARM MODES

Sel-I-AI#	I-ALARM#
0	RT-I-CI#
1	L-I-CI#

Once latched, the alarm remains high until cleared by the CPU port or a chip level reset. I-CI-Reset# and CPU-Reset are write only transactions that generate a one-shot pulse and cannot be read back through the CPU port.

Current Alarm Readback

L-OI-Src#, L-OI-Snk#, RT-OI-Src# and RT-OI-Snk# may be read back through the CPU port.

Current Clamps vs Current Alarms

The current clamps are used for a variety of functions.

1. Protect the DPS

The current clamps protect the DPS when it faces a short circuit or an overcurrent situation.

2. Protect the DUT

The current clamps protect the DUT from excessive current flow.

3. FI Mode

The current clamps are used to support FI mode.

Current Alarms are used to identify an overcurrent situation and raise a flag. That flag may be used to place the DPS in HiZ or may be ignored.

There are 3 possible configurations for the current clamps and alarms:

1. Clamps and alarm off
2. Clamps on and alarm off
3. Clamps and alarm on

It is NOT possible to have the alarms active and the clamps off.

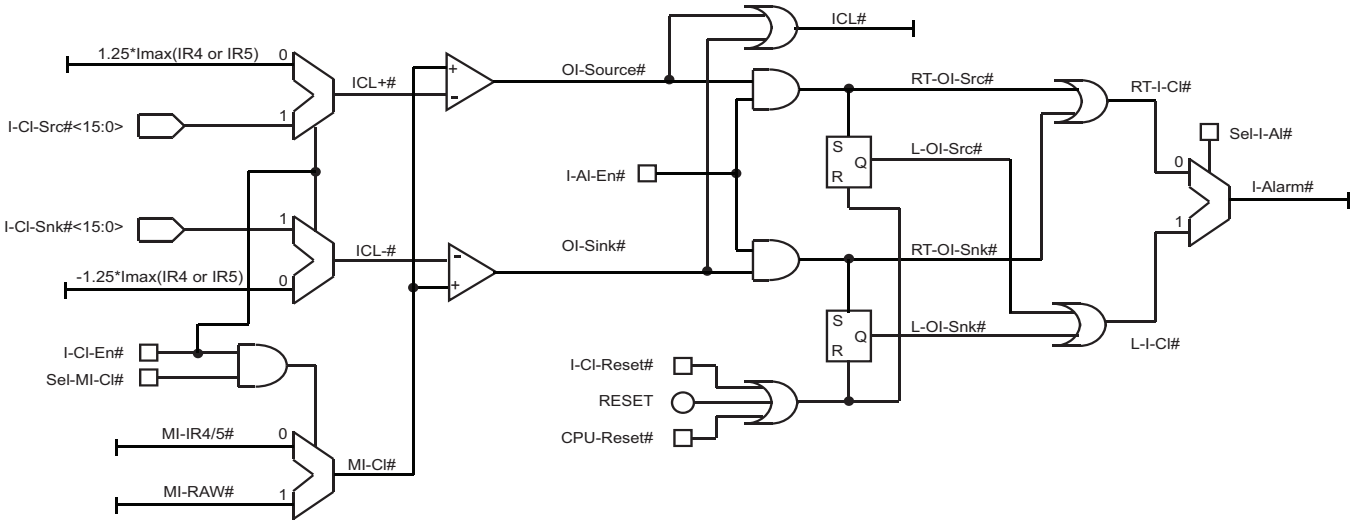


FIGURE 22. OVER-CURRENT ALARM CIRCUITRY

Kelvin Alarm

Each channel has its own independent Kelvin Alarm detector to guarantee that a proper feedback path is connected to the forcing op amp. The CPU selects the voltage difference between FORCE_# and V-FB# signals that define the Kelvin connection.

TABLE 60. KELVIN ALARM THRESHOLDS

Kelvin-Th#<3:0>	Kel-Thresh#±
0000	±175mV
0001	±350mV
•	•
1110	±2.625V
1111	±2.8V
Resolution	175mV

When the difference between FORCE_# and V-FB# exceeds the threshold, a Kelvin fault state is detected.

TABLE 61. KELVIN FAULT STATE INDICATORS

LOOP CONDITION	Kelvin-Fault#
FORCE_# – V-FB# > Kel-Thresh+	1
FORCE_# – V-FB# < Kel-Thresh-	1
Kel-Thresh– < FORCE_# – V-FB# and FORCE_# – V-FB# < Kel-Thresh+	0

A real time Kelvin alarm is signaled when an open loop condition occurs..

Any occurrence of a Kelvin alarm is captured by the latched Kelvin alarm signal. The CPU port selects the source of the channel Kelvin alarm. Kel-Al# and L-Kel-Al# may be read back through the CPU port.

TABLE 62. KELVIN ALARM INDICATOR FUNCTIONALITY

Sel-Kel-Al#	Kel-Al#
0	RT-Kel-Al#
1	L-Kel-Al#

Once a Kelvin alarm has been latched, it remains latched until cleared by the CPU port or a chip level reset. CPU-Reset and Kel-Al-Reset# are write only transactions that generate a one-shot pulse and therefore cannot be read back.

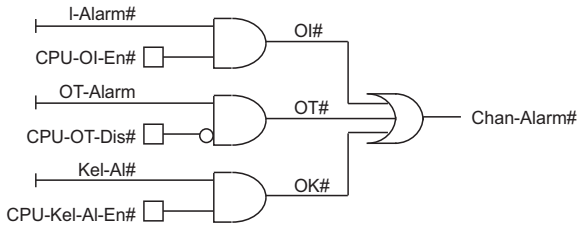


FIGURE 23.

Chip Alarm

The ALARM* pin indicates that an over temperature, over current or Kelvin alarm has occurred.

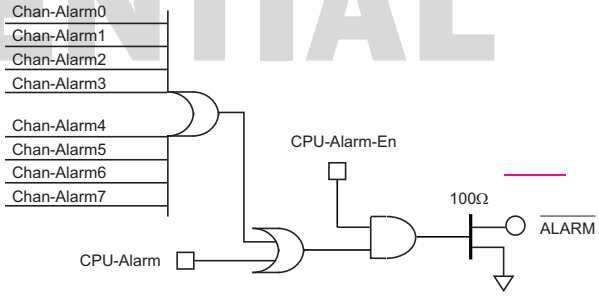


FIGURE 25. CHIP ALARM CIRCUITRY

$\overline{\text{ALARM}}$ may be gated off or forced active by the CPU port.

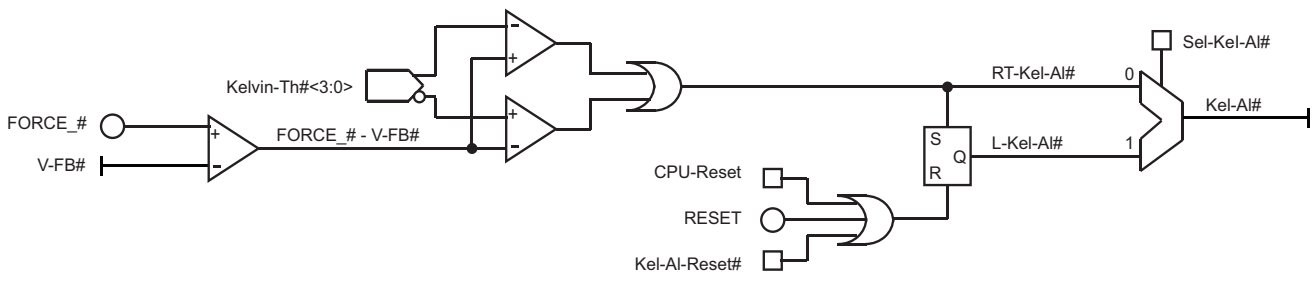


FIGURE 24. OVER-CURRENT AND KELVIN ALARM CIRCUITRY

TABLE 63. CHIP ALARM FUNCTIONALITY

CPU-ALARM	CPU-ALARM-EN	CHAN-ALARM#	$\overline{\text{ALARM}}$
1	1	X	0 (Active)
1	0	X	1 (HiZ)
0	1	0	1 (HiZ)
X	1	1	0 (Active)

$\overline{\text{ALARM}}$ is an open drain active low output that pulls current when active.

Diagnostics

Each channel has access to internal per-channel nodes for diagnostic support.

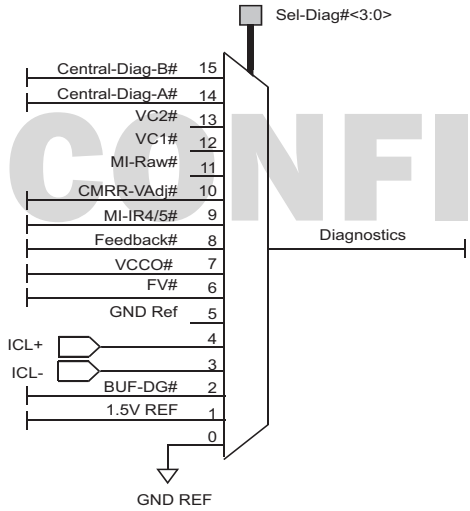


FIGURE 26. DIAGNOSTIC CIRCUITRY

The central diagnostic nodes are routed out to the individual channels with each channel having up to 2 central nodes.

TABLE 64. DIAGNOSTIC MUX CONNECTIONS

CHANNEL	Central-Diag-A	Central-Diag-B
0	Test+	Test-
1	Central-Level+	Central-Level–
2	Vb-Tj	Va-Tj
3	VDD	GND
4	VCC/2	VEE/2
5	VDD	GND
6	GND	Tj
7	DAC_P	DAC_N

VC1# and VC2# are per-channel bias voltages that can be selected as inputs to the per-channel diagnostics MUX using the Sel-Diag#<3:0> bits. These voltages vary proportionally with temperature and can be used as a method to calibrate for various temperature related accuracy errors/temperature coefficients.

Below is an example showing the process for calibrating the MI (Measure Current) Tempco:

1. Calculate Offset TempCo: Measure current with no load (using the MONITOR or MI_MONITOR path) and the difference between VC2 and VC1 on a particular channel with the ISL55180 in thermal equilibrium. Next, load an ADJACENT channel with a current load which will cause the temperature of the channel being calibrated to change. Wait for thermal equilibrium and again measure the current with no load, VC2, and VC1. The offset TempCo in terms of delta VC1–VC2 can now be calculated and can be use dto correct the MI offset change due to local channel temperature change.
2. Calculate Gain Tempco: Two different load currents (calibration points) are needed for the channel being calibrated. The loading on the ADJACENT channel can be changed to give measurements at two cal points with the same VC2–VC1 value for both. Then change the ADJACENT channel loading to product a different VC2–VC1 voltage and repeat the measurements at the two cal points. This will permit calculating a gain Tempco.

NOTE: The actual temperature does not need to be known for this calibration. All that is really needed is to know that MI changes for a given change in VC2–VC1.

DAC_P and DAC_N are per-chip voltages used for the LSB auto-calibration.

MI_Raw# is a voltage that tracks current in the selected current range and is used as an input to the comparator for the current clamp and current alarm features.

Temperature Sensing

The ISL55180 has its own independent temperature sense capability. There are two internal voltages:

1. Va-Tj
2. Vb-Tj

Which, when measured, may be used to calculate the junction temperature as expressed in Equation 2

.

$$Tj[°C] = \{(Va - Tj) - (Vb - Tj) \bullet 1637\} - 221$$

Required Off-Chip Components

A precision voltage reference level and external resistor is required per chip. In addition, each channel may require external capacitors in order to support CPU selectable stability under different capacitive loads.

There may be a need for decoupling capacitors on the power supply pins. The need for decoupling capacitors is dependent upon the particular application, and is therefore system dependent.

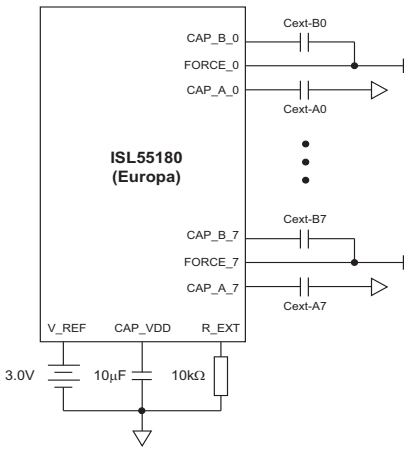


FIGURE 27. EXTERNAL COMPONENT CONNECTIONS

V_REF

V_REF is an analog input voltage that is used to program the on-chip DC levels. V_REF should be held at +3.0V with respect to GND. There is one V_REF pin shared by all channels on the same chip.

V_REF SENSITIVITY

The previous equations that predict the DAC output assume that V_REF = 3.000V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio before being multiplied by the gain.

Offset adjust has ample range to correct for deviations in V_REF. As long as V_REF is held stable after calibration, any deviation in V_REF from 3.0V will not affect DC accuracy.

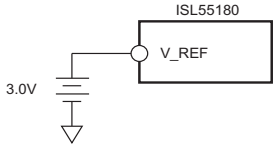


FIGURE 28. EXTERNAL VOLTAGE REFERENCE

Device Under Test Ground

The DUT-GND_# pin is a per channel ground reference input that provides a means of tracking the ground level at the DUT and making additional voltage offsets inside the chip so that the voltage levels generated on-chip are with respect to the ground level at the DUT.

BUF_DG# is the internal buffered version of DUT_GND#.

DUT_GND_# is NOT added into the DC level when forcing or measuring a current. The inputs to the DUT_GND_# pins should be stable, filtered, and reflect the actual ground level at the DUT.

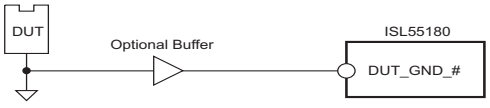


FIGURE 29. DUT GROUND SENSE CONNECTION

VOH_SDIO

VOH_SDIO is the positive power supply of the output stage of the SDIO pin and used to set the voltage level for a logical 1 at the output such that it is consistent with voltage compliance at the destination.

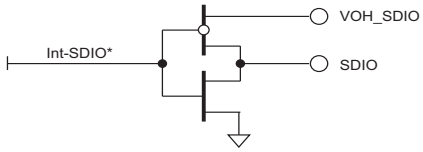


FIGURE 30. SERIAL DATA LOGIC LEVEL SETTING

R_EXT

R_EXT is a precision external resistor used to control various internal bias currents.

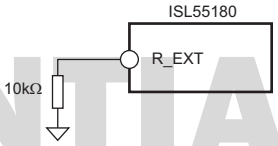


FIGURE 31. EXTERNAL REFERENCE RESISTOR CONNECTION

CAP_VDD

C_EXT is used to filter VDD on-chip.

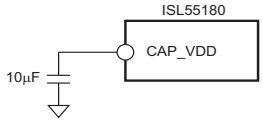


FIGURE 32. EXTERNAL CAPACITOR CONNECTION

Chip Reset

RESET is an external hardware reset signal that places all internal registers into a low state. Reset must be executed after a power-up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power-up sequence.** RESET is active high.

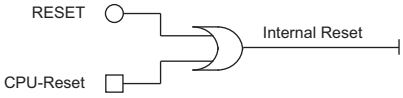


FIGURE 33. CHIP RESET

In addition, the CPU port can execute a reset (as a write only transaction). If the CPU-Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one shot pulse that performs the same function as an external RESET.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC ≥ VDD, VOH_SDIO, VCCO_#
2. VEE ≤ GND
3. VDD ≥ VOH_SDIO, GND
4. VCCO_# ≥ GND

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

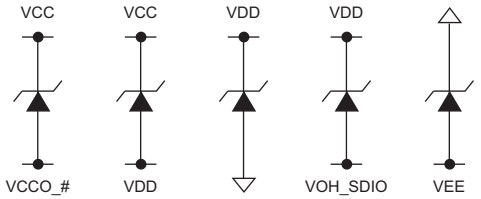


FIGURE 34. EXTERNAL SCHOTTKY DIODE SUPPLY CLAMPS

Power Supply/Analog Voltage Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCC
3. VCCO_#
4. VDD
5. VOH_SDIO
6. V_REF

DC Levels

Each channel requires several DC levels in order to function properly. The levels are all generated on-chip with a 16-bit DAC that is programmed through the CPU port.

Voltage Level Programming

The CPU port may select 1 of 2 voltage range options.

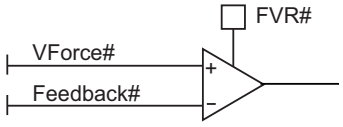


FIGURE 35. VOLTAGE LEVEL PROGRAMMING

The voltage range that is achievable is restricted by the power supply levels and headroom limitations. If a level is programmed beyond the power supply rails, saturation will occur and the actual DC level will not match the desired programmed level.

TABLE 65. VOLTAGE RANGE OPTIONS

MODE	FVR#	FULL SCALE (FS) (V)	VOLTAGE SWING (V)	RESOLUTION (LSB) (µV)	VMID (V)
FV	0	8	-2 to +6	122	+2
FV	1	16	-2 to +14	244	+6

Level Programming

When generating a voltage, use:

V_{OUT} = (Value – V_{MID}) • Gain

+ V_{MID}

+ Offset

+ DUT_GND

Value is described by:

Value = {(DAC Code)/(2^N–1)} • FS + V_{MIN}

where:

V_{MIN} = – 2V

N = 16,

2^N – 1 = 65,535

Current Clamp Programming

When programming current clamp values, use:

IOUT = (I_{DAC} – I_{MID}) • Gain + I_{MID} + Offset

I_{MID} = (I_{MAX} * 1.5)/2

I_{DAC} = ((DAC Code) / (2^N–1)) • I_{MAX} • 1.5

I-CI+ = positive current flow out of the part

I-CI– = negative current flow into the part

Imax = Dependent on current range selected for use in current clamp comparator

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at their true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per pin errors. The range of possible offset voltage correction is a % of the full-scale voltage range of each particular voltage group.

TABLE 66. OFFSET AND GAIN ADJUSTMENT RANGE

CODE	VALUE
OFFSET	
0000H	-5.4% of FS
7FFFH	0
FFFFH	+5.4% of FS
GAIN	
0000H	0.75 (-25%)
7FFFH	1.0
FFFFH	1.25 (+25%)

DC Calibration and Level Test Procedure

The part is designed and tested to meet its DC accuracy specifications after a calibration is performed. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. The calibration and test points are listed in the DC Electrical Specifications Section.

The test points are broken into two categories:

1. inner test
2. outer test

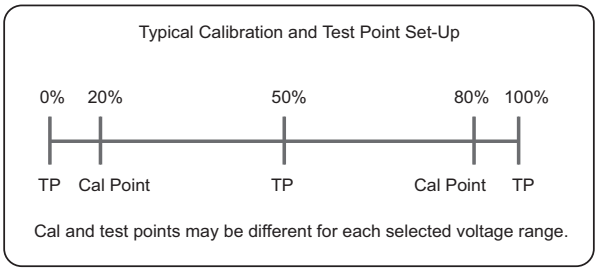


FIGURE 36.

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

Every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration techniques, which are located in Appendix A.

CALIBRATION PROCEDURE

1. Calibrate Monitor
2. Perform DAC LSB Calibration
3. Calibrate DAC Cal Bits
4. Calibrate Offset DAC
5. Calibrate Gain DAC
6. Calibrate Per Channel Central Offset/Gain
7. Calibrate the DC Level (FV, ICL)
8. Calibrate CME
9. Calibrate MI

LEVEL CALIBRATION

Initialize

- Select desired voltage range (VR0, VR1) (8V, 16V)
- Set Gain = 1.0; Offset = 0.0V

Measure

- Set Level 1 = Cal Point 1. Measure Output1' (low)
- Set Level 2 = Cal Point 2. Measure Output2' (high)

Calculate

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) - Gain' o (Level2 - Vmid)

Finish

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

DAC Calibration

A 16-bit DAC is used to generate all of the required DC levels. To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs as well as an LSB auto-calibration procedure. The default condition of these adjustment bits is the zero correction state.

DAC LSB (LEAST SIGNIFICANT BIT) AUTO-CALIBRATION

The CPU port can initiate an auto-calibration sequence to adjust the DAC LSB. Setting the register bit high initiates the sequence. When the bit is subsequently read back as a 0, the calibration is complete. Once the calibration sequence has been started, wait at least 50ms before polling,

LSB calibration values are stored in the DAC-N/DAC-P registers (central resource address 6).

TABLE 67. LSB AUTO CALIBRAITON

LSB-AUTO-CAL	LSB CAL STATUS
1	LSB calibration in progress
0	LSB calibration complete

DAC MSB CALIBRATION

To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level after the LSB calibration but prior to the gain and offset correction.

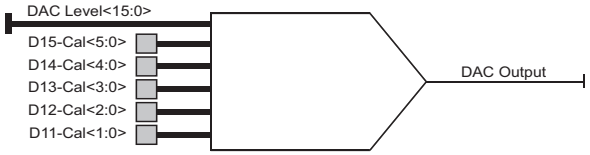


FIGURE 37.

TABLE 68. CAL RANGE VS VOLTAGE RANGE VS DAC BITS

	8V	16V
D15	±7.564mV	±15.128mV
D14	±3.66mV	±7.32mV
D13	±1.708mV	±3.416mV
D12	±732µV	±1.464mV
D11	±244µV	±488µV

TABLE 69. D15 CALIBRATION

D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	D15 Adjustment
0	1	1	1	1	1	+62 LSB
			•			•
0	0	0	0	0	1	+2 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	-2 LSB
			•			•
1	1	1	1	1	1	-62 LSB

TABLE 70. D14 CALIBRATION

D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	D14 Adjustment
0	1	1	1	1	+30 LSB
		•			•
0	0	0	0	1	+2 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	-2 LSB
		•			•
1	1	1	1	1	-30 LSB

TABLE 71. D13 CALIBRATION

D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>	D13 Adjustment
0	1	1	1	+14 LSB
	•			•
0	0	0	1	+2 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	-2 LSB
	•			•
1	1	1	1	-14 LSB

TABLE 72. D12 CALIBRATION

D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	D12 Adjustment
0	1	1	+6 LSB
0	1	0	+4 LSB
0	0	1	+2 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	-2 LSB
1	1	0	-4 LSB
1	1	1	-6 LSB

TABLE 73. D11 CALIBRATION

D11-Cal<1>	D11-Cal<0>	D11 Adjustment
0	1	+2 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	-2 LSB

CPU Port

All on-chip DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip.

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back.

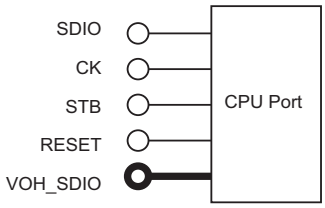


FIGURE 38. CPU PORT

CK is the CPU port clock signal. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction and remains high for the duration of the transaction. STB must go low before another transaction may begin.

Clock Requirements

It is recommended that the CK be running at all times as it refreshes the DC levels throughout the chip.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

WE is read back as a don't care (X) value.

Read vs Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type. Unused data bits are read back as a don't care (X) state.

TABLE 74. CPU TRANSACTION TYPES

1ST SDIO BIT	CPU TRANSACTION TYPE
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

"Any Channel" Write

The CPU port can write to any or all selected channels with one write transaction by setting the selected channel bit in the address. Setting the channel bit hit high results in that channel being written to. Setting the channel bit low means the channel will not be written to.

TABLE 75. MULTI-CHANNEL ADDRESSING

A13	A12	A11	A10	A9	A8	A7	A6
Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0

Channel Read Back

When performing a read transaction, exactly one channel must be selected and programmed to a 1, with the remaining channel bits all programmed to 0.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 76. CHIP ID REGISTER

D15:D4	D3:D0
Product-ID<11:0> F16 Hex (3862)	Die-Rev<3:0>

Address Space

Address Description

Information is stored on chip in two ways:

1. DC Level Memory
2. Registers

Each storage mechanism is then broken into two categories:

1. Per channel resources
2. Central resources.

The address space is partitioned into several different segments to clearly mark the resource type and function.

DAC Sample and Hold (S/H) State Machine

The internal DAC's used in the ISL55180 are S/H DACs. To update a single DAC level, it takes 387 clocks cycles. The clock used for this operation is the CPU interface clock. The first 256 clocks are used to select the desired level and let the DAC level settle. The next 128 clocks are needed to refresh the S/H. The 3 remaining clock cycles are used to control the state machine. To calculate the time to refresh one DAC level, multiply the CPU clock time by the number of clocks needed to update one level. If using a 25Mhz clock the time needed is:

$$40ns \cdot 387 \text{ cycles} = 15.48\mu s.$$

There are 32 total internal levels to the S/H DAC, therefore to update the entire DAC the time would be:

$$32 \cdot 40ns \cdot 387 \text{ cycles} = 495.36\mu s.$$

The order the state machine uses to refresh the DAC matches the RAM address mapping: ForceA0, ForceA1, ..., ForceA7, ForceB0, ForceB1, etc. This order allows several channels to update whenever a multi-channel write is performed for the same level.

Whenever writing to a specific level, the state machine will complete the current level already being processed and then jump to the level just written. After the selected level is written, the state machine then proceeds in the normal order from this level forward (i.e. it doesn't jump back). Therefore you should assume that, at worst case, it takes 774 clocks to update a single level after being written, 387 to complete the current level, plus 387 to update the desired level. One caveat to this is with a multi-channel write. There will still be, at worst case, 774 clocks to update the first (lower numbered) channel of the multi-channel write. The other channels in the multi-channel write will be updated in sequence after the first one. That means that if channel 0 and channel 7 are written as part of a multi-channel write, then channel 0 could take 774 clocks to update (worst case) and then channel 7 will update 7x387 clocks later.

Care should be taken when continuously writing to a particular level such that other levels are not starved of being refreshed by the CPU clock. If this happens, levels can droop out of specification.

TABLE 77. ISL55180 REGISTER MAP

PER CHANNEL RESOURCE REGISTER STORAGE																
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS								PER CHANNEL RESOURCE ADDRESS						DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	0	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0	A5	A4	A3	A2	A1	A0	Register Data

CENTRAL RESOURCE REGISTER STORAGE																
REGISTER BIT	CENTRAL BIT	UNUSED BITS							CENTRAL RESOURCE ADDRESS							DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Register Data

CHANNEL # DC LEVEL STORAGE																
REGISTER BIT	CENTRAL BIT	CHANNEL DESTINATION SELECTION								DAC FUNCTION		DC LEVEL ADDRESS				DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0	0	0	0	0	0	0	ForceA#<15:0> Level
0	0									0	0	0	0	0	1	ForceB#<15:0> Level
0	0									0	0	0	0	1	0	I-Cl-Src#<15:0> Level
0	0									0	0	0	0	1	1	I-Cl-Snk#<15:0> Level
0	0									0	0	4 - 15				Not Used

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0	0	1	0	0	0	0	ForceA#<15:0> Offset
0	0									0	1	0	0	0	1	ForceB#<15:0> Offset
0	0									0	1	0	0	1	0	I-Cl-Src#<15:0> Offset
0	0									0	1	0	0	1	1	I-Cl-Snk#<15:0> Offset
0	0									0	1	4 - 15				Not Used

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0	1	0	0	0	0	0	ForceA#<15:0> Gain
0	0									1	0	0	0	0	1	ForceB#<15:0> Gain
0	0									1	0	0	0	1	0	I-Cl-Src#<15:0> Gain
0	0									1	0	0	0	1	1	I-Cl-Snk#<15:0> Gain
0	0									1	0	4 - 15				Not Used

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0	1	1	0 - 15				Not Used

NOTE: Do not write to or read from any of the unused locations.

Protocol Timing Diagram

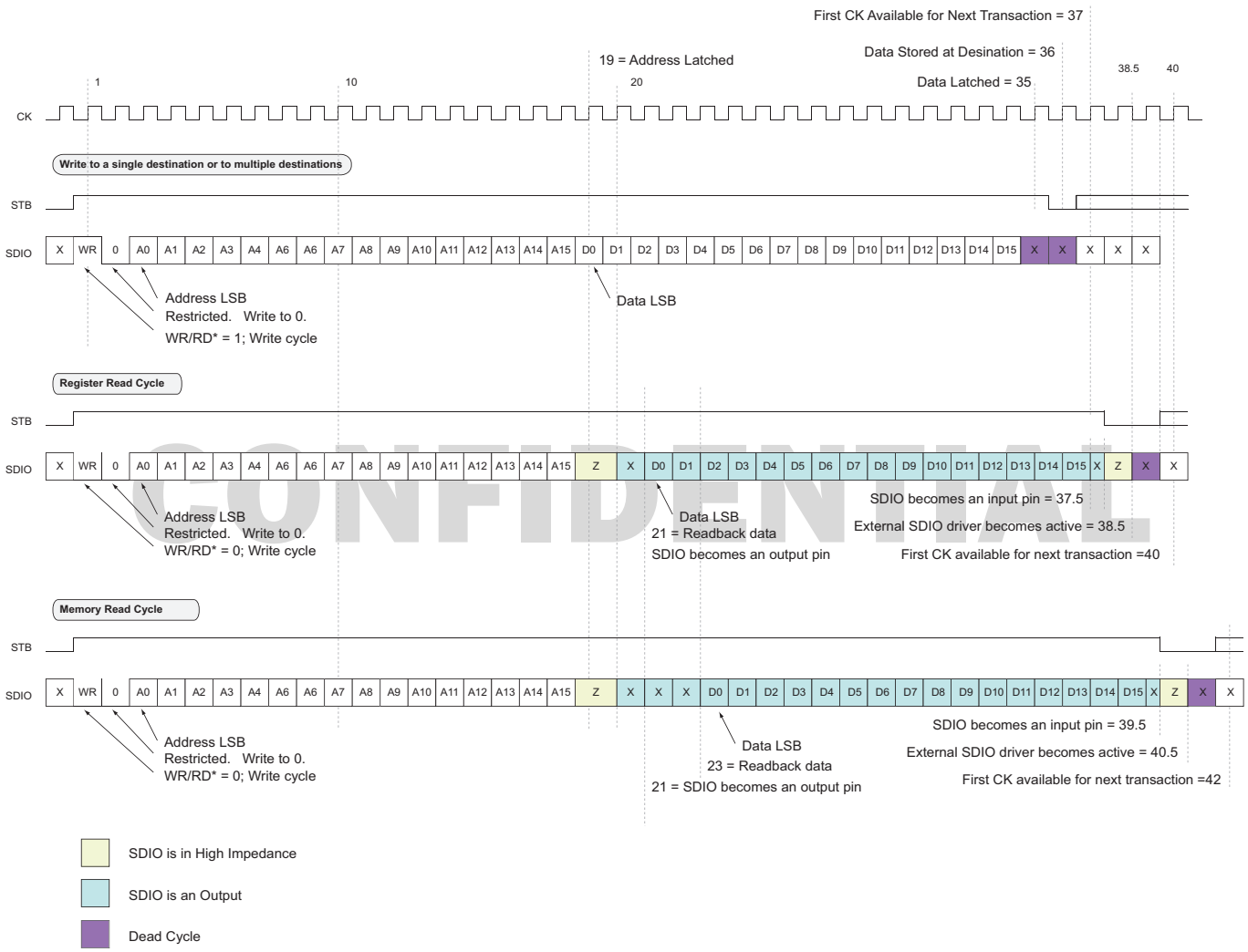


FIGURE 39. PROTOCOL TIMING DIAGRAM

Per Pin Registers

CHANNEL # CONTROL REGISTERS (0 ≤ # ≤ 7)																			
A15	A14	A<13:6>	A<5:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	#	0		WE	Sel-RT-D#	CPU-D#<1>	CPU-D#<0>	WE	FVR#	WE	FI/FV*#	WE	Sel-V-FB#<1>	Sel-V-FB#<0>	WE	Sel-VForce#	WE	Tight-Loop*#	Source and Feedback Selection
1	0	#	1	WE	Con-Res#<3>	Con-Res#<2>	Con-Res#<1>	Con-Res*#<0>	Con-Cap#<4>	Con-Cap#<3>	Con-Cap#<2>	Con-Cap#<1>	Con-Cap#<0>	WE	FV-Mode#	WE	Sel-DPS-En#	Sel-RT-En#	CPU-En#	DPS Control/Miscellaneous
1	0	#	2		WE	Kel-Al-Reset#	I-Cl-Reset#	WE	Sel-Kel-Al#	WE	CPU-OI-En#	CPU-Kel-Al-En#	CPU-OT-Dis#	WE	Sel-MI4#	Sel-MI-Cl#	I-Al-En#	I-Cl-En#	Sel-I-Al#	Clamp and Alarm Control
1	0	#	3					Sel-FV<1>	Sel-FV<0>	DPS-En#	Chan-	L-OI-Src#	RT-OI-Src#	OI-Source#	L-OI-Snk#	RT-OI-Snk#	OI-Snk#	L-Kel-Al#	RT-Kel-Al#	Status Read Back
1	0	#	4	WE	Kelvin<#3>	Kelvin#<2>	Kelvin#<1>	Kelvin#<0>	WE	Con-EF-ES#	Con-FS#	Con-ES-F#	Con-ES-S#	Con-EF-F#	WE	Sel-Diag#<3>	Sel-Diag#<2>	Sel-Diag#<1>	Sel-Diag#<0>	Diagnostics and Calibration
1	0	#	5	WE	Bbias#	Sel-G#-Out	WE	IR#<5>	IR#<4>	IR#<3>	IR#<2>	IR#<1>	IR#<0>	WE	Sel-MU-Neg#<1>	Sel-MU-Neg#<0>	WE	Sel-MU-Pos#<1>	Sel-MU-Pos#<0>	Measurement Unit Source Selection
1	0	#	6								WE	OS#<7>	OS#<6>	OS#<5>	OS#<4>	OS#<3>	OS#<2>	OS#<1>	OS#<0>	Offset Adjust
1	0	#	7								WE	Av#<7>	Av#<6>	Av#<5>	Av#<4>	Av#<3>	Av#<2>	Av#<1>	Av#<0>	Gain Adjust

Read Only

Write Only

Per Pin Registers - continued

CHANNEL # CONTROL REGISTERS (0 ≤ # ≤ 7)																				
A15	A14	A<13:6>	A<5:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	#	8								WE	CME-Adj0#<7>	CME-Adj0#<6>	CME-Adj0#<5>	CME-Adj0#<4>	CME-Adj0#<3>	CME-Adj0#<2>	CME-Adj0#<1>	CME-Adj0#<0>	CME Adjust IR0
1	0	#	9								WE	CME-Adj1#<7>	CME-Adj1#<6>	CME-Adj1#<5>	CME-Adj1#<4>	CME-Adj1#<3>	CME-Adj1#<2>	CME-Adj1#<1>	CME-Adj1#<0>	CME Adjust IR1
1	0	#	10								WE	CME-Adj2#<7>	CME-Adj2#<6>	CME-Adj2#<5>	CME-Adj2#<4>	CME-Adj2#<3>	CME-Adj2#<2>	CME-Adj2#<1>	CME-Adj2#<0>	CME Adjust IR2
1	0	#	11								WE	CME-LAdj3#<7>	CME-LAdj3#<6>	CME-LAdj3#<5>	CME-LAdj3#<4>	CME-LAdj3#<3>	CME-LAdj3#<2>	CME-LAdj3#<1>	CME-LAdj3#<0>	CME Adjust IR3 Low Voltage
1	0	#	12								WE	CME-HAdj3#<7>	CME-HAdj3#<6>	CME-HAdj3#<5>	CME-HAdj3#<4>	CME-HAdj3#<3>	CME-HAdj3#<2>	CME-HAdj3#<1>	CME-HAdj3#<0>	CME Adjust IR3 High Voltage
1	0	#	13								WE	CME-HAdj4#<7>	CME-HAdj4#<6>	CME-HAdj4#<5>	CME-HAdj4#<4>	CME-HAdj4#<3>	CME-HAdj4#<2>	CME-HAdj4#<1>	CME-HAdj4#<0>	CME Adjust IR4 Low Voltage
1	0	#	14								WE	CME-Adj4#<7>	CME-Adj4#<6>	CME-Adj4#<5>	CME-Adj4#<4>	CME-Adj4#<3>	CME-Adj4#<2>	CME-Adj4#<1>	CME-Adj4#<0>	CME Adjust IR4 High Voltage
1	0	#	15								WE	CME-Adj5#<7>	CME-Adj5#<6>	CME-Adj5#<5>	CME-Adj5#<4>	CME-Adj5#<3>	CME-Adj5#<2>	CME-Adj5#<1>	CME-Adj5#<0>	CME Adjust IR5
1	0	#	16								WE	ESP#<7>	ESP#<6>	ESP#<5>	ESP#<4>	ESP#<3>	ESP#<2>	ESP#<1>	ESP#<0>	ESP Resistance Compensation Value
1	0	#	17-63																	Not Used

Central Resource Registers

CENTRAL RESOURCE CONTROL REGISTERS																				
A15	A14	A<13:7>	A<6:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPU-Reset (Blue = Write Only)
1	1	0	1			WE	Reserved	Reserved	Reserved	WE	MUR<1>	MUR<0>	WE	Sel-Mon-OE	CPU-Mon-OE	WE	Sel-MU<2>	Sel-MU<1>	Sel-MU<0>	Measurement Unit Control/Ganging
1	1	0	2			WE	Sel-RT-Central-D	WE	CPU-Cent-D<3>	CPU-Cent-D<2>	CPU-Cent-D<1>	CPU-Cent-D<0>	WE	Sel-MI-Mon-OE	CPU-MI-Mon-OE	WE	Sel-Cent-MI<2>	Sel-Cent-MI<1>	Sel-Cent-MI<0>	Measure Current Monitor/Central Level Select
1	1	0	3	L-OT	RT-OT	WE	OT-Flag-Reset			WE	CPU-Alarm	WE	CPU-Alarm-En	WE	CPU-OT	WE	CPU- Tj-En	WE	Sel-OT-Alarm	Alarm Control
1	1	0	4				WE	D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	WE	D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	**DESCRIPTION**
1	1	0	5			WE	LSB-Auto-Cal	WE	D11-Cal<1>	D11-Cal<0>	WE	D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	WE	D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>	Mid DAC Bit Calibration
1	1	0	6		DAC-N<6>	DAC-N<5>	DAC-N<4>	DAC-N<3>	DAC-N<2>	DAC-N<1>	DAC-N<0>		DAC-P<6>	DAC-P<5>	DAC-P<4>	DAC-P<3>	DAC-P<2>	DAC-P<1>	DAC-P<0>	DAC-N/DAC-P
1	1	0	7 – 126																	Not Used
1	1	0	127	Product-ID<11>	Product-ID<10>	Product-ID<9>	Product-ID<8>	Product-ID<7>	Product-ID<6>	Product-ID<5>	Product-ID<4>	Product-ID<3>	Product-ID<2>	Product-ID<1>	Product-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>	Die ID (Red = Read only)

Read Only

Write Only

After being set high, will remain high until autocal sequence is complete.

Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows Equation 1:

$$T_J = P_D \bullet \theta_{JA} + T_A \quad \text{(EQ. 1)}$$

where:

T_J = Junction Temperature

P_D = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_A = Ambient Temerature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ_{JC}) plus the resistance from the case to ambient (θ_{CA})

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θ_{JA}. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \text{(EQ. 2)}$$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

θ_{JC} Calculation

$$\theta_{JC} = \theta(\text{silicon}) + \theta(\text{dieattach}) + \theta(\text{paddle}) \quad \text{(EQ. 3)}$$

$$\theta_{JC} = 0.072°C/W + 0.61°C/W + 0.006°C/W$$

$$\theta_{JC} = 0.688°C/W$$

The calculation is based upon ideal assumptions and it should be treated as a best-case value.

The thermal resistance of any material is defined by Equation 4:

$$\theta = (\text{Intrinsic material resistivity}) \bullet \text{Thickness}/\text{Area}$$

or

$$\theta = \text{Thickness}/(\text{Intrinsic material conductivity} \bullet \text{Area}) \quad \text{(EQ. 4)}$$

Intrinsic Thermal Conductivity

Die Attach Thermal Conductivity = 1.4W /M °K

Silicon Thermal Conductivity = 141.2W/M °K

Paddle Thermal Conductivity = 263W/M °K

Plastic Thermal Conductivity = 0.88W/M °K

(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θ_{JC} through the paddle. The assumption is that all heat flow will go through the paddle and none through the surrounding plastic).

Manufacturing Information

Moisture Sensitivity

The part is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre-Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ±5°C for a duration 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

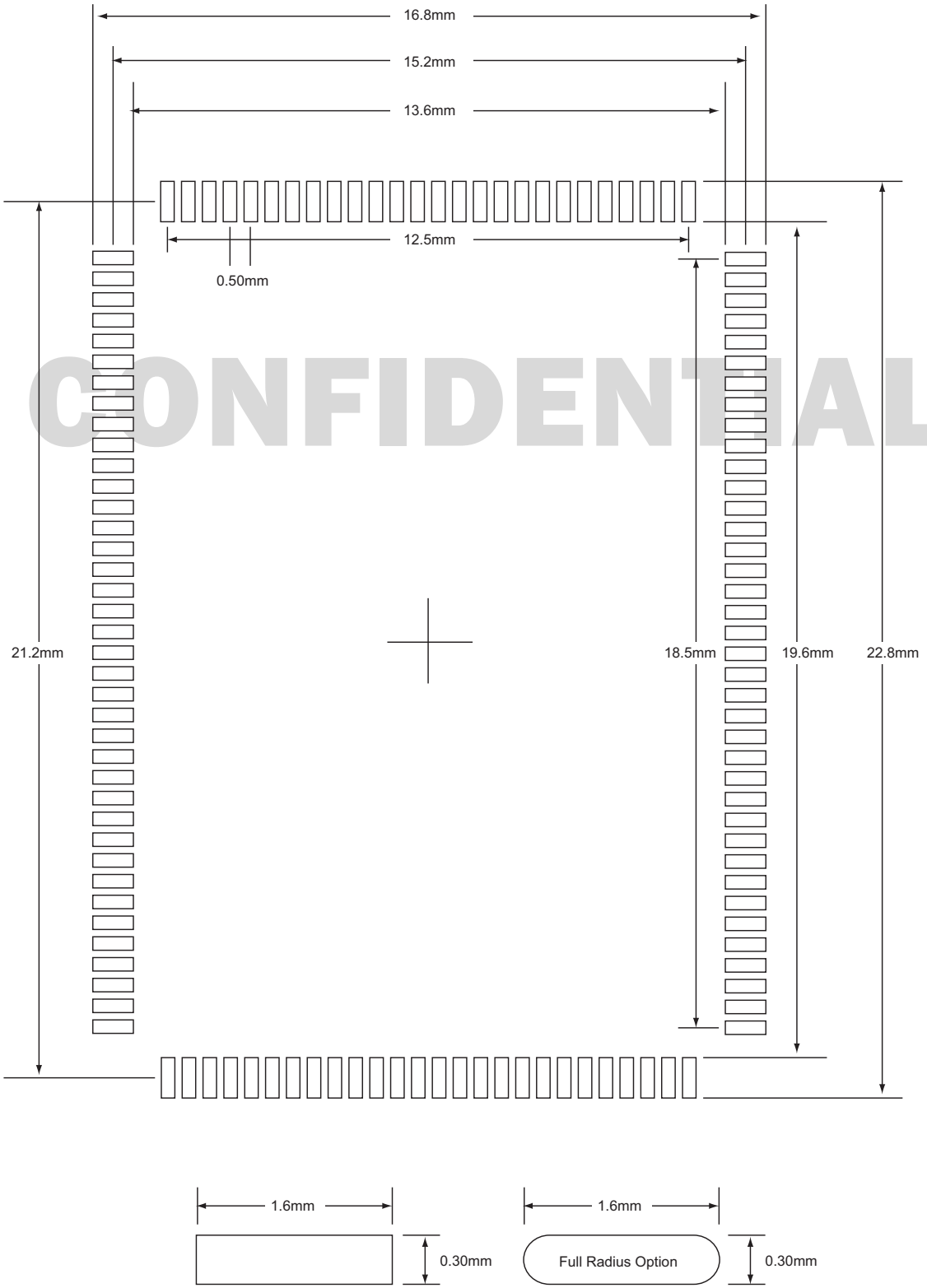
PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

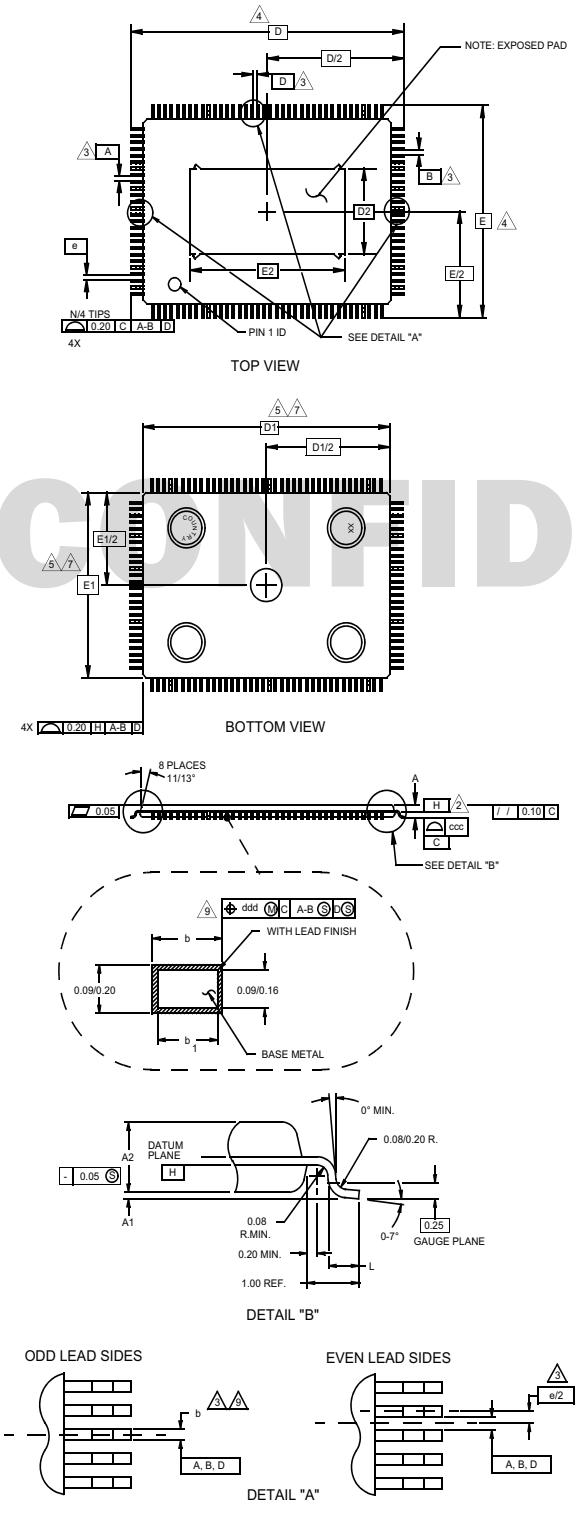
- Chip Floor Life ≤168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Recommended PCB Footprint



Package Outline Drawing



Q128.14x20A

128 Lead Thin Quad Flatpack with Top Exposed Pad

SYMBOL	MILLIMETERS BHB MIN	MILLIMETERS BHB NOM	MILLIMETERS BHB MAX	NOTES
A	-	-	1.60	
A1	0.05	-	0.15	13
A2	1.35	1.40	1.45	
D		22 BSC		4
D1		20 BSC		7, 8
D2		(12.81-0.76) BSC		14
E		16 BSC		4
E1		14 BSC		7, 8
E2		(8.38-0.76) BSC		14
L	0.45	0.60	0.75	
N		128		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

Rev. 0 3/09

NOTES:

1. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at center lines between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm per side on D1 and E1 dimensions.
6. “N” is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. Package top dimensions are smaller than package bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located at the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 Registration MS-026, variations BHA & BHB.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimensions D2 and E2 represent the size of the exposed pad. The actual dimensions may be reduced up to 0.76mm due to mold flash.

Revision History

DATE	CHANGE
August 28, 2022	• Page 10: Updated Recommended Operating Conditions for GANG#_IN and GANG#_OUT pins to (VCC-1.5V) and (VEE+1.5V) • Page 13: Spec #10800. Removed 0V Test Point. Updated Test Points to: VCC - 1.5V and VEE + 1.5V • Page 13: Spec #10800. Removed 0V Test Point. Updated Test Points to: VCC - 1.5V and VEE + 1.5V • Page 28: Update Figure to change I-AI-Reset to I-CI-Reset# • Appendix section 10.4.1.2 CME Calibration Procedure section. Vload equation updated.
June 2, 2017	• Page 16: Update all Typ values for MI Temperature Coefficient • Page 25: Update diagram • Page 35: Figure 8 - change 1.25 * Imax to 2*Imax and -1.25*Imax to -2*Imax • Page 36: Table 30 - add note (**) • Page 47: Figure 22 updated • Page 48: Figure 24 updated • Page 49: Table 63 updated
Sept 1, 2015	• Page 59: Second page of Per Pin Registers Table was inadvertently omitted from last revision and is provided in this revision.
April 1, 2015	• Updated from Intersil to Elevate format. • Page 11: Power Supply Current Table updated • Page 16: Tables 1 and 2 updated. • Page 18: Add #10 to end of each paragraph. • Page 19: Note 1 - change from VCC = +13V, VCCO_# = +4V, VEE = -3V, VCC = +3.3V to VCC = +12V, VCCO_# = +6V, VEE = -4V, VDD = +3.3V. • Page 20: Output Impedance and Leakage section of table updated. • Page 33: Table 20 - remove IR3 from second line; remove IR3 from following paragraph. • Pae 82: Table 4 - remove Current Range IR3 from table
Nov 21, 2014	• Page 11: Power Supply Current Table - Spec #11230, change units from A to mA, change Pd from 8500 to 8.5. • Page 18: Update entire Current Clamps section. • Page 21: ESP Table - Change Test Conditions from FV Mode = 0 to Sel-MI4# = 0; FV Mode = 1 to Sel-MI4# = 1. - Spec #14842: change min/max values to 0.115/1.135 • Page 26: Central Resource vs. Channel Mode Figure: Add mux to Central-D<3:0>. • Page 31: Table 10 - Change Central_D<3:0> to CENTRAL_D<3:0> • Page 32: Table 12 - Change -126mV to -158.74mV; -63mV to -79.37mV, +126mV to +158.74mV, +63mV to +79.37mV • Page 33: Table 16 - Change IR0, IR1, IR2, IR4, IR5 to IR0, IR1, IR2, IR3, IR4, IR5 - Last paragraph - change ...performed in IR4 and IR5 to performed in IR3, IR4 and IR5 • Page 42: Monitor Reference Section - last para, change to ... MONITOR or MI_MONITOR is active • Page 79: Add Current Clamp Calibration Section

DATE	CHANGE
Sept 24, 2014	• Page 16: Tables 1 & 2: Add separate values for IR4 • Page 19: Spec #14832, Change min/max values to 0.720/0.780 - Spec #14842: change min/max values to 0.115/1.135 • Page 67: Figures 3 & 4 - Add calibration points • Page 69: Sections 6.1 through 6.4 - Add Section references • Page 82: Update first paragraph

DATE	CHANGE
August 12, 2014	• Page 1: Features - Power Management - remove “patent pending” • Page 11: Power Supply Current Table: Spec #11410 - Max = 90mA. • Page 12: Digital Outputs Table: Spec #13360 - changeVOL (Sinking 4mA) to VOL (Sinking 2mA) • Page 19: Monitor Table: - Spec #14830, 14832 - Change Units from mV to V - Spec #14831 - Change min/max from 0.975/1.025mV to 0.95/1.05V - Spec #14840 - Change min/max from 0.49/0.51 to 0.47/0.53 - Spec #14841 - Change min/max from 0.245/0.255 to 0.235/0.265 - Spec #19112 - Change min/max from 100/175 to 75/150 • Page 20: Switch Resistance Values Table: - Spec #19210 - change min/max from 1/1.5 to 0.75/1.65 - spec #19220 - change min/max from 14/100 to 11/35 - Spec #19230 - change min from 2 to 1.75 • Page 21 - Central Level Gain and Offset Table - Spec #16394 - change Spec # to 16295 - Replace all “TBDs” with values • Page 21 - ESP Table - Replace all “TBDs” with values • Page 36: Clamp Source - 3rd para: Change MI-IR5% to MI-IR5# - Table 26 - Add Note

DATE	CHANGE
May 15, 2014	• Page 1: Features - Pdq 800mW/chip changed to Pdq 920mW/Chip • Page 11: Power Supply Current Table: replace all “TBDs” with values. • Page 13: Analog Pins Table: Add spec #s 20210 and 20560 • Page 14: DAC Table - Spec #16220: change from -2/+2.5 min/max to -3/+3 min max • Page 16: Measure Current, Table 1 - Change VCC + 12.5V to +12V, VEE = -3.5V to -4V, VDD = +3.25V to +3.45V. • Page 17: Spec #14140 - Change from .5/1.0 min/max to -0.125/+0.0125 min/max - Delete Spec #14141 • Page 19: Delete Spec #s 14803, 14823, 14833, 14843 - Spec 19112: Change from 70/100 typ/max to 175 max - Spec 14710: Change Max +5 to +7 - Spec 14711, 14713: delete Typ values • Page 20: Switch Resistance Values Table - Add spec numbers - Add spec 19250 - Kelvin Alarms Table: Spec 14430 - change test conditions to “not production tested”. • Page 21: Central Level Gain and Offset - Spec #s 16390, 16391, 16290, 16291: replace “TBD” with values

DATE	CHANGE
April 8, 2014	• Page 15: Replace “TBD” with values. • Page 19: MV Temperature Coefficient: Replace “TBD” with values • Page 17: MI Temperature Coefficient’s updated - Add spec # 14141

DATE	CHANGE
January 31, 2014	• Pages 25, 28, 35, 47 - Change ±2*Imax# to ±2*Imax(IR4 or IR5)

DATE	CHANGE
January 27, 2014	• Page 27 - Measurement Unit Figure: Change MI0 through MI7 to MI-S0 through MI-S7 • Page 42 - Figure 15: Change MI0 through MI7 to MI-S0 through MI-S7 • Page 42 - Table 37: Change MI0 through MI7 to MI-S0 through MI-S7

DATE	CHANGE
December 17, 2013	• Page 44 - Table 46: Update last 3 values • Page 45 - Table 48: Column 5: change Con-Res*#<0>=1 to Con-Res##<0> = 0.

DATE	CHANGE
December 6, 2013	• Page 48 - Kelvin Alarm: 1st three paragraphs updated. Table 57: change all SENSE_# to V-VB#. • Page 48 - Kelvin Alarm: Table 57: change all SENSE_# to V-VB#. • Page 48 - Figure 23 updated. • Page 67 - Figure 5 updated.

DATE	CHANGE
October 9, 2013	• Page 16-20 - Resolved formatting issue that caused pages to be dropped from previous revision • Page 13 - Analog Pins: Spec #s 10800 & 10801: Change VCC, VEE to VCC – 0.5V, VEE + 0.5V • Page 21 - Central Gain and Offset: Add Note 1 to Spec 16291; Update Notes 4 and 6 • Page 31 - Short Circuit Limit: update 1st paragraph • Page 31 - Clamp Source: Update 3rd paragraph • Page 32 - Figure 7: update diagram • Page 48 - Kelvin Alarm: remove last sentence from 3rd paragraph

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)
ISL55180CNEZ	ISL55180CNEZ	Tj = 25°C to 100°C	128 Ld, 14 x 20mm LQFP

NOTE: These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Appendix A

ISL55180 Calibration Procedure

1. Calibration Overview

Calibration is the process of transferring accuracy standards from one measurement or source instrument to another. In an ideal case, a voltage applied to the input of a unity gain amplifier would equal the output voltage of the amplifier. In reality, there are several factors that will have an impact of the accuracy of the amplifier and introduce errors. Some of the errors introduced are: input offset voltages, gain errors, and linearity errors. To reduce these types of errors in the amplifiers and their surrounding circuitry, calibration is performed. This accuracy transfer aids in the process of verifying the performance of an instrument is within a set of pre-defined specifications.

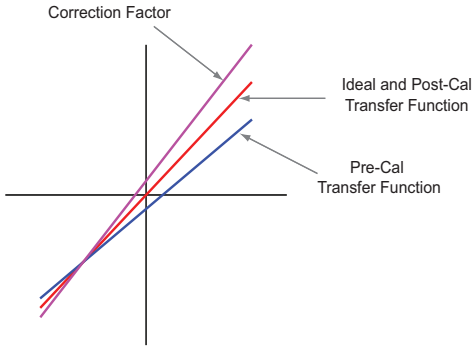


FIGURE 1. CALIBRATION

2. Calibration Basics

1. The basic calibration formula that is used for the ISL55180 calibration routines is the "slope intercept" or straight line equation: Y = (M * X) + B; where M=Gain or slope; B=Offset or y-intercept, X=Input or Independent Variable; Y=Output or Dependent Variable.
   - In the context of this document the variables from the slope intercept equation are referred to as follows: M=Gain; B=Offset; X=Input; Y=Output
   - To calculate the Gain and Offset using 2 Input points and 2 Output points

     -Gain = (Y2 - Y1) / (X2 - X1)

     -Offset = Y2 - (Gain * X2)
   - To solve for Y if X is known Y = Gain * X + Offset
   - To solve for X if Y is known

     -X = (Y - Offset) / Gain
2. Each Path requires its own calibration factors
3. Each op-amp has some gain/offset error contribution
4. Only need 1 calibration factor even if multiple op-amps are in the same path
5. Resistive paths (i.e. muxes, switches) typically don't require additional calibration factors; however could cause gain error (voltage divider)

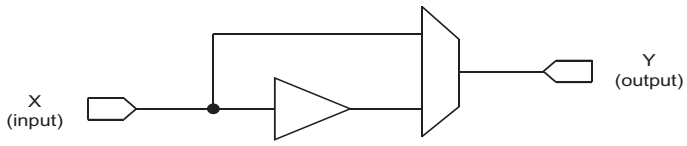


FIGURE 2. CALIBRATION BASICS

3. DC Calibration

Proper calibration is essential to ensure that the ISL55180 is operating with the accuracy expected by the user. The ISL55180 is designed and tested to meet DC accuracy specifications in this datasheet with either a two or four point calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks (ForceA#, ForceB#, I-Cl-Src#, I-Cl-Snk#). In general, most calibration points are at 20% and 80% of the full-scale value for that range for a 2-point calibration. For measure current calibration, a common 4-point/2-segment technique is used with calibration points at +/-80% and +/-20% of the Imax (maximum current) range. The calibration points used for ATE testing are listed separately for each functional block by range in the DC Electrical Specifications section.

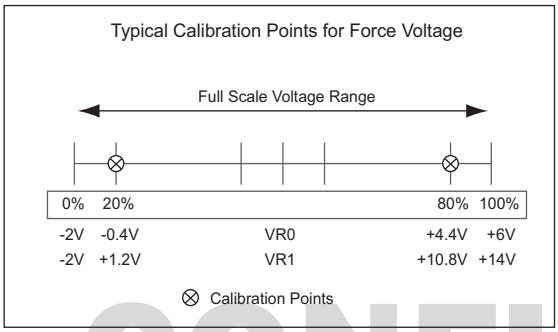


FIGURE 3. TYPICAL FORCE VOLTAGE CALIBRATION POINTS

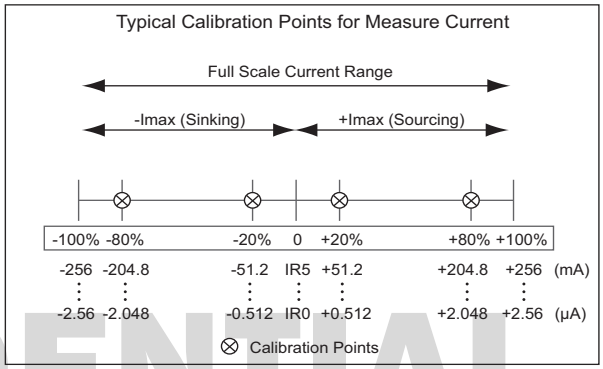


FIGURE 4. MEASURE CURRENT CALIBRATION POINTS

Scope

This document is meant as a basic calibration document for one channel and does not encompass all aspects of the chip. Certain aspects of the calibration have been purposely omitted such as the ganging, the ESP function, Force Current (Using current clamps), Current Clamps, and the per-channel Central Gain and Offset to limit the complexity and length of the calibration documentation. The calibration for these and more complex features will be covered at a later date with Elevate Semiconductor Application Notes.

The calibration methods in the document describe how the ISL55180 has been calibrated in the EVM(Evaluation Module)/ATE (Automated Test Equipment) environment. In an actual customer environment, the ISL55180 would typically be calibrated via the EXT_FORCE/EXT_SENSE pins that would be connected to one main central calibration resource. Due to the limitations of resources in the EVM/ATE environments, the FORCE_# pin or SENSE_# pin were used for some calibration.

Equipment Needed

Analog to Digital Converter, Source Voltage/Current Measurement Unit, Power Supplies

System Level DC Accuracy Limits

Alternate calibration procedures and techniques using more or fewer calibration points may also be employed in order to achieve the desired system level accuracy and make trade-offs between accuracy and calibration time. The resulting system level accuracy may be superior or inferior to the techniques listed below and will be dependent on the specific details of a particular application. To meet the DC specifications in this datasheet, the calibration procedures listed were used.

4. ISL55180 DPS Channel Overview

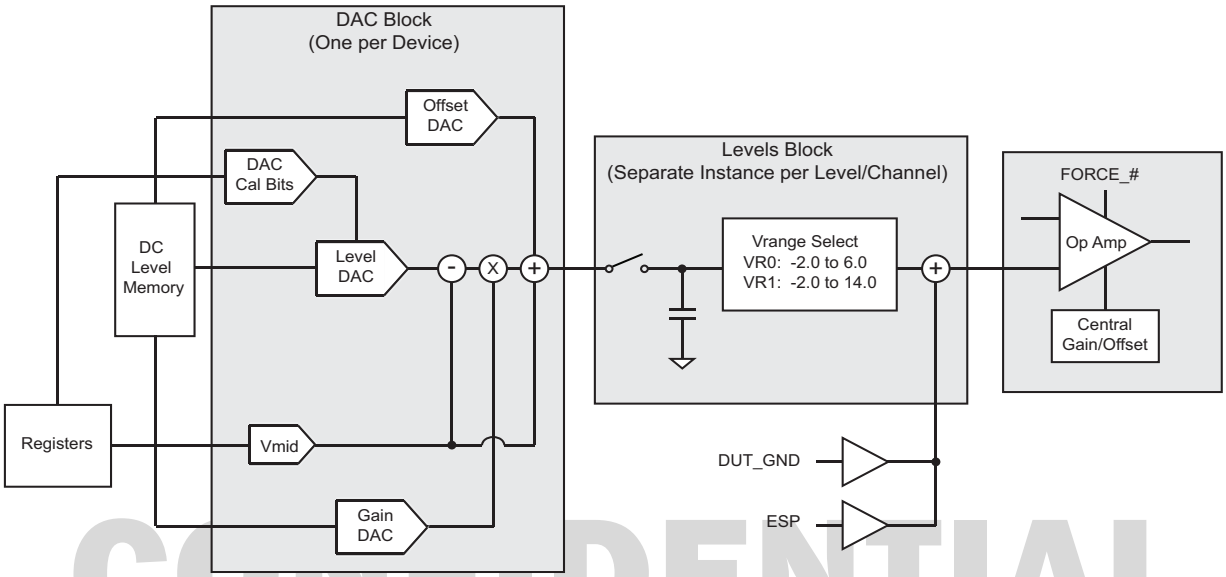


FIGURE 5. ISL55180 DPS CHANNEL

The ISL55180 DPS channel is comprised of several blocks as shown in Figure 5 above. There is one on-chip sample and hold 16-bit DAC that creates the required output voltage levels for all on-chip level functionality. The DAC circuit is comprised of a main Level DAC and has registers and logic which allow for on-chip calibration of this main Level DAC via the Offset and Gain correction DACs. Each Level DAC, Offset DAC, and Gain DAC has addressable registers which are accessible to the user through the CPU port. The values programmed into the Offset and Gain registers are calculated during a calibration procedure. The Gain/Offset DACs are calibrated independently and the calibration values are globally applied to all Functional Blocks. The Level DAC, voltage range select, and output forcing amplifiers are calibrated together to obtain specific per level calibration values. Vmid corresponds to a Value DAC code of 0x7fff and is the value at which the level Pivots. The Offset DAC and Gain DAC provide a hardware correction and allow an application to broadcast the same Level DAC code to many separate parts or channels at one time. The Sample and hold portion of the DAC will not be covered in this section, but to get more information see the DAC Sample and Hold (S/H) State Machine section of this data sheet. Following the S/H cap is the Voltage Range select section of the channel. There are 2 voltage range options for the ISL55180: 8V and a 16V Range. DUT_GND (DUT Ground)is then added to the level to make sure the output voltage level of the ISL55180 is relative to the DUT. A central Gain/Offset can then added to the voltage level at the output Op-Amp to compensate for any errors when sharing one level among multiple channels.

5. Hardware/Software Calibration Distinction

A Hardware Calibration nomenclature implies a software algorithm is used to calibrate and determine the calibration values. The calibration values are then loaded into the ISL55180 (hardware registers/RAM) which then applies the calibration correction factor. The ISL55180 contains Gain and Offset calibration registers for all of the DC Levels. In addition, the ISL55180 contains calibration registers for the DAC MSB (Most Significant Bit) Calibration Bits, DAC LSB (Least Significant Bit) Auto-Calibration, and CME (Common Mode Error) Adjust.

The Software Calibration nomenclature implies a software algorithm is used to calibrate and determine the calibration values. Software is then required to apply the calibration correction factor to determine the actual result and store the calibration values until use. These include the calibration for the Gain DAC, Offset DAC, MV (Measure Voltage), and MI (Measure Current).