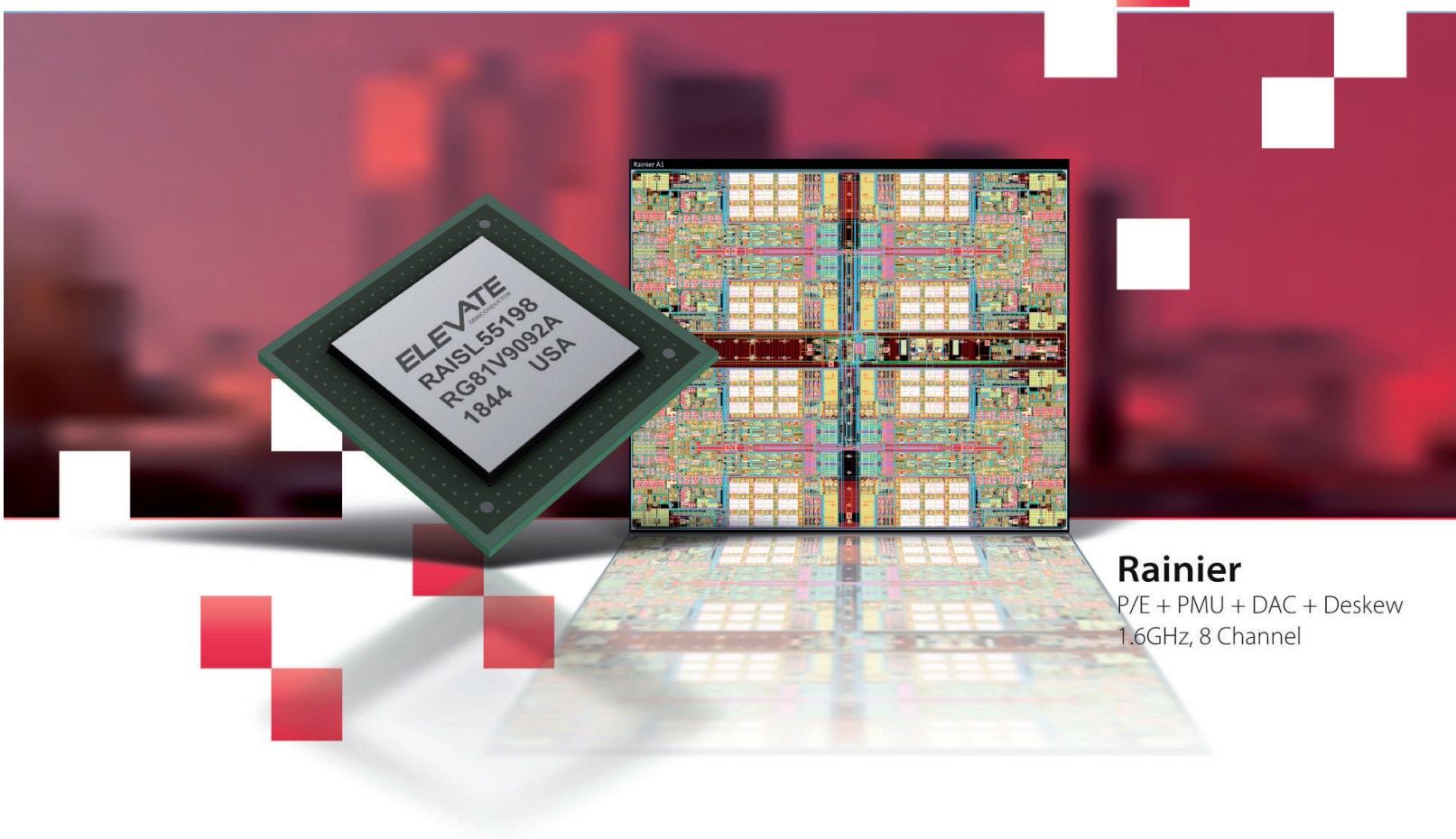
PRODUCT SELECTION GUIDE

AUGUST 2022

Integrated Components for Automated Test Equipment

Confidential 2022



Rainier

P/E + PMU + DAC + Deskew

1.6GHz, 8 Channel

Powering the Next Generation of Semiconductor Test

ELEVATE SEMICONDUCTOR

www.elevatesemi.com

NEW PRODUCTS

New Products

Amid ongoing global supply chain issues in the semiconductor industry, ElevATE has substantially ramped up production and innovation to address persistently high demand. New products currently under development include an SOC Dual High-Voltage DPS/VI (Whitney), a 1.6GHz Octal Pin Electronics Driver (Rainier) and a Quad High-Performance DPS (Kilauea).

Engage With ElevATE

Our experienced team of engineers can assist. Whether you are designing your own semiconductor, need a turnkey ATE solution, or just need assistance in your own development, ElevATE can help anywhere along the process.

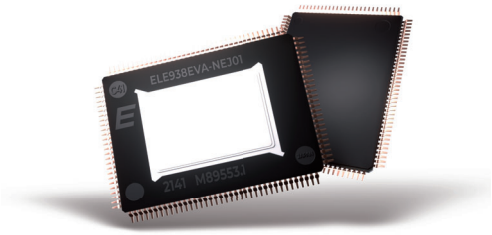
ELE58HOA (Hood) - SOC Octal High-Density PMU

ELE44WH1 (Whitney)

SOC Dual Channel +/-60V PMU/DPS

** Product Under Development- Specifications Subject to Change*

Whitney is a two channel +/-60V, highly-integrated System-on-a-Chip (SOC) per-pin parametric unit (PPMU). Each channel includes the capability to force voltage, force current, measure voltage, measure current, and make window compare measurements. Six 16-bit DACs included in each channel are used to accomplish the above. The functionality of the Whitney device is controlled using a SPI interface that can clock up to 100MHz.



Features

- Per-Pin PMU
- Wide Output Voltage Range. 60V Output Range across –60V to +60V Common Mode 8V Driver Output Swings

- 2 Per-Pin V/I's
- Flexible compensation options
- 4-Quadrant Operation (FV/MI/FI/MV - any Force/Measure Combination
- Extremely Wide V/I Operating Range
- 5 On-Chip Current Measure Ranges ±2µA, ±20µA, ±200µA, ±2mA, ±50mA
- 3 On-Chip Current Force Range, ±200µA, ±2mA, ±50mA
- 1 External High Current Force/Measure Range
- Up to ±200mA (Using an External Resistor)
- Per-Channel Wide-Voltage Window Comparator
- Go-No-Go Functional Testing
- Low Leakage Across Entire Voltage Range
- Gangable

- On-Chip DC Levels
- Per Level Offset Correction
- 16-bit Resolution/14-bit Accuracy
- High and Low DUT Sens

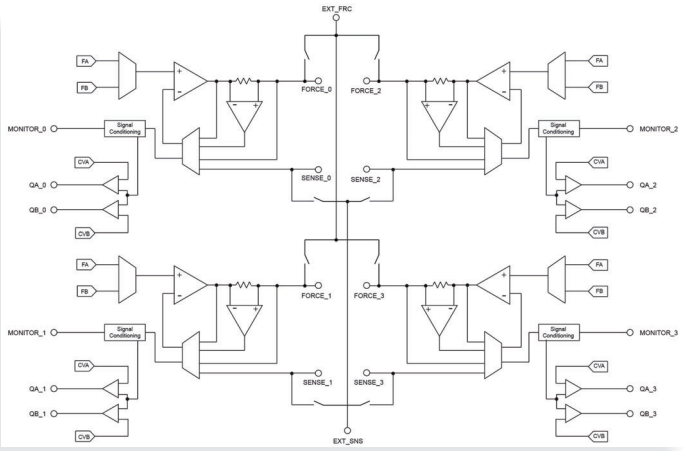
- Per-Channel Monitor Pins
- Integrated ADC Pre-Conditioning

- Up to 100MHz SPI Interface

- Package/Power Dissipation
- Lead Free (RoHS Compliant)
- Extremely Small PCB Footprint
- 14mm x 20mm, 128 Lead LQFP w/Exposed Heat Slug
- Pdq 800mW/Channel (Full Scale Supplies)

Applications

- Automated Test Equipment
- Avionics/Military Equipment
- Automotive
- IoT Test Equipment

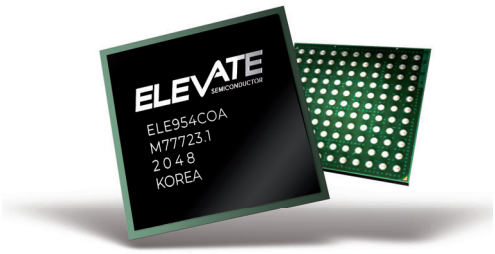


Kilauea

SOC Quad High-Performace DPS

** Product Under Development- Specifications Subject to Change*

Kilauea is a highly-integrated System-on-a-Chip (SOC) Device Under Test (DUT) power supply solution incorporating 4 independent DUT Power Supply (DPS) units. The interface, control, and I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-channel basis.



Features

- Per-Channel DPS
- FV, FI, MV, MI, Hi-Z Capability
- 28V Measure Voltage Input Compliance Range
- 3 Force Voltage Ranges (3.2V, 17V, 28V), -0.1V to 3.1V, -7V to +10V, -2 to 26V force voltage range
- 4 Measure Voltage Ranges (4V, 8V, 17V, 28V)
- 7 Current Ranges: (1200mA, 400mA, 40mA, 4mA, 400µA, 40µA, 4µA)
- Programmable Voltage and Current Clamps
- Programmable slew control. Range is 3-bit control over 1mS to 100mS range
- Programmable compensation control
- Guard circuit to enhance sensitive low current measurement application

- Power Management
- Independent Output Buffer Power Supply (VCCO)
- Ability to Exceed VCCO in Lower Current Ranges

- Flexible Ganging Capability
- No Restrictions on Maximum # DPS Units

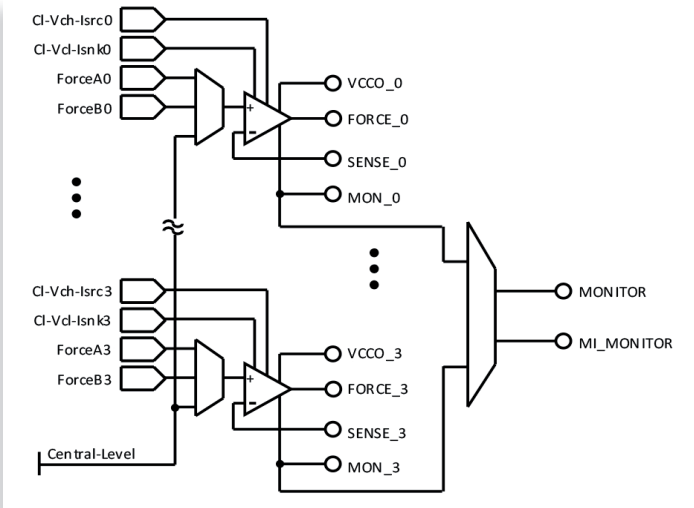
- Protection
- On-Chip Junction Temperature Monitor
- Over-Temperature Shut Down per Chip
- Kelvin Connection Sensing/Alarm per Channel
- Over-Current Sensing/Alarm per Channel

- On-Chip DAC to Generate DC Levels
- 2 Independent FV Levels/Channel
- Central Resource Mode w/16 Selectable Levels
- Independent Source and Sink Clamps
- 16 bits/Level
- On-Chip Offset and Gain Correction per Level

- Package/Power Dissipation
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pdq ≤ 500mW/Channel

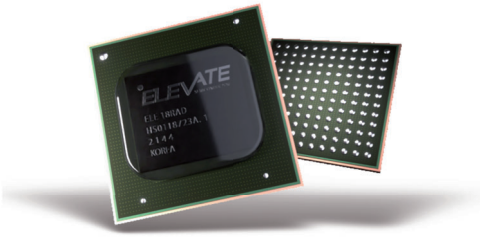
Applications

- Automated Test Equipment (ATE)
- Logic/ASIC Verifiers
- Instrumentation



** Product Under Development- Specifications Subject to Change*

Rainier is a highly-integrated System-on-a-Chip (SoC) pin electronics solution that incorporates every analog function, along with digital support circuitry required to create 8 independent pin channels for Automated Test Equipment. Each channel is configured via a 100MHz SPI interface, and all real-time data is programmed and read back through high-speed differential SSTL pins that can be configured to interface directly to other devices using multiple single-ended and differential logic families.



Features

- Pin Electronics Driver/Comparator
- 3-level Driver (DVH/DVL/VTT)
- 100mV to 6V Swing Across -1.5V to +4.5V Range
- Extremely Low Hi-Z Leakage over Entire I/O Range
- Short Circuit Protection
- Up to 6V Comparator Input Range
- 1.2GHz Comparator Equivalent Bandwidth

- Per-Pin PMU
- FV, FI, MV, MI
- 5 FI/MI Current Ranges (±4µA, ±40µA, ±400µA, ±4mA, ±40mA
- 4 Quadrant Operation
- +13V Super Voltage Capability
- Programmable Voltage and Current Clamps
- Go-No-Go Comparators

- On-Chip DC Levels
- Dedicated Level DACs per Channel
- Per Level Offset Correction
- 16-bit Resolution/14-bit Accuracy
- DUT Ground Sensing and Correction (1 Per Chip)

- Per-Pin Active Load
- 2 Active Load Ranges (±24mA, ±1mA)
- Independently Programmable Current Source, Current Sink, and Commutating Voltage levels

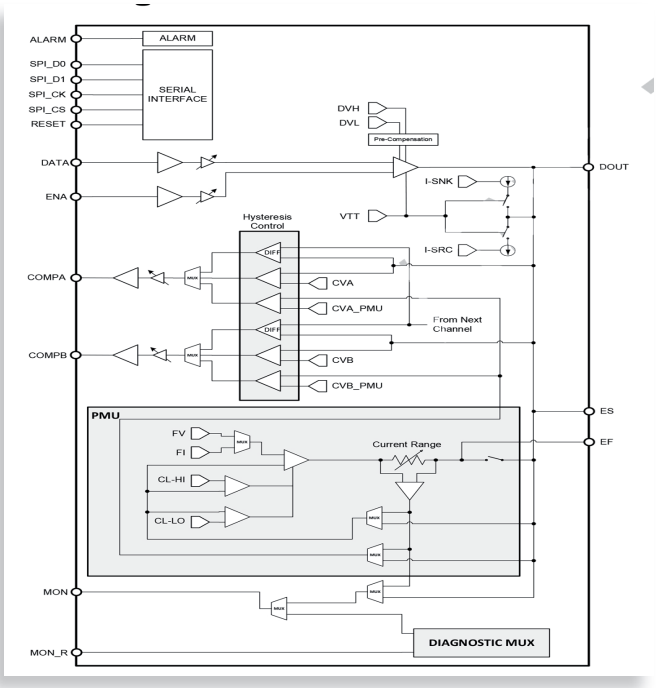
- Per-Pin Timing Deskew
- Propagation Delay Adjustment
  - 1.4ns Delay Adjustment Range
  - 1.4ps Delay Adjustment Resolution
- Falling Edge Adjust Range -100ps to 100p

- 100MHz SPI Interface
- High-Speed FLEX I/O
- Analog Measure Bus

- Lead Free Package
- 14mm x 14mm, 144 Ball FcBGA (1.0mm Pitch)

Applications

- Automated Test Equipment (ATE)
- Instrumentation and Characterization Equipment
- ASIC Verifiers



Powering the Next Generation of Semiconductor Test

Integrated Components for Automated Test Equipment

- Integrated Pin Electronics
- Integrated DUT Power Supplies
- Integrated V/I and PPMUs
- High Current Pin Drivers

At ElevATE, we know firsthand how fast the semiconductor market is changing. New, self-driving vehicles, safety systems requiring 3 to 5x the intelligence of previous generations, artificial intelligence systems being deployed in more and more applications all spell the same thing for the future of semiconductor test: evolutionary change just won't cut it; revolutionary change is required! We design state-of-the art products, utilizing technology that allows for the highest density in the industry - built for the requirements of the next 20 years, not the last 20.

ElevATE takes test seriously – in fact, we are the last major standalone ATE IC company in the industry. Our founders hail from Brooktree experience in the ATE business during the 90s and have remained in the industry ever since; our products have lifecycles measured in decades, not 2-5 years like other semiconductor manufacturers. Over the past 3 years our team has grown considerably in Applications Engineering, Quality Engineering, and Design/Product Engineering. We hire people with a passion for building leading edge analog circuits, then testing them extensively to make sure they work in any environment. As a private, well-funded company we are not subject to the whims of wall street or corporate America with its quarterly earnings targets or shifting priorities; we are simply focused on our test customers' needs and driving the technology to its limits to meet those needs. As we continue to grow, we are excited to start more innovative projects, and to release more parts in the next 3 years than we have in the past 5 years.

David J. Kenyon, CEO and President

Engage us and see why we are the right choice for your semiconductor test needs, now and in the future.

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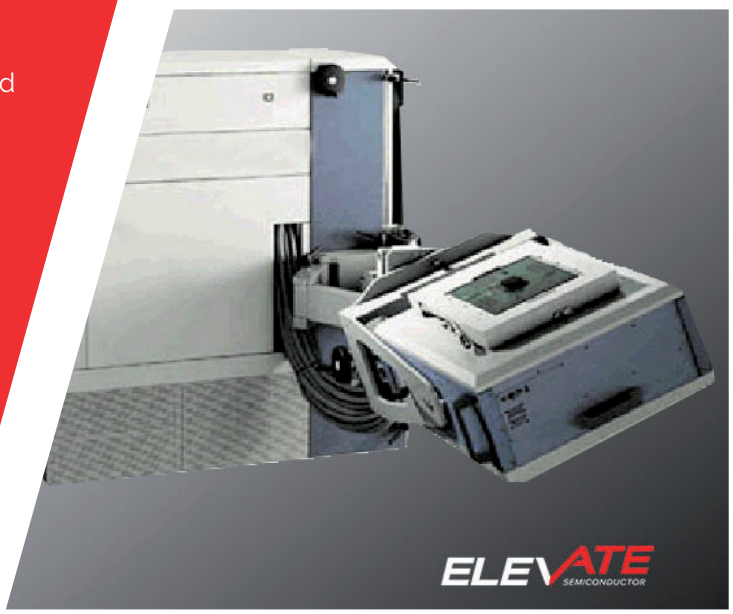
Integrated Digital Pin Electronics

ElevATE is the market leader in low power, high density integrated pin electronics. Developed in a pure CMOS technology, our products enable customers to develop next-generation high density instruments with increased parallelism for reduced cost of test and improved system reliability. Integrated timing delay, or "Deskew," circuitry comes standard on our integrated pin electronics products and enables flexible timing control and edge placement in a system without the need for an expensive ASIC. Packed with system-level features, these products greatly simplify the design of ATE systems for improved time to market.



ATE Manufacturer Solutions

ATE Manufacturer Solution Channel Controller

- Pattern Generator
- Timing Generator
- Format Section
- Error Section
- All Other Blocks

ElevATE Solutions

- Pin Electronics
- Deskew
- PPMU
- DACs
- Digital Support Functions

DUT

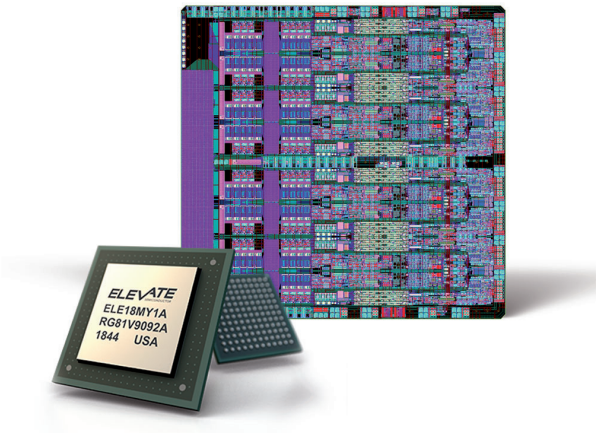
Integrated Digital Pin Electronics Table

	Product	ELE18MY1 (Mystery)	ISL55161 (Venus4)	ISL55163 (Venus4 Lite)	ISL55162 (Venus3)	ISL55164 (Venus)	ISL55169 (Mercury)	ISL55188 (Saturn)	ELE22K12A (Kilimanjaro)
Overview	Description	P/E + PPMU + DAC + Deskew + Load	P/E + PMU + Load + DAC + Deskew	P/E + PMU + Load + DAC	P/E + PMU + DAC + Deskew	P/E + PMU + DAC + Deskew	P/E + PMU + DAC + Deskew	P/E + PMU + DAC + Load + Deskew	Pin Driver + Window Comp
	Status	Production	Production	Production	Production	Production	Production	Production	Production
	# Channels	8	2	2	2	2	8	2	2
	Package	14mm x 14mm 144 Ball FcBGA (1.0mm Pitch)	10mm x 10mm TQFP w/exposed slug up 9mm x 9mm QFN (Top Exposed Paddle)	10mm x 10mm TQFP w/exposed slug up 9mm x 9mm QFN (Top Exposed Paddle	10mm x 10mm TQFP w/exposed slug up	10mm x 10mm TQFP w/exposed slug up	14mm x 20mm TQFP w/exposed slug up	14mm x 20mm TQFP w/exposed slug up	5mm x 5mm QFN w/exposed slug down
	Pdq	1.1W/Channel	500mW/Channel	500mW/Channel	1.1W/Channel	1.1W/Channel	500mW/Channel	1.5W/Channel	125mW/Channel
Pin Electronics	Fmax	500MHz	400MHz	400MHz	300MHz	133MHz	66MHz	75MHz	100MHz
	Driver	Dual Mode 3-level Driver	3 Level/8V	3 Level/8V	3 Level/8V	3 Level/8V	2 Level/8V	2 Level/24V	2 Level/15V
	Compara-tor	8V	16V	16V	16V	16V	16V	32V	15V
	Load	Active	Active, ± 24mA	Active, ± 24mA	Resistive	Resistive		Active, ± 24mA	
	DC Levels	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	Off-Chip
PMU	PMU	1/Channel	1/Channel	1/Channel	1/Channel	1/Channel	1/Chip	1/Channel	
	DC Levels	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	
	Imax	50mA	32mA	32mA	32mA	32mA	32mA	200mA	
Deskew	Delay	7ns	3.2ns - 5.0ns		6.4ns - 12.8ns	8ns - 20ns	10ns - 20ns	10ns - 20ns	
	FEA	-50ps to 50ps	±50% of Delay		±12.5% of Delay	±25% of Delay	±25% of Delay	±25% of Delay	
	Resolution	10ps	12ps - 20ps		12ps - 25ps	15ps - 37.5ps	312.5ps - 625ps	312.5ps - 625ps	

ELE18MY1 (Mystery)

SOC Octal 500MHz Integrated Pin Electronics /PMU/DAC/Load/Deskew

Mystery is a highly-integrated SOC pin electronics solution that incorporates every analog function, along with digital support circuitry required to create 8 independent pin channels for Automated Test Equipment. Each channel is configured via a 100MHz SPI interface, and all real-time data is programmed and read back through high-speed FLEX I/O pins that can be configured to interface directly to other devices using multiple single-ended and differential logic families.



Features

- Pin Electronics Driver/Comparator
- Dual Mode 3-level Driver with Hi-Z Capability (DVH, DVL, VTT)
- HV (High Voltage) Driver Mode
  - 25mV to 8V Swing Across –2V to +6V Range
  - Programmable Driver Slew Rate
- HS (High Speed) Driver Mode
  - 25mV to 4V Swing Across 0V to +4V Range
- Up to 8V Comparator Input Range
- 1GHz Comparator Equivalent Bandwidth
- Extremely Low Hi-Z Leakage over Entire I/O Range
- Short Circuit Protection

- Per-Pin PMU (PPMU)
- FV, FI, MV, MI
- 4 Quadrant Operation
- –2V to +6V FV/MV Range
- 5 Current Ranges (±2µA, ±20µA, ±200µA, ±2mA, ±50mA)
- Programmable Voltage and Current Clamps
- Resistive Load Function (12 Selectable Resistor Values)

- On-Chip DC Levels
- 17 True DAC levels per Channel (not Sample and Hold)
- Per Level Offset Correction
- 16-bit Resolution/14-bit Accuracy
- DUT Ground Sensing and Correction (1 Per Chip)

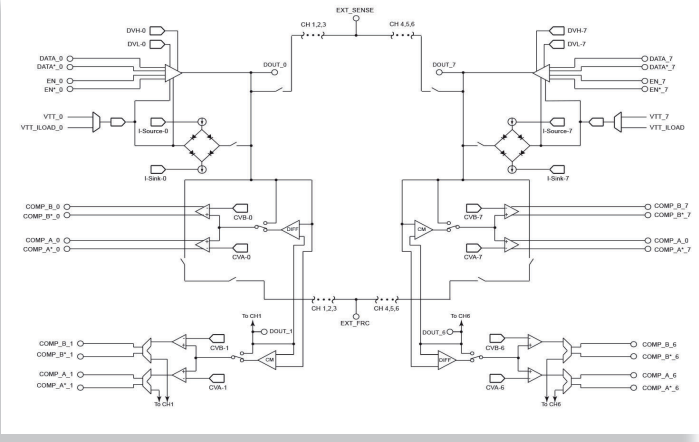
- Per-Pin Active Load
- +/- 24mA Maximum Current
- Independently Programmable Current Source, Current Sink, and Commutating Voltage levels

- Per-Pin Deskew
- Propagation Delay Adjustment
- 7ns Delay Adjustment Range
- 10ps Delay Adjustment Resolution

- Package/Power Dissipation
- 14mm x 14mm 144 Ball FcBGA
- Pdq ≤ 1.1W/Channel

Applications

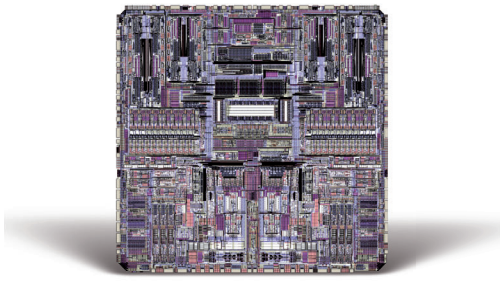
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



ISL55161 (Venus4)

SOC Dual Channel 400MHz Integrated Pin Electronics /PMU/DAC/Load/Deskew

Venus4 is a highly integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per-channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each Venus4 chip.



Features

- Pin Electronics Driver/Comparator
- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings
- Extremely Low Hi-Z Leakage over 16V Range
- Differential Driver and Comparator Modes
- 16V Comparator Input Compliance Range

- PMU
- FV, FI, MV, MI
- FI Voltage Clamps
- Eight current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
- Resistive Load (eight selectable resistor values)
- Remote Sense Option

- On-Chip DC Levels
- 13 DAC Levels/Channel
- Gain and Offset Correction/Level
- DUT Ground Sensing and Corrections

- Active Load
- 24mA Imax
- 16V Input Compliance Range
- Extremely Low Hi-Z Leakage over 16V Range
- Independent Power-down Option

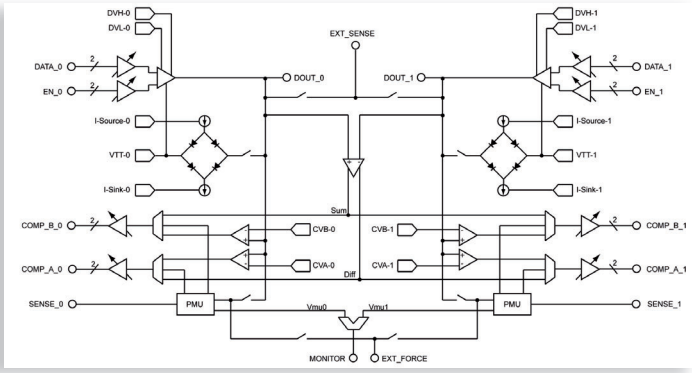
- Deskew
- Propagation Delay Adjustment
- Falling Edge Adjustment

- Flexible High-Speed Digital Inputs and Outputs
- Selectable On-chip Terminations for Inputs
- Read-back Internal States

- Package/Power Dissipation
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pdq ≤ 1.1W/Channel @ 11V Operation

Applications

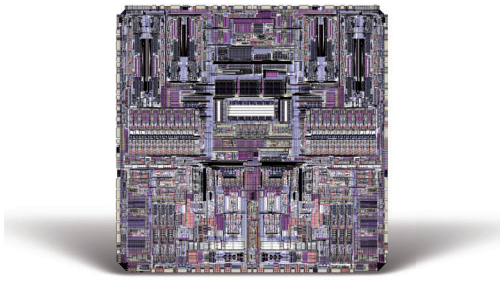
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



ISL55163 (Venus4 Lite)

SOC Dual Channel 400MHz Integrated Pin Electronics /PMU/DAC/Load

Venus4 Lite is a highly-integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per-channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip. Venus4 Lite is pin compatible with Venus4.



Features

- Pin Electronics Driver/Comparator
- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings
- Extremely Low Hi-Z Leakage over 16V Range
- Differential Driver and Comparator Modes
- 16V Comparator Input Compliance Range

- PMU
- FV, FI, MV, MI
- FI Voltage Clamps
- Eight current Ranges (32mA, 8mA, 2mA, 512µA, 128µA,
- 32µA, 8µA, 2µA)
- Resistive Load (eight selectable resistor values)
- Remote Sense Option

- On-Chip DC Levels
- 13 Levels/Channel
- Gain and Offset Correction/Level
- DUT Ground Sensing and Correction

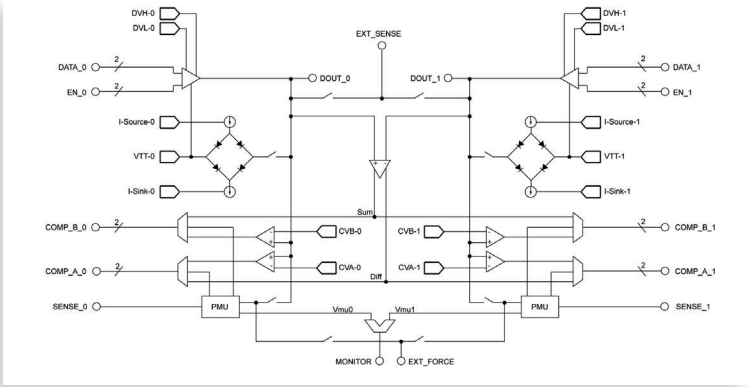
- Active Load
- 24mA Imax
- 16V Input Compliance Range
- Extremely Low Hi-Z Leakage over 16V Range
- Independent Power-down Option

- Flexible High-Speed Digital Inputs and Outputs
- Selectable On-chip Terminations for Inputs
- Read-back Internal States

- Package/Power Dissipation
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pdq ≤ 500mW/Channel

Applications

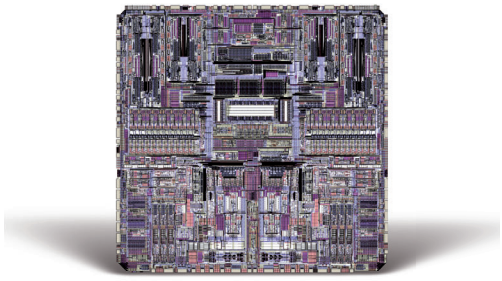
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



ISL55162 (Venus3)

SOC Dual Channel 300MHz Integrated Pin Electronics /PMU/DAC/Deskew

Venus3 is a highly-integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support circuitry, required on a per-channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip. Venus3 is pin and functionally compatible with Venus.



Features

- Pin Electronics Driver/Comparator
- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings
- 16V Comparator Input Compliance Range
- Extremely Low Hi-Z Leakage over 16V Range

- Per-Pin PMU
- FV, FI, MV, MI
- 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
- 4 Quadrant Operation
- +13V Super Voltage Capability
- FI Voltage Clamps
- Resistive Load (8 selectable resistor values)

- On-Chip DC Levels
- 11 Levels/Pin
- Gain and Offset Correction/Level
- DUT Ground Sensing and correction

- Deskew
- Propagation Delay Adjustment
- Falling Edge Adjustment
- Delay Range set by PLL Clock

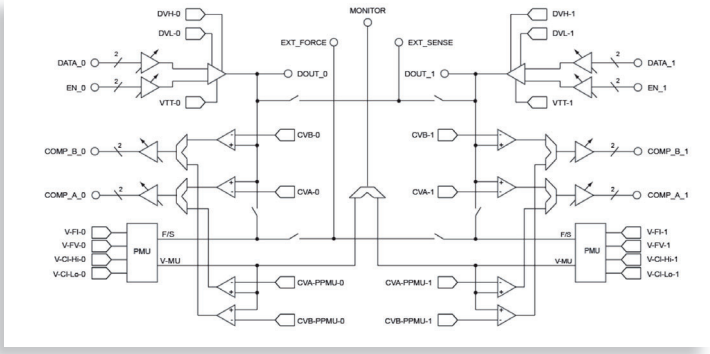
- Flexible High-Speed Digital Inputs and Outputs
- Selectable On-Chip Terminations for Inputs
- 50Ω Series Termination for Comparator Outputs

- 3-Bit Serial CPU Port

- Lead Free Package
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pdq < 1.1W/Channel

Applications

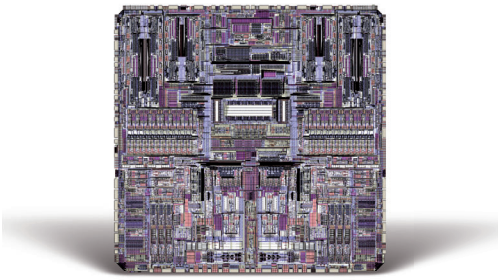
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



ISL55164 (Venus)

SOC Dual Channel 133MHz Integrated Pin Electronics /PMU/DAC/Deskew

Venus is a highly-integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per-channel basis for Automated Test Equipment, The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip. The Venus chip is pin and functionally compatible with Venus3.



Features

- 133MHz
- 3.75ns Minimum Pulse Width

- Pin Electronics Driver
- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings

- Per-Pin PMU
- FV, FI, MV, MI
- 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
- +12V Super Voltage Capability
- Resistive Load (8 selectable resistor values)

- On-Chip DC Levels
- 11 Levels/Channel
- Gain and Offset /Level
- DUT Ground Sensing /Pin

- Deskew
- Propagation Delay Adjustment (up to 12.8ns range)
- Falling Edge Adjustment (up to ±3.2ns range)
- Auto Calibration via PLL

- Pin Electronics Comparator
- Extremely Low Leakage over a 16V Input Range
- 16V Comparator Input Voltage Range

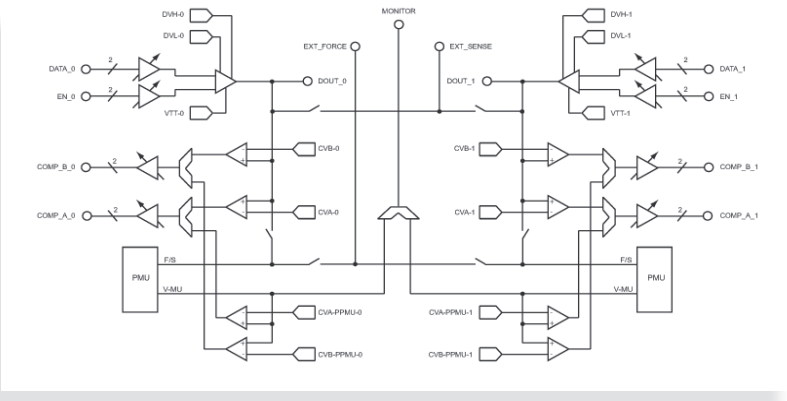
- Flexible High-Speed Digital Inputs and Outputs

- 3-Bit Serial CPU Port
- Load Internal Registers and Memory
- Read Back Internal States
- Selectable On-chip Terminations for High-Speed Inputs
- 50Ω Series Terminated High-Speed for Comparator Outputs

- Package/Power Dissipation
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pdq ≤ 1.10W/Channel; Pdq ≤ 2.2W/Chip

Applications

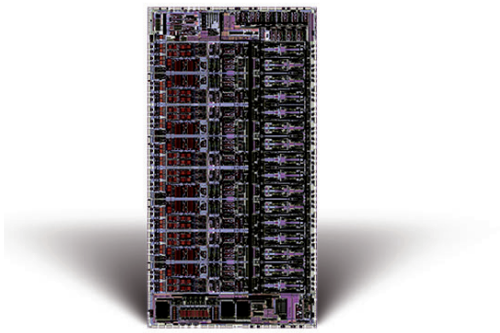
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



ISL55169 (Mercury)

SOC Octal 66 MHz Integrated Pin Electronics/PMU/Deskew

Mercury is a highly-integrated SOC pin electronics solution aimed at incorporating every analog function (with some digital support functionality) required on a per-channel basis for Automated Test Equipment. The interface, control, and I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.



Features

- 66MHz
- 7.5ns Minimum Pulse Width

- Pin Electronics Driver
- 2 Level Driver w/ On Chip Buffers
- 8V Driver Output Swings
- Extremely Low Leakage over a 16V Hi-Z Range

- Per-Chip PMU
- FV, FI, MV, MI
- 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
- 12V Super Voltage Capability

- On-Chip DC Levels
- 4 Levels / Channel
- 8 Levels / Central PMU
- 16 Bits per Level
- 16 Bit per Level Offset Correction
- 16 Bit per Level Gain Correction

- Deskew
- Propagation Delay Adjustment (up to 20ns range)
- Falling Edge Adjustment (up to ±5ns range)
- Auto Calibration via PLL

- Pin Electronics Comparator
- Extremely Low Leakage over a 16V Input Range
- 16V Comparator Input Voltage Range

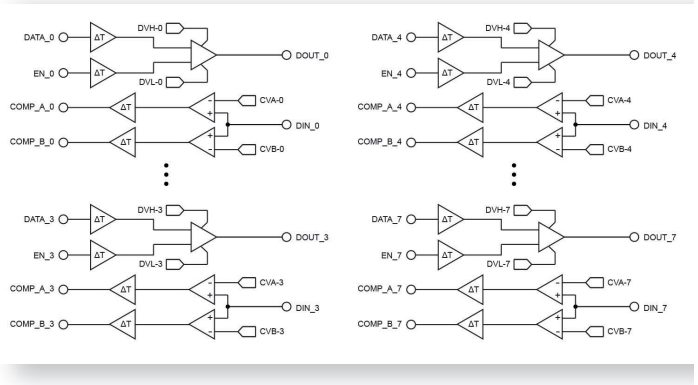
- Flexible High-Speed Digital Inputs and Outputs
- 50Ω Series Terminations High-Speed for Comparator Outputs
- Selectable On-Chip Terminations for High-Speed Inputs

- 3-Bit Serial CPU Port
- Load Internal Registers and Memory
- Read Back Internal States
- Selectable On-chip Terminations for High-Speed Inputs
- 50Ω Series Terminated High-Speed for Comparator Outputs

- Package/Power Dissipation
- 128 Lead, 14mm X 20mm, TQFP w/ Heat Slug
- Pdq ≤ 500mW/Channel; Pdq ≤ 4.0W/Chip

Applications

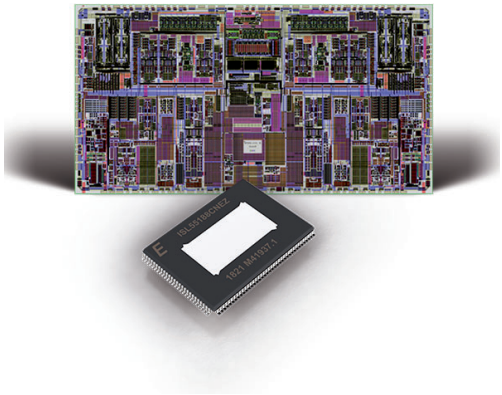
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



ISL55188 (Saturn)

SOC, Dual Channel Integrated Pin Electronics/PMU/DAC/Deskew

Saturn is a highly-integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per-channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip.



Features

- Pin Electronics Driver
- 75 MHz Fmax
- 2 Level Driver (DVH / DVL)
- DC Level Generators On Chip
- 24V Driver Output Swings
- Adjustable Output Voltage Range (-15V to +24V)
- Programmable Slew Rates (1 V/ns to .1 V/ns)
- Iout = 200 mA (DC)
- Extremely Low Leakage Over the operating Range

- PMU
- 5 Current Ranges
- (200 mA, 20 mA, 2 mA, 200 µA, 20 µA,)
- FV / MI
- FI / MV
- Imax = 200 mA

- On-Chip DC Levels
- 10 Levels / Channel; 16-Bit Levels
- 16-Bit Gain and 16-Bit Offset Correction / Level
- DUT Ground Sensing and Correction

- Deskew
- Propagation Delay Adjustment
- Falling Edge Adjustment
- Delay Range set by PLL Clock

- Pin Electronics Comparator
- Threshold Level Generators On Chip
- Extremely Low Leakage over a 32V Range
- 32V Comparator Input Compliance Range
- Differential Comparator

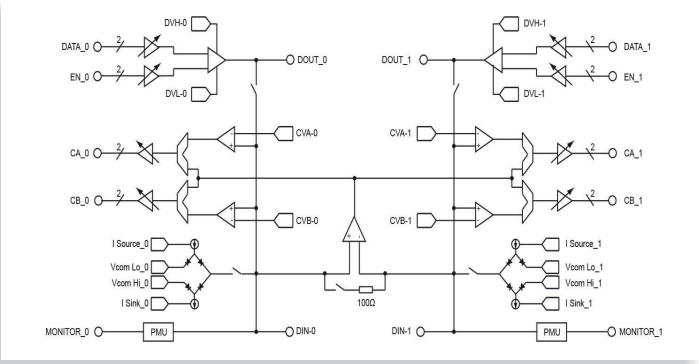
- 3-Bit Serial CPU Port
- 2 Control Bits per Channel (for Ext Relay Support)

- Flexible Real Time Digital Inputs and Outputs
- 50Ω Series Terminations for Comparator Outputs
- Selectable On-Chip Terminations for Inputs

- Package
- 128 Lead, 14mm X 20mm, TQFP w/Heat Slug
- Pdq < 1.5 Watts/Channel; Pdq < 3.0 Watts/Chip

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifier

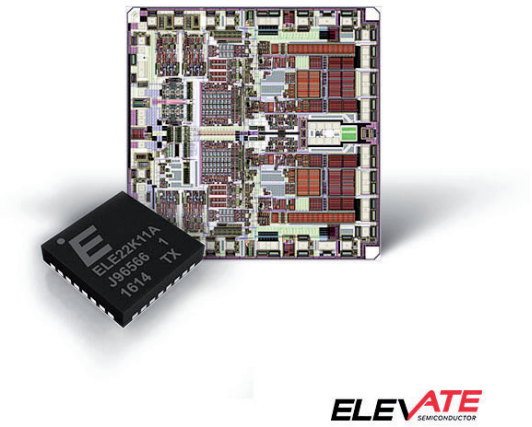


ELE22K12A (Kilimanjaro)

Dual Channel, Pin Electronics

Kilimanjaro is a dual channel pin electronics driver and window comparator fabricated in a wide-voltage Bi-CMOS process. It is designed specifically for Test During Burn-In (TDBI) applications and low cost testers where cost, functional density, and power are all at a premium.

Kilimanjaro incorporates two channels of programmable drivers and window comparators into a small 5mm x 5mm QFN package. Each channel has per-pin driver levels, data, and high-impedance control, along with per-pin high and low window comparator thresholds levels.



Features

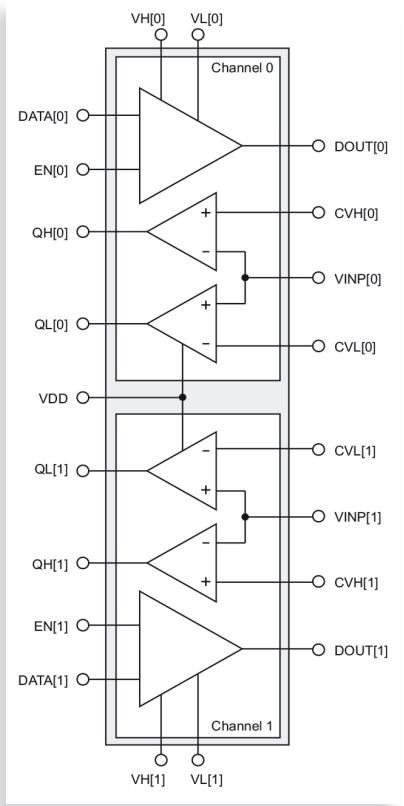
- 15V I/O Range
- 125mA DC Current Capability
- Low Output Impedance
- 100MHz Operation
- Driver Short Circuit Protection
- Per-Pin Flexibility
- Programmable Input Thresholds
- LVTTL Compatible I/O
- Small Footprint (5mm x 5mm QFN with Exposed Heat Slug)
- Improved Small Signal Swing and Timing Performance
- Low Preshoot/Overshoot/Undershoot

- Package

- 32 Lead, 5mm X 5mm, QFN

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifier



Integrated PMU, DPS and V/I Products

ElevATE is the market leader in integrated PMU, V/I, and DPS products. We have leveraged our knowledge and expertise in system-on-a-chip solutions to offer the widest product portfolio available in this space. As a pioneer in the integrated analog pin space, we have developed products with the most advanced features in the industry. These features include ground-breaking advances in technology like glitch-free current measurement range changing, programmable pole and zero placement, less than 0.5V force amp headroom for improved system efficiency, and "ESP," a method to double the DPS density of existing systems. With a myriad of fully integrated, scalable, and digitally reconfigurable solutions available, we are confident that you will find a solution for your testing challenges.

ATE Manufacturer Solutions

ElevATE Solutions

- DUT Power Supplies
- DACs
- External Force and Sense Switches
- Overcurrent Protection

DUT

Integrated PMU, DPS and V/I Table

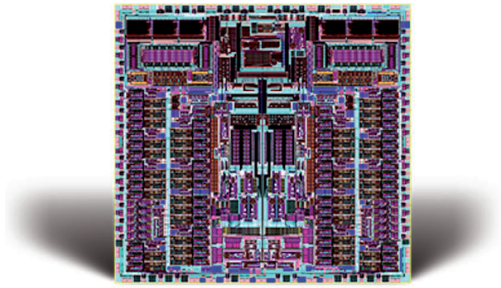
	Product	ISL55187 (Neptune Plus)	Pluto2-301N (Pluto2)	ISL55185 (Triton)	Jupiter -314N (Jupiter)	ISL55180 (Europa)	ELE58VE2A (Vesuvius)	ELE58HOA (Hood)
Overview	Description	Integrated PMU + Companion DAC Levels	Integrated PMU + 10MHz Pin Electronics	Integrated V/I	Integrated DPS	Integrated DPS	Integrated DPS	Integrated PMU
	Status	Production	Production	Production	Production	Production	Production	Production
	# Channels	2	8	8	1	8	8	8
	Package	8mm x 8mm QFN w/ exposed slug down	14mm x 20mm TQFP w/ exposed slug up	14mm x 20mm TQFP w/ exposed slug up	10mm x 10mm TQFP w/ exposed slug up	14mm x 20mm TQFP w/ exposed slug up	14mm x 20mm TQFP w/ exposed slug up	10mm x 10mm MLF w/ exposed slug down
	Pdq	343mW/Channel	125mW/Channel	350mW/Channel	1W/Channel	100mW/Channel	115mW/Channel	150mW/Channel
Details	Architecture	Traditional	Traditional	Traditional	Glitch-Free	Glitch-Free	Glitch-Free	Traditional
	DC Levels	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip	On-Chip
	Imax	64mA Gangable	64mA Gangable	24mA	1A Gangable	256mA Infinitely Gangable	512mA Infinitely Gangable	50mA
	FV Range	14V	14V	28V	20V	14V	14V	8.5V

ISL55187 (Neptune Plus)

SOC Dual Channel Integrated PMU/DAC/Resistive Load

Neptune Plus is a highly-integrated SOC pin electronics support solution incorporating two independent channels of:

- PMU
- DC Levels for the Pin Electronics
- Resistive Load



The interface, control, and I/O are digital. All analog circuitry is inside the chip. Two complete and independent channels are integrated into each chip. For most tester applications, except for the pin electronics, no additional analog hardware is required on a per-pin basis.

Features

- Per-Pin PMU
- FV, FI, MV, MI
- 8 Current Ranges (32mA, 8mA, 2mA, 512µA, 128µA, 32µA, 8µA, 2µA)
- FI Voltage Clamps
- FV Current Clamps
- On-Chip Current Ganging
- Supports 64mA/Channel in FV Mode

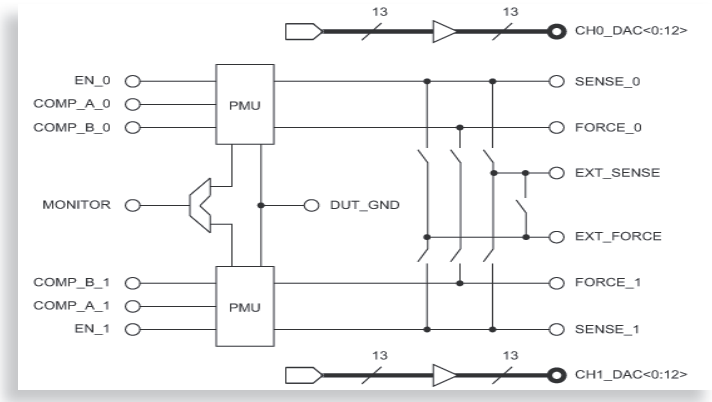
- On-Chip DC Levels
- All PMU Levels Generated On-Chip
- 13 Levels/Channel Brought Off-Chip
- 16 Bits per Level
- 16 Bit per Level Offset Correction
- 16 Bit per Level Gain Corrective

- Resistive Load
- 8 Resistance Options
- High-Speed Real Time Control

- External Force/Sense Switches On-Chip

- 3-Bit Serial Port

- Package/Power Dissipation
- 56 Lead 8mm x 8mm QFN with Exposed Heat Slug
- Pdmax ≤ 700mW/Channel; Pdmax≤1.4W/Chip (Maximum Output Current)
- 128 Lead, 14mm X 20mm, MQFP w/Heat Slug
- Pdq ≤ 500mW/Channel; Pdq ≤ 4.0W/Chip



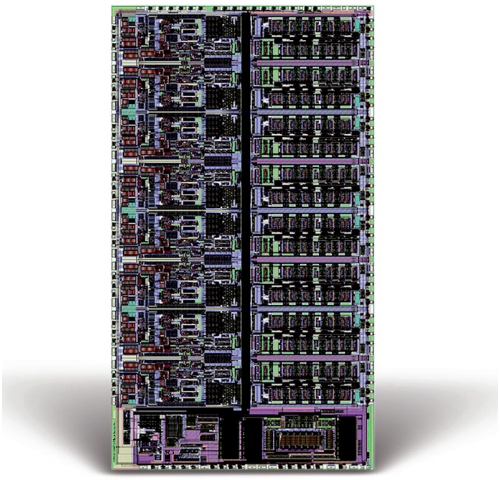
Pluto2-301N (Pluto2)

SOC Octal Integrated DPS/PMU/VI/Pin Electronics

Pluto2 is a highly-integrated SOC pin electronics solution incorporating eight independent channels of:

- DPS / PMU / VI
- Pin Electronics
- Resistive Load

The interface, control, and I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.



Features

- Per-Pin DPS / PMU
- FV, FI, MV, MI – 4 Quadrant Operation
  - 64 mA Imax in FV / MI
  - 32 mA Imax in FI / MV
- 8 Current Ranges
  - (32 mA, 8 mA, 2 mA, 512 µA, 128 µA, 32 µA, 8 µA, 2 µA)
  - 14V FV Range
- FI Voltage Clamps
- FV Current Clamps
- Per-Pin Monitor
- Central (Per-Chip) Monitor

- Per-Pin PMU
- 2 Level Driver w/ On Chip Buffers
- 14V Driver Output Swings
- 10 MHz Driver Operation
- 16V Comparator Input Voltage Range
- Extremely Low Input Leakage over a 16V Range

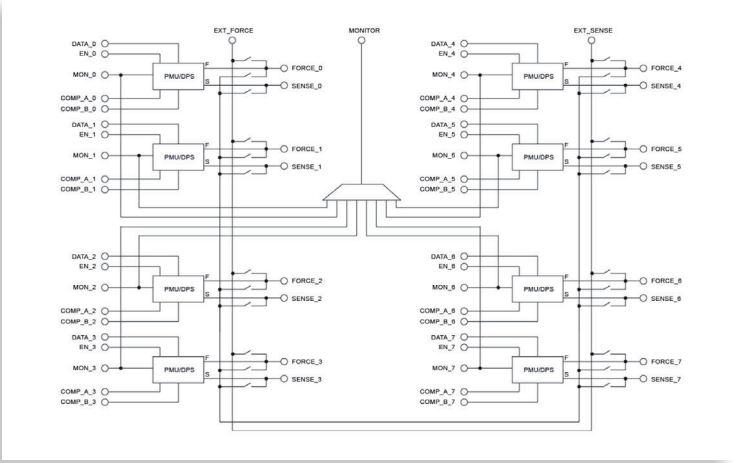
- Ganging Capability
- High current applications
- No limit on ganged Imax
- Gang control circuitry built in

- 3-Bit Serial CPU Port

- Pin Electronics Driver and Comparator
- Extremely Low Leakage over a 16V Input Range
- 16V Comparator Input Voltage Range

- DAC
- DC Level Generation
- 10 DC Levels per Channel (16 Bits / Level)
- On Chip Offset and Gain Correction
- Ability to shift voltage ranges up and down

- Package/Power Dissipation
- Lead Free
- 128 Lead, 14mm X 20mm, TQFP w/ Heat Slug
- Pdq ≤ 125mW/Channel; Pdq ≤ 1W/Chip
- On-Chip Thermal Monitor

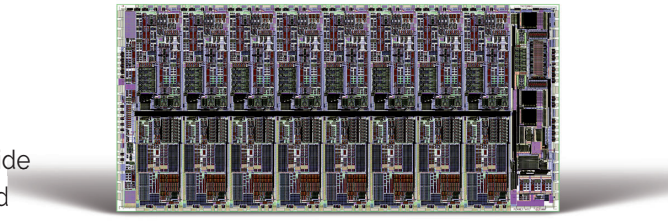


ISL55185 (Triton)

SOC Octal Wide-Voltage PMU/Load

Triton is a highly-integrated SOC pin electronics solution incorporating eight independent channels of:

- PMU
- Active load
- External force/external sense



The interface, control, and I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.

Features

- Per-Pin PMU
- FV/MI/MV
- 5 Current Ranges (24mA, 4mA, 400µA, 40µA, 4µA)
- FV Current Clamps
- 32V Input Compliance/28V Output Forcing Range
- Extremely Low Input Leakage over a 32V Range

- Per-Channel Active Load
- 24mA Maximum Current
- MI capability
- Independent Source and Sink Current Levels
- Extremely low Hi-Z Leakage over a 32V Range
- 32V Input Compliance/28V Output Forcing Range

- Monitor
- Differential Per Channel monitor with Hi-Z
- Differential Central Monito with Hi-Z

- External Force/Sense per Channel

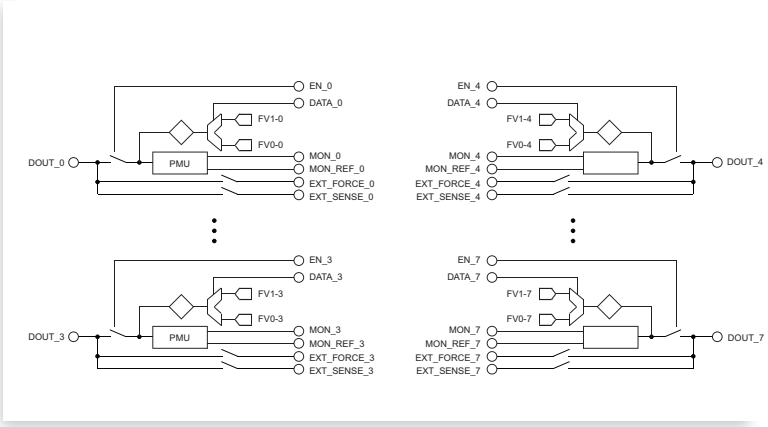
- 3-bit Serial Port

- DAC
- DC Level Generation
- 4 DC Levels Per Channel (16 bits/level)
- On-chip Offset and Gain Correction per Level

- Package / Power Dissipation
- 128 Lead, 14mm x 20mm LQFP w/Heat Slug
- Pdq ≤ 250mW/Channel; Pdq ≤ 2W/Chip

Applications

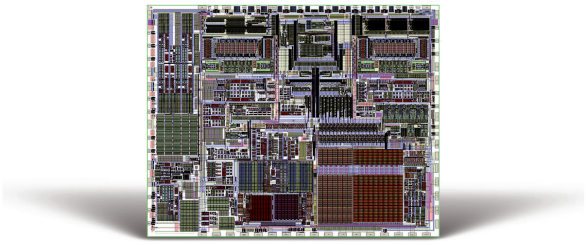
- Automated Test Equipment
- Instrumentation
- ASIC Verifier



Jupiter-314N (Jupiter)

SOC Gangable DPS

Jupiter is a highly-integrated SOC Device Under Test Power Supply (DPS) incorporating all analog and digital functionality required for a single DPS unit for Automatic Test Equipment. The interface, control, and I/O are digital; all analog circuitry is inside the chip. One chip constitutes one complete DPS.



Features

- 1A DC Output Drive Capability
- 6 Current Ranges
  - (1,024mA, 128mA, 8mA, 1mA, 125µA, 15.625µA)
- Glitchless Current Range Changing
- Hi-Z Capability w/ Extremely Low Leakage

- Full Functionality
- FV, FI, MV, MI
- 4 Quadrant Operation
- Bump function

- Ganging Capability for Higher Current Applications

- Integrated External Force and Sense Switches

- Independent Power Supply for Output Stage
- Operating Voltage
- 24V Supply Range
- Adjustable Output Range
- 4 Voltage Ranges (4V, 8V, 16V, 24V)
- Adjustable Slew Rate
- External Precision DAC Drive Capability

- Programmable Clamps
- Voltage Clamps
- Current Clamps

- Ultra Low Noise External DAC Mode

- Programmable Alarms
- Over Current
- Over Voltage
- Over Temperature
- Kelvin Sense

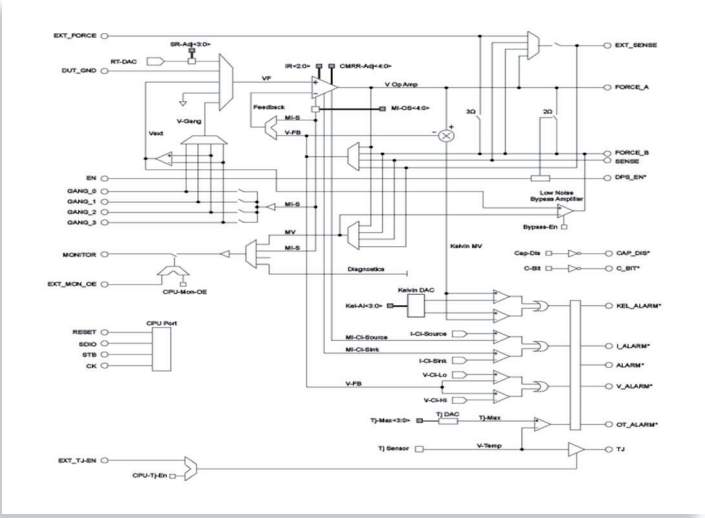
- Dedicated Real Time DAC for Forcing Level
- Increment / Decrement Option
- Linear / Binary Increment / Decrement Option
- 16 Bit per Level Offset & Gain Correction

- Global External Force/Sense Connectable to any Channel

- On-Chip DC Support Levels
- 16 Bits per Level
- 16 Bit per Level Offset & Gain Correction

- 3-Bit Serial CPU Port
- Load Internal Registers and Memory
- Read Back Internal States

- Package / Power Dissipation
- Lead Free
- 64 Lead, 10mm X 10mm, TQFP w/ Heat Slug
- Pdq (No Load) = 700mW to 1.5 Watt



ISL55180 (Europa)

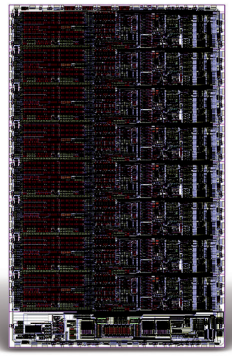
SOC Octal Integrated DPS

Europa is a highly-integrated SOC Device Under Test (DUT) power supply solution incorporating eight independent DUT Power Supply (DPS) units.

The interface, control, and I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-channel basis.

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. Real-time control is accomplished via the central EN and DATA_# pins. Real-time observation is accomplished via the central monitor.



Features

- Per-Channel DPS
- FV, FI, MV, MI, HiZ Capability
- 16V Measure Voltage Input Compliance Range
- 2 Force Voltage Ranges (8V, 16V)
- 3 Measure Voltage Ranges (4V, 8V, 16V)
- 6 Current Ranges: (256mA, 25.6mA, 2.56mA, 256µA,
- 25.6µA, 2.56µA)
- Programmable Current Clamps

- Power Management
- Independent Output Buffer Power Supply (VCCO)
- Ability to Exceed VCCO in Lower Current Ranges (Patent Pending)

- Flexible Ganging Capability
- No Restrictions on Maximum # DPS Units

- Protection
- On-Chip Junction Temperature Monitor
- Over-Temperature Shut Down per Chip
- Kelvin Connection Sensing/Alarm per Channel
- Over-Current Sensing/Alarm per Channel

- Global External Force/Sense Connectable to any Channel

- Monitor
- One General Purpose Central Monitor per Chip
  - Scaling and Shifting Capability
  - Hi-Z Capability
- One Dedicated Measure Current Monitor per Chip
  - Scaling and Shifting Capability
  - Hi-Z Capability

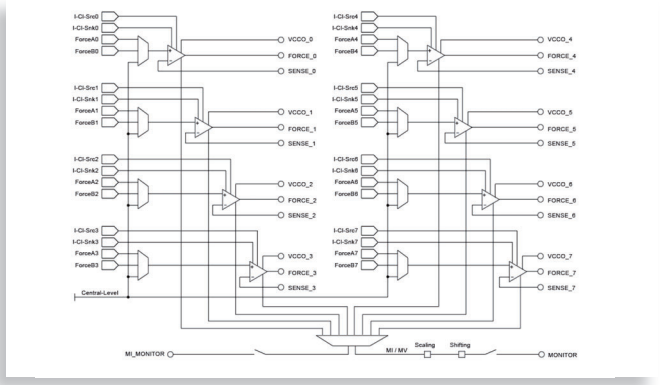
- 3-Bit Serial CPU Port

- DAC
- DC Level Generation
- 2 Independent FV Levels/Channel
- Central Resource Mode w/16 Selectable Levels
- Independent Source and Sink Clamp Levels/Channel
- 16 bits/Level
- On-Chip Offset and Gain Correction per Level

- Package/Power Dissipation
- Pb-Free (RoHS Compliant)
- 128 Lead, 14mm x 20mm, TQFP w/Exposed Heat Slug
- Pdq ≤ 100mW/Channel; Pdq ≤ 800mW/Chip

Applications

- Automated Test Equipment
- Instrumentation
- Logic/ASIC Verifier



ELE58VE2A (Vesuvius)

SOC Octal Integrated DPS

Vesuvius is a highly-integrated SOC Device Under Test (DUT) power supply solution incorporating eight independent DUT Power Supply (DPS) units.

The interface, control, and I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-channel basis. All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test. An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. Real-time control is accomplished via the central EN and DATA_# pins. Real-time observation is accomplished via the central monitor.

Features

- Per-Channel DPS
- FV, FI, MV, MI, HiZ Capability
- 16V Measure Voltage Input Compliance Range
- 2 Force Voltage Ranges (8V, 16V)
- 3 Measure Voltage Ranges (4V, 8V, 16V)
- 6 Current Ranges: (512mA, 25.6mA, 2.56mA, 256µA, 25.6µA, 2.56µA)
- Programmable Voltage and Current Clamps

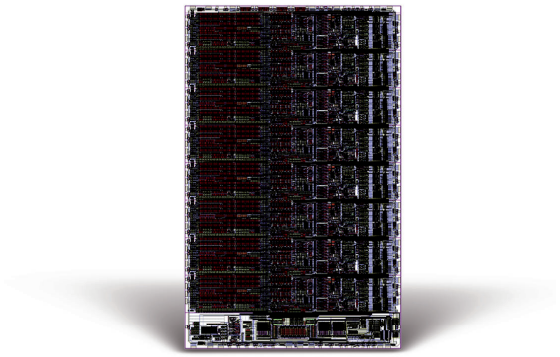
- Power Management
- Independent Output Buffer Power Supply (VCCO)
- Ability to Exceed VCCO in Lower Current Ranges

- Flexible Ganging Capability
- No Restrictions on Maximum # DPS Units

- Protection
- On-Chip Junction Temperature Monitor
- Over-Temperature Shut Down per Chip
- Kelvin Connection Sensing/Alarm per Channel
- Over-Current Sensing/Alarm per Channel

- Global External Force/Sense Connectable to any Channel

- Monitor
- One General Purpose Central Monitor per Chip
  - Scaling and Shifting Capability
  - Hi-Z Capability
- One Dedicated Measure Current Monitor per Chip
  - Scaling and Shifting Capability
  - Hi-Z Capability
- Eight Independent V/I Monitors Per Chip
  - Maximum Measurement Throughput



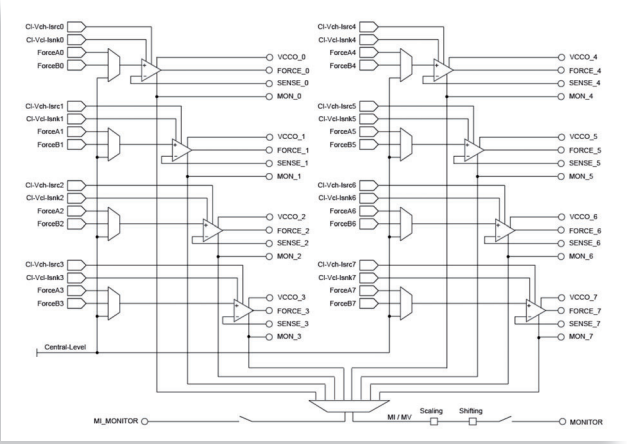
- 3-Bit Serial CPU Port

- DAC
- DC Level Generation
- 2 Independent FV Levels/Channel
- Central Resource Mode w/16 Selectable Levels
- Independent Source and Sink Clamp Levels/Channel
- 16 bits/Level
- On-Chip Offset and Gain Correction per Level

- Package/Power Dissipation
- Pb-Free (RoHS Compliant)
- 128 Lead, 14mm x 20mm, TQFP w/Exposed Heat Slug
- Pdq ≤ 115mW/Channel; Pdq ≤ 920mW/Chip

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifier

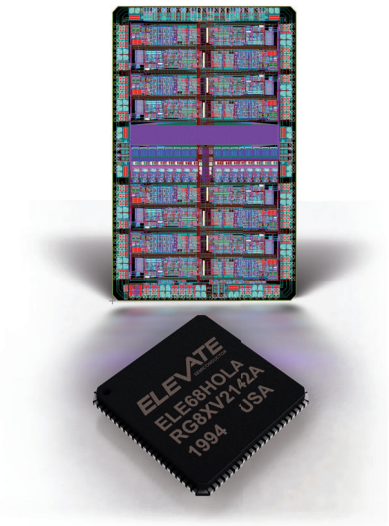


ELE58HOA (Hood)

SOC Octal High-Density PPMU

Hood is a highly-integrated System-on-a-Chip (SoC) PPMU solution incorporating eight independent channels of PMU.

The interface and control are digital. All analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.



Features

- Per-Pin PMU
- FV, FI, MV, MI
- 4 Quadrant Operation
- –2V to 6.5V FV/MV Range
- 6 Current Ranges (±2µA, ±20µA, ±200µA, ±2mA, ±15mA, ±50mA)
- Programmable Voltage and Current Clamps
- Resistive Load Function (12 Selectable Resistor Values)
- Reduced Glitch Current Range Changing

- Protection
- On-Chip Junction Temperature Monitor
- Over-Temperature Shutdown Per-Chip

- Global External FORCE/SENSE Connectable to any Channel

- Remote Sense from Adjacent Channel

- 100MHz SPI Interface

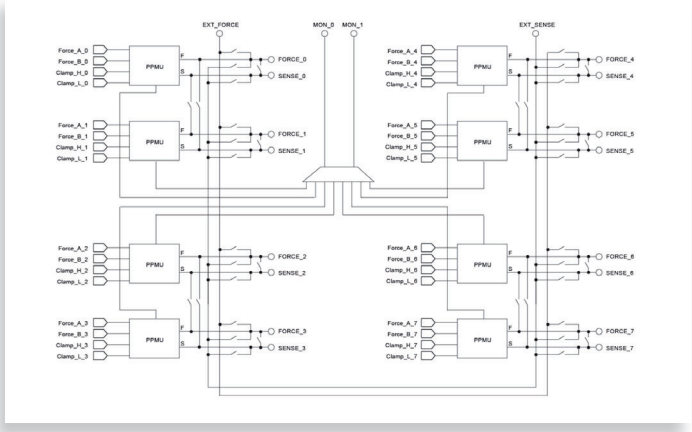
- On-Chip Independent DACs to Generate DC Levels
- 6 DC Levels per Channel
  - 2 Levels for Forcing Function
  - 2Levels for Voltage Clamps
  - 2 Levels for Current Clamps
  - On-Chip Offset Correction

- Monitor
- Two MV/MI Monitors (one for each 4 channels)
- Ability to Route any Channel to Either Monitor
- On-Chip Signal Preconditioning (Optimized for Direct Connection to AD7609B)

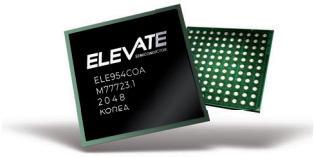
- Package/Power Dissipation
- 88 Pad, 10mm x 10mm MLF
- Pdq ≤ 150mW/Channel
- Pstandby ≤ 75mW/Channel

Applications

- Automated Test Equipment
- Instrumentation



ELEVATE
SEMICONDUCTOR



Powering the Next Generation of Semiconductor Test