

PRODUCT SELECTION GUIDE

Integrated Components for Automated Test Equipment



Mystery

SOC Octal 500 MHz Integrated Pin
Electronics

Powering the Next Generation of Semiconductor Test

Integrated Components for Automated Test Equipment

- Integrated Pin Electronics
- Integrated DUT Power Supplies
- Integrated V/I and PPMU
- High Current Pin Drivers



At Elevate, we know firsthand how fast the semiconductor market is changing. New, self-driving vehicles, safety systems requiring 3 to 5x the intelligence of previous generations, artificial intelligence systems being deployed in more and more applications all spell the same thing for the future of semiconductor test: evolutionary change just won't cut it; revolutionary change is required! We design state-of-the-art products, utilizing technology that allows for the highest density in the industry - built for the requirements of the next 20 years, not the last 20.

Elevate is a leading supplier of innovative, lower power, high density components for the design of next generation Automated Test Equipment (ATE). With a proven track record of consistently delivering the highest density, lowest power solutions available, systems designed around Elevate products have a competitive advantage in the ATE market space and are able to adapt successfully to emerging trends and challenges while providing ever increasing end user value.



David J. Kenyon, CEO and President

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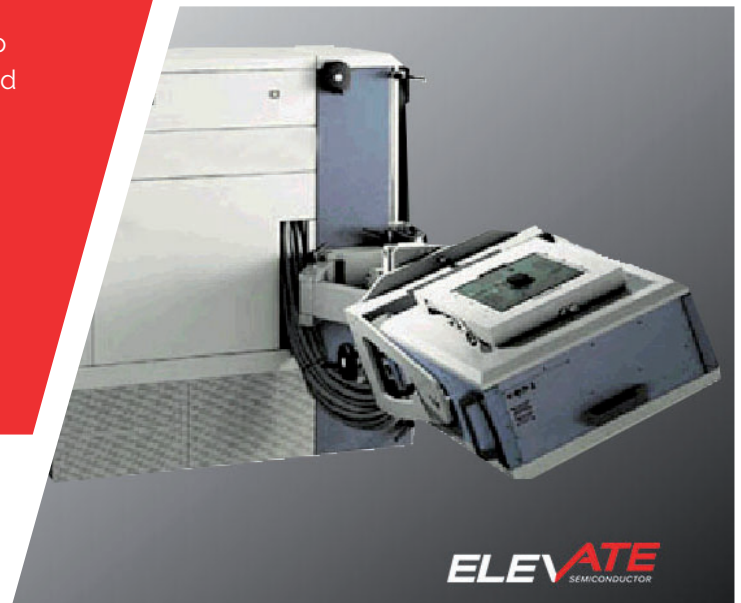


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Integrated Digital Pin Electronics

Elevate is the market leader in low power, high density integrated pin electronics. Developed in a pure CMOS technology, our products enable customers to develop next generation high density instruments with increased parallelism for reduced cost of test and improved system reliability. Integrated timing delay, or "Deskew", circuitry comes standard on our integrated pin electronics products and enables flexible timing control and edge placement in a system without the need for an expensive ASIC. Packed with system level features, these products greatly simplify the design of ATE systems for improved time to market.



ATE Manufacturer Solutions

ATE Manufacturer Solution Channel Controller

- Pattern Generator
- Timing Generator
- Format Section
- Error Section
- All Other Blocks

ElevATE Solutions

- Pin Electronics
- Deskew
- PPMU
- DACs
- Digital Support Functions

A large red arrow pointing to the right, containing the text "DUT" in a white box. The arrow is part of a flow diagram showing the integration of ATE Manufacturer Solution Channel Controller and ElevATE Solutions into a Device Under Test (DUT).

DUT

Integrated Digital Pin Electronics Table

| Product | | ELE18MY1 (Mystery) | ISL55164 (Venus) | ISL55162 (Venus3) | ISL55161 (Venus4) | ISL55163 (Venus4 Lite) | ISL55169 (Mercury) | ISL55188 (Saturn) | ELE22KI2A (Kilimanjaro) |
|-----------------|-------------|--------------------------------------|------------------------------|------------------------------|---|---|------------------------------|---------------------------------|-----------------------------|
| Overview | Description | P/E + DAC + PPMU + Deskew + Load | P/E + PMU + DAC + Deskew | P/E + PMU + DAC + Deskew | P/E + PMU + Load + DAC + Deskew | P/E + PMU + Load + DAC | P/E + PMU + DAC + Deskew | P/E + PMU + DAC + Deskew + Load | Pin Driver + Window Comp |
| | Status | Production | Production | Production | Production | Production | Production | Production | Production |
| | # Channels | 8 | 2 | 2 | 2 | 2 | 8 | 2 | 2 |
| | Package | 14 x 14 144 Ball FcBGA (1.0mm Pitch) | 10x10 TQFP w/exposed slug up | 10x10 TQFP w/exposed slug up | 10x10 TQFP w/exposed slug up 9x9 QFN (Top Exposed Paddle) | 10x10 TQFP w/exposed slug up 9x9 QFN (Top Exposed Paddle) | 14x20 TQFP w/exposed slug up | 14x20 TQFP w/exposed slug up | 5x5 QFN w/exposed slug down |
| | Pdq | 700mW/Channel | 750mW/Channel | 1W/Channel | 600mW/Channel | 600mW/Channel | 350mW/Channel | 1.5W/Channel | 125mW/Channel |
| Pin Electronics | Fmax | 500MHz | 133MHz | 300MHz | 400MHz | 400MHz | 66MHz | 75MHz | 100MHz |
| | Driver | Dual Mode 3-level Driver | 3 Level/8V | 3 Level/8V | 3 Level/8V | 3 Level/8V | 2 Level/8V | 2 Level/24V | 2 Level/15V |
| | Comparator | 8V | 16V | 16V | 16V | 16V | 16V | 32V | 15V |
| | Load | Active, ± 24mA | Resistive | Resistive | Active, ± 24mA | Active, ± 24mA | | Active, ± 24mA | |
| | DC Levels | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | Off-Chip |
| PMU | PMU | 1/Channel | 1/Channel | 1/Channel | 1/Channel | 1/Channel | 1/Chip | 1/Channel | |
| | DC Levels | On chip | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | |
| | Imax | 50mA | 32mA | 32mA | 32mA | 32mA | 32mA | 200mA | |
| Deskew | Delay | 7ns | 8ns - 20ns | 6.4ns - 12.8ns | 3.2ns - 5.0ns | | 10ns - 20ns | 10ns - 20ns | |
| | FEA | ±50ps to 50ps | ±25% of Delay | ±12.5% of Delay | ±50% of Delay | | ±25% of Delay | ±25% of Delay | |
| | Resolution | 10ps | 15ps - 37.5ps | 12ps - 25ps | 12ps - 20ps | | 312.5ps - 625ps | 312.5ps - 625ps | |
| Part No. | | ELE18MY1-FCT01 | ISL55164CNEZ | ISL55162CNEZ | ISL55161CNEZ | ISL55163CNEZ | ISL55169CNEZ | ISL55188CNEZ | ELE22KI2A-RBJ01 |

ELE18MY1 (Mystery)

SOC Octal 500MHz Integrated Pin Electronics/DAC/PPMU/DESKEW

ELEVATE
SEMICONDUCTOR

The Mystery is a highly integrated SOC pin electronics solution that incorporates every analog function, along with digital support circuitry required to create 8 independent pin channels for Automated Test Equipment. Each channel is configured via a 100MHz SPI interface, and all real time data is programmed and read back through high speed FLEX I/O pins that can be configured to interface directly to other devices using multiple single-ended and differential logic families.

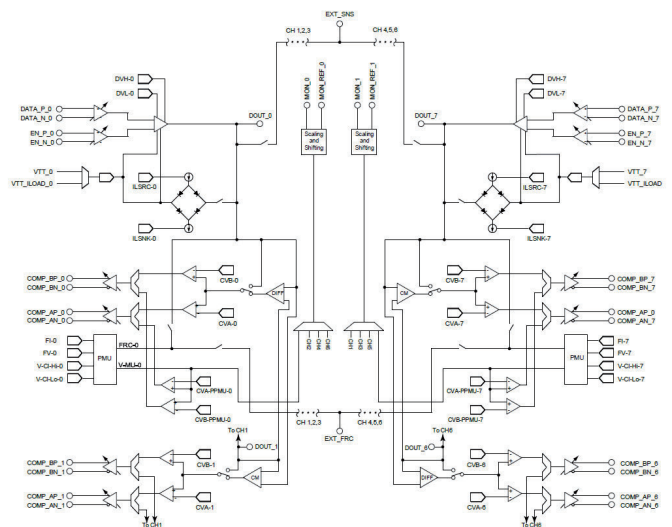
Features

- **Pin Electronics Driver/Comparator**
 - Dual Mode 3-level Driver with Hi-Z Capability (DVH, DVL, VTT)
 - HV (High Voltage) Driver Mode
 - 25mV to 8V Swing Across -2V to +6V Range
 - Programmable Driver Slew Rate
 - HS (High Speed) Driver Mode
 - 25mV to 4V Swing Across 0V to +4V Range
 - Up to 8V Comparator Input Range
 - 1GHz Comparator Equivalent Bandwidth
 - Extremely Low Hi-Z Leakage over Entire I/O Range
 - Short Circuit Protection
- **Per Pin PMU (PPMU)**
 - FV, FI, MV, MI
 - 4 Quadrant Operation
 - -2V to +6V FV/MV Range
 - 5 Current Ranges ($\pm 2\mu\text{A}$, $\pm 20\mu\text{A}$, $\pm 200\mu\text{A}$, $\pm 2\text{mA}$, $\pm 50\text{mA}$)
 - Programmable Voltage and Current Clamps
 - Resistive Load Function (12 Selectable Resistor Values)
- **Per Pin Active Load**
 - +/- 24mA Maximum Current
 - Independently Programmable Current Source, Current Sink, and Commutating Voltage levels
- **Per Pin Timing Deskew**
 - Propagation Delay Adjustment
 - 7ns Delay Adjustment Range
 - 10ps Delay Adjustment Resolution
- **On-Chip DC Levels**
 - 17 True DAC Levels per Channel (not Sample and Hold)
 - Per Level Offset Correction
 - 16-bit Resolution/14-bit Accuracy
 - DUT Ground Sensing and Correction (1 Per Chip)

- **100MHz SPI Interface**
- **High Speed FLEX I/O**
- **Analog Measure Bus**
- **Extremely Small PCB Footprint**
 - 14mm x 14mm, 144 Ball FcBGA (1.0mm Pitch)
- **Pmax < 700mW per Channel**

Applications

- **Automated Test Equipment**
- **Instrumentation**
- **ASIC Verifier**

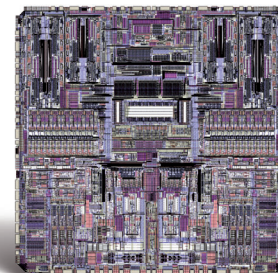


ISL55161 (Venus4)

SOC Dual Channel 400MHz Pin Electronics Driver/Comparator/Active Load/Timing Deskew/PPMU/DACs

ELEVATE
SEMICONDUCTOR

The ISL55161 is a highly integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each ISL55161. The ISL55161 is pin and functionally compatible with Venus4.



Features

- Pin Electronics Driver/Comparator

- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings
- Extremely Low HiZ Leakage over 16V Range
- Differential Driver and Comparator Modes
- 16V Comparator Input Compliance Range

- Load

- 24mA I_{max}
- 16V Input Compliance Range
- Extremely Low HiZ Leakage over 16V Range
- Independent Power-down Option

- Deskew

- Propagation Delay Adjustment
- Falling Edge Adjustment

- PMU

- FV, FI, MV, MI
- FI Voltage Clamps
- Eight current Ranges (32mA, 8mA, 2mA, 512μA, 128μA, 32μA, 8μA, 2μA)
- Resistive Load (eight selectable resistor values)
- Remote Sense Option

- On-Chip DC Levels

- 13 Levels/Channel
- Gain and Offset Correction/Level
- DUT Ground Sensing and Corrections

- Flexible High Speed Digital Inputs and Outputs

- Selectable On-chip Terminations for Inputs
- Read-back Internal States

- Package/Power Dissipation

- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pd_q ≤ 500mW/Channel @ 11V Operation

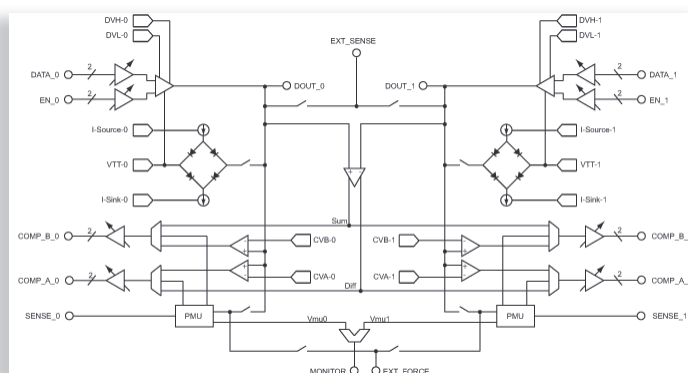
Applications

- Automated Test Equipment

- Instrumentation

- ASIC Verifier

Highly Integrated System-on-a-Chip Solutions with 9mm x 9mm OR 10mm x 10mm Footprint



ISL55163 (Venus4 Lite)

SOC Dual Channel 400MHz Pin Electronics Driver/Comparator/Active Load/PPMU/DACs

ELEVATE
SEMICONDUCTOR

The ISL55163 is a highly integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each ISL55163. The ISL55163 is pin compatible with Venus4.

Features

- Pin Electronics Driver/Comparator

- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings
- Extremely Low HiZ Leakage over 16V Range
- Differential Driver and Comparator Modes
- 16V Comparator Input Compliance Range

- Load

- 24mA I_{max}
- 16V Input Compliance Range
- Extremely Low HiZ Leakage over 16V Range
- Independent Power-down Option

- PMU

- FV, FI, MV, MI
- FI Voltage Clamps
- Eight current Ranges (32mA, 8mA, 2mA, 512μA, 128μA, 32μA, 8μA, 2μA)
- Resistive Load (eight selectable resistor values)
- Remote Sense Option

- On-Chip DC Levels

- 13 Levels/Channel
- Gain and Offset Correction/Level
- DUT Ground Sensing and Correction

- Flexible High Speed Digital Inputs and Outputs

- Selectable On-chip Terminations for Inputs
- Read-back Internal States

- Package/Power Dissipation

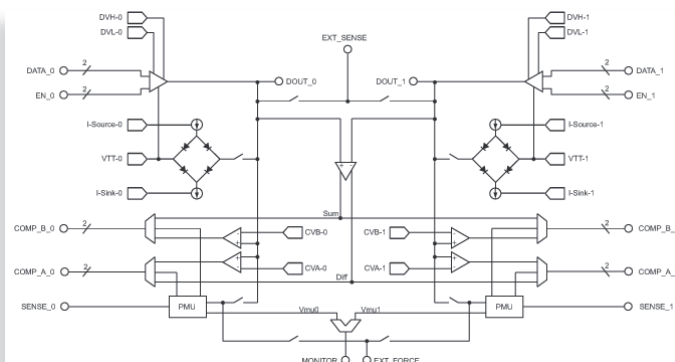
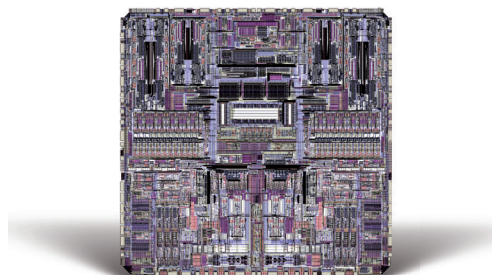
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- 64-Lead, 9mm x 9mm QFN with Top Exposed Heat Slug
- Pd_q ≤ 500mW/Channel

Applications

- Automated Test Equipment

- Instrumentation

- ASIC Verifier

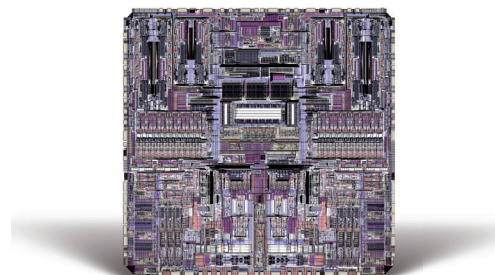


ISL55162 (Venus3)

SOC Dual Channel 300MHz Pin Electronics Driver/Comparator/PPMU/
Timing Deskew/DAC

ELEVATE
SEMICONDUCTOR

The ISL55162 is a highly integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support circuitry, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each chip. ISL55162 is pin and functionally compatible with Venus, Venus Plus and Venus2.



Features

- Pin Electronics Driver/Comparator

- 3-level Driver (DVH/DVL/VTT)
- 8V Driver Output Swings
- 16V Comparator Input Compliance Range
- Extremely Low HiZ Leakage over 16V Range

- Per Pin PMU

- FV, FI, MV, MI
- 8 Current Ranges (32mA, 8mA, 2mA, 512μA, 128μA, 32μA, 8μA, 2μA)
- 4 Quadrant Operation
- +13V Super Voltage Capability
- FI Voltage Clamps
- Resistive Load (8 selectable resistor values)

- Deskew

- Propagation Delay Adjustment
- Falling Edge Adjustment
- Delay Rangeset by PLL Clock

- On-Chip DC Levels

- 11 Levels/Pin
- Gain and Offset Correction /Level
- DUT Ground Sensing and correction

- 3-Bit Serial CPU Port

- Flexible High Speed Digital Inputs and Outputs

- Selectable On-Chip Terminations for Inputs
- 50Ω Series Termination for Comparator Outputs

- Lead Free Package

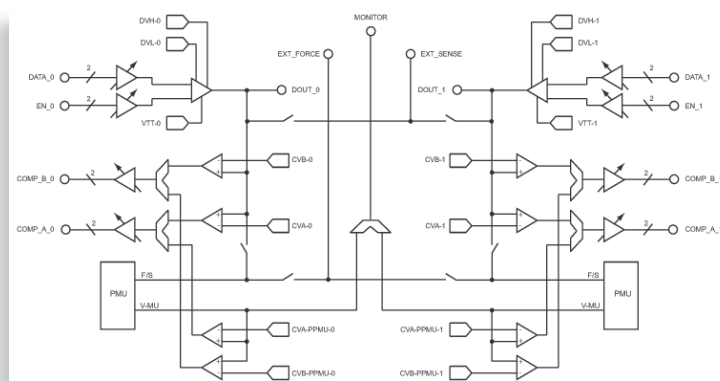
- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- Pdq < 1.1W/Channel

Applications

- Automated Test Equipment

- Instrumentation

- ASIC Verifier

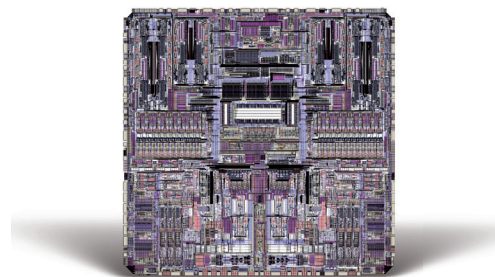


ISL55164 (Venus)

SOC Dual Channel 133MHz Pin Electronics Driver/Comparator/PPMU/
Timing Deskew/DACs

ELEVATE
SEMICONDUCTOR

The ISL55164 is a highly integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each ISL55164. The ISL55164 is pin and functionally compatible with Venus.



Features

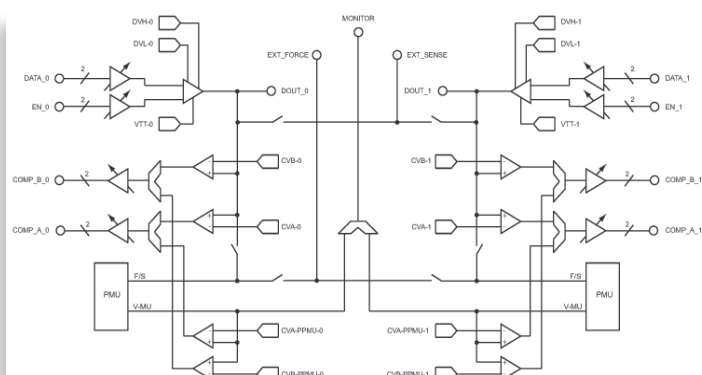
- **133MHz**
- **3.75ns Minimum Pulse Width**
- **Pin Electronics Driver/Comparator**
 - 3-level Driver (DVH/DVL/VTT)
 - 8V Driver Output Swings
 - 16V Comparator Input Compliance Range
 - Extremely Low HiZ Leakage over 16V Range
- **Per Pin PMU**
 - FV, FI, MV, MI
 - 8 Current Ranges (32mA, 8mA, 2mA, 512μA, 128μA, 32μA, 8μA, 2μA)
 - +12V Super Voltage Capability
 - Resistive Load (8 selectable resistor values)
- **Deskew**
 - Propagation Delay Adjustment (up to 12.8ns range)
 - Falling Edge Adjustment (up to ±3.2ns range)
 - Auto Calibration via PLL
- **On-Chip DC Levels**
 - 11 Levels/Channel
 - Gain and Offset /Level
 - DUT Ground Sensing/Pin
- **Flexible High Speed Digital Inputs and Outputs**
- **3-Bit Serial CPU Port**
 - Load Internal Registers and Memory
 - Read Back Internal States
 - Selectable On-chip Terminations for High Speed Inputs
 - 50Ω Series Terminated High Speed for Comparator Outputs

- Package/Power Dissipation

- 64-Lead, 10mm x 10mm TQFP with Top Exposed Heat Slug
- $Pd_q \leq 1.10W/Channel$; $Pd_q \leq 2.2W/Chip$

Applications

- **Automated Test Equipment**
- **Instrumentation**
- **ASIC Verifier**

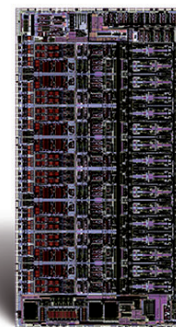


ISL5516g (Mercury)

System on a Chip, 66 MHz Octal Pin Electronics Driver/
Comparator/Timing Deskew w/Shared PMU

ELEVATE
SEMICONDUCTOR

ISL5516g is a highly integrated SOC pin electronics solution aimed at incorporating every analog function (with some digital support functionality) required on a per channel basis for Automated Test Equipment (see figure below.) The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.



ELEVATE
SEMICONDUCTOR

Features

- 66 MHz

- 7.5 ns Minimum Pulse Width

- Pin Electronics Driver

- 2 Level Driver w/ On Chip Buffers
- 8V Driver Output Swings
- Extremely Low Leakage over a 16V HiZ Range

- Pin Electronics Comparator

- Extremely Low Leakage over a 16V Input Range
- 16V Comparator Input Voltage Range

- Per-Chip PMU

- FV, FI, MV, MI
- 8 Current Ranges (32 mA, 8 mA, 2 mA, 512 μ A, 128 μ A, 32 μ A, 8 μ A, 2 μ A)
- 12V Super Voltage Capability

- Deskew

- Propagation Delay Adjustment (up to 20 ns range)
- Falling Edge Adjustment (up to ± 5 ns range)
- Auto Calibration via PLL

- On-Chip DC Levels

- 4 Levels / Channel
- 8 Levels / Central PMU
- 16 Bits per Level
- 16 Bit per Level Offset Correction
- 16 Bit per level Gain Correction

- Flexible High Speed Digital Inputs and Outputs

- 50 Ω Series Terminations High Speed for Comparator Outputs
- Selectable On-Chip Terminations for High Speed Inputs

- 3-Bit Serial CPU Port

- Load Internal Registers and Memory
- Read Back Internal States
- Selectable On-chip Terminations for High Speed Inputs
- 50 Ω Series Terminated High Speed for Comparator Outputs

- Package/Power Dissipation

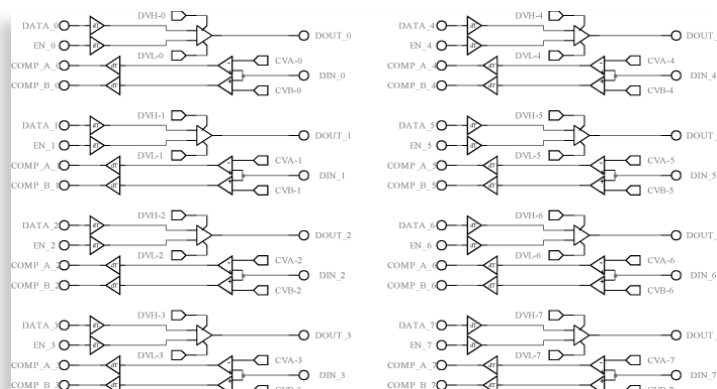
- 128 Lead, 14 mm X 20 mm, TQFP w/ Heat Slug
- Pd_q \leq 500 mW / Channel; Pd_q \leq 4.0W / Chip

Applications

- Automated Test Equipment

- Instrumentation

- ASIC Verifier

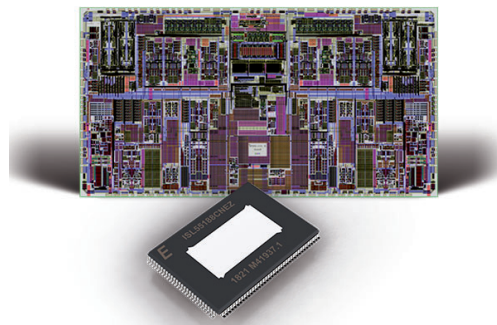


ISL55188 (Saturn)

SOC, Dual Channel Wide Voltage Pin Electronics Solution

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The ISL55188 is a highly integrated SOC pin electronics solution aimed at incorporating every analog function, along with some digital support functionality, required on a per channel basis for Automated Test Equipment. The interface, control and I/O of the chip are all digital; all analog circuitry is inside the chip. Two complete tester channels are integrated into each ISL55188



Features

- Pin Electronics Driver

- 75 MHz Fmax
- 2 Level Driver (DVH / DVL)
- DC Level Generators On Chip
- 24V Driver Output Swings
- Adjustable Output Voltage Range (-15V to +24V)
- Programmable Slew Rates (1 V/ns to 0.1 V/ns)
- Iout = 200 mA (DC)
- Extremely Low Leakage Over the operating Range

- Pin Electronics Comparator

- Threshold Level Generators On Chip
- Extremely Low Leakage over a 32V Range
- 32V Comparator Input Compliance Range
- Differential Comparator

- Deskew

- Propagation Delay Adjustment
- Falling Edge Adjustment
- Delay Range set by PLL Clock

- PMU

- 5 Current Ranges
- (20 μ A, 200 μ A, 2 mA, 20 mA, 200 mA)
- FV / MI
- FI / MV
- Imax = 200 mA

- On-Chip DC Levels

- 10 Levels / Channel; 16-Bit Levels
- 16-Bit Gain and 16-Bit Offset Correction / Level
- DUT Ground Sensing and Correction

- 3-Bit Serial CPU Port

- 2 Control Bits per Channel (for Ext Relay Support)

- Flexible Real Time Digital Inputs and Outputs

- 50 Ω Series Terminations for Comparator Outputs
- Selectable On-Chip Terminations for Inputs

- Package

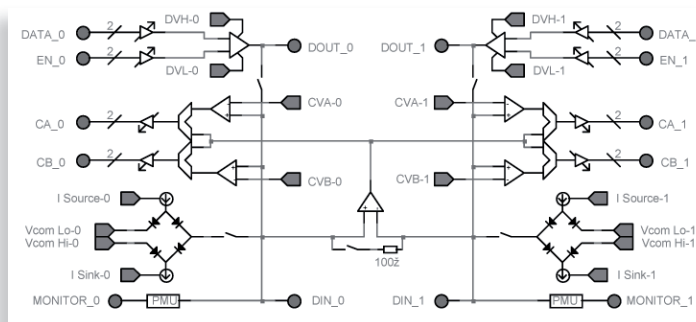
- Lead Free
- 128 Lead, 14 mm X 20 mm, TQFP w/ Heat Slug
- Pdq < 1.5 Watts / Channel; Pdq < 3.0 Watts / Chip
-

Applications

- Automated Test Equipment

- Instrumentation

- ASIC Verifier



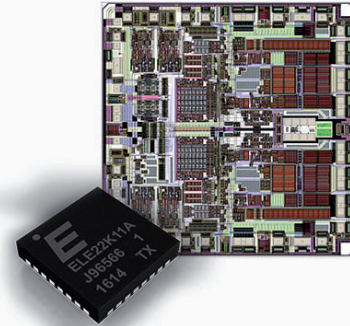
ELE22Kl2A (Kilimanjaro)

Low Cost, Dual Channel, 15V Pin Electronic Driver/Window Comparator

ELEVATE
SEMICONDUCTOR

The Kilimanjaro is a dual-channel pin electronics driver and window comparator product fabricated in a wide voltage Bi-CMOS process. It is designed specifically for Test During Burn-In (TDBI) applications and low cost testers, where cost, functional density, and power are all at a premium.

The Kilimanjaro incorporates two channels of programmable drivers and window comparators into a small 5mm x 5mm QFN package. Each channel has per pin driver levels, data, and high impedance control, along with per-pin high and low window comparator thresholds levels.



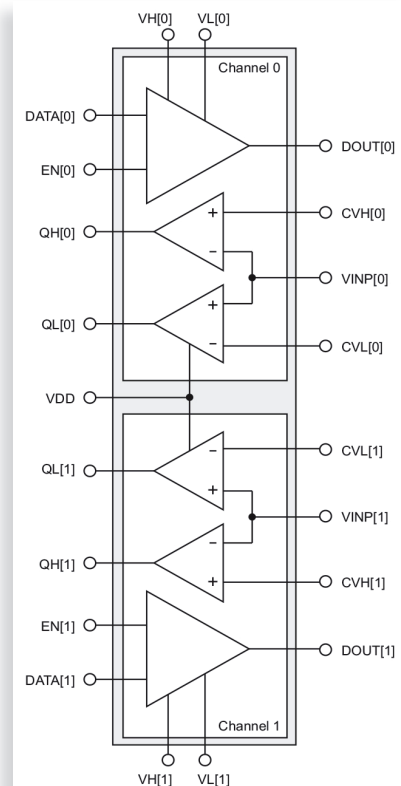
ELEVATE
SEMICONDUCTOR

Features

- 15V I/O Range
- 125mA DC Current Capability
- Low Output Impedance
- 100MHz Operation
- Driver Short Circuit Protection
- Per-Pin Flexibility
- Programmable Input Thresholds
- LVTTTL Compatible I/O
- Small Footprint (5mm x 5mm QFN with Exposed Heat Slug)
- Improved Small Signal Swing and Timing Performance
- Low Preshoot/Overshoot/Undershoot
- Pin and Functionally Compatible with E7801 and E7802

Applications

- Automated Test Equipment
- Instrumentation
- ASIC Verifier



Integrated PMU, DPS and V/I



Integrated PMU, DPS and V/I Products

ElevATE is the market leader in integrated PMU, V/I, and DPS products. We have leveraged our knowledge and expertise in system-on-a-chip solutions to offer the widest product portfolio available in this space. As a pioneer in the integrated analog pin space, we have developed products with the most advanced features in the industry. These features include ground-breaking advances in technology like glitch-free current measurement range changing, programmable pole and zero placement, less than 0.5V force amp headroom for improved system efficiency, and "ESP", a method to double the DPS density of existing systems. With a myriad of fully integrated, scalable, and digitally reconfigurable solutions available, we are confident that you will find a solution for your testing challenges.



ATE Manufacturer Solutions

ElevATE Solutions

- DUT Power Supply
- DACs
- External Force and Sense Switches
- Overcurrent protection

DUT

Integrated PMU, DPS and V/I



Integrated PMU, DPS and V/I Table

| Product | | ISL55187 (Neptune Plus) | Pluto2 | ISL55185 (Triton) | Jupiter | ISL55180 (Europa) | ELE58VE2A (Vesuvius) | ELE58HOA (Hood) |
|-------------|------------------|---------------------------------------|--|----------------------------------|----------------------------------|----------------------------------|-----------------------------------|----------------------------------|
| Overview | Description | Integrated PMU + Companion DAC Levels | Integrated PMU + 10MHz Pin Electronics | Integrated V/I | Integrated DPS | Integrated DPS | Integrated DPS | Integrated PMU |
| | Status | Production | Production | Production | Production | Production | Production | Pre-Production |
| | # Channels | 2 | 8 | 8 | 1 | 8 | 8 | 8 |
| | Package | 8x8 QFN w/ exposed slug down | 14x20 TQFP w/ exposed slug up | 14x20 TQFP w/ exposed slug up | 10x10 TQFP w/ exposed slug up | 14x20 TQFP w/ exposed slug up | 14x20 TQFP w/ exposed slug up | 8X8 MLF w/ex- posed slug down |
| | Pdq | 300mW/Channel | 125mW/Channel | 350mW/Channel | 1W/Channel | 100mW/Channel | 115mW/Chan- nel | 150mW/Channel |
| Details | Architecture | Traditional | Traditional | Traditional | Glitch-Free | Glitch-Free | Glitch-Free | Traditional |
| | DC Levels | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip | On-Chip |
| | I _{max} | 64mA Gangable | 64mA Gangable | 24mA | 1A Gangable | 256mA Infinitely Gangable | 512mA Infinitely Gang- able | 50mA |
| | FV Range | 14V | 14V | 28V | 26V | 14V | 14V | 8V |
| Part Number | | ISL55187CRZ | PLUTO2 | ISL55185CNEZ | JUPITER-314N | ISL55180CNEZ | ELE58VE2A-NEJ01 | ELE58HOA-RBT01 |

ISL55187 (Neptune)

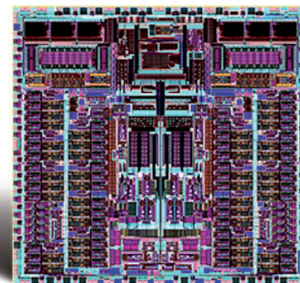
SOC Dual Channel, Pin Electronics Companion PMU/DAC Resistive Load

ELEVATE
SEMICONDUCTOR

The ISL55187 (Neptune Plus) is a highly integrated SOC pin electronics support solution incorporating two independent channels of:

- PMU
- DC Levels for the Pin Electronics
- Resistive Load

The interface, the control, and the I/O are digital. All analog circuitry is inside the chip. Two complete and independent channels are integrated into each chip. For most tester applications, except for the pin electronics, no additional analog hardware is required on a per pin basis.



Features

- Per Pin PMU

- FV, FI, MV, MI
- 8 Current Ranges (32mA, 8mA, 2mA, 512μA, 128μA, 32μA, 8μA, 2μA)
- FI Voltage Clamps
- FV Current Clamps
- On-Chip Current Ganging
- Supports 64mA/Channel in FV Mode

- On-Chip DC Levels

- All PMU Levels Generated On-Chip
- 13 Levels/Channel Brought Off-Chip
- 16 Bits per Level
- 16 Bit per Level Offset Correction
- 16 Bit per Level Gain Corrective

- Resistive Load

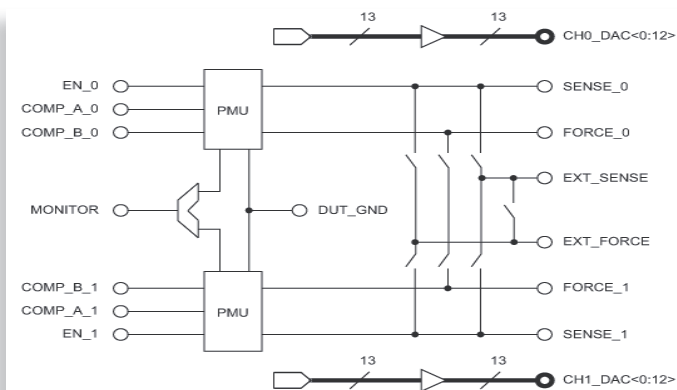
- 8 Resistance Options
- High Speed Real Time Control

- External Force/Sense Switches On-Chip

- 3-Bit Serial Port

- Package/Power Dissipation

- 56 Lead 8mm x 8mm QFN with Exposed Heat Slug
- $Pd_q \leq 343mW/channel$; $Pd_q \leq 685mW/Chip$ (No Output Current)
- $Pd_{max} \leq 700mW/Channel/Pd_{max} \leq 1.4W/Chip$ (Maximum Output Current)
- 128 Lead, 14 mm X 20 mm, MQFP w/ Heat Slug
- $Pd_q \leq 500 mW / Channel$; $Pd_q \leq 4.0W / Chip$



Pluto2

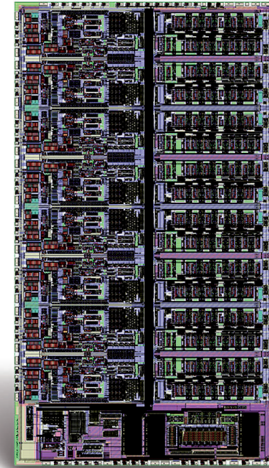
SOC Octal DPS/PMU/VI with Ganging 10Mhz Pin Electronics

ELEVATE
SEMICONDUCTOR

Pluto2 is a highly integrated SOC pin electronics solution incorporating 8 independent channels of:

- DPS / PMU / VI
- Pin Electronics
- Resistive Load

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip. For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.



Features

- Per Pin DPS / PMU

- FV, FI, MV, MI – 4 Quadrant Operation
 - 64 mA I_{max} in FV / MI
 - 32 mA I_{max} in FI / MV
- 8 Current Ranges
 - (32 mA, 8 mA, 2 mA, 512 μ A, 128 μ A, 32 μ A, 8 μ A, 2 μ A)
 - 14V FV Range
- FI Voltage Clamps
- FV Current Clamps
- Per Pin Monitor
- Central (Per Chip) Monitor

- Pin Electronics Driver and Comparator

- Extremely Low Leakage over a 16V Input Range
- 16V Comparator Input Voltage Range

- Per Pin PMU

- 2 Level Driver w/ On Chip Buffers
- 14V Driver Output Swings
- 10 MHz Driver Operation
- 16V Comparator Input Voltage Range
- Extremely Low Input Leakage over a 16V Range

- Ganging Capability

- High current applications
- No limit on ganged I_{max}
- Gang control circuitry built in

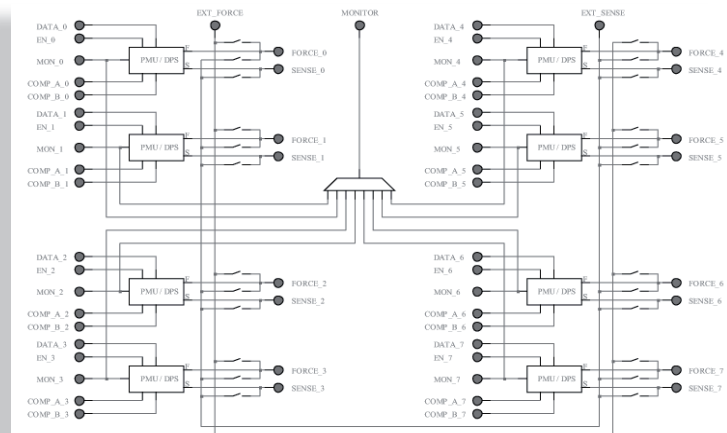
- 3 Bit Serial CPU Port

- On Chip DAC to Generate DC Levels

- 10 DC Levels per Channel (16 Bits / Level)
- On Chip Offset and Gain Correction
- Ability to shift voltage ranges up and down

- Package/Power Dissipation

- Lead Free
- 128 Lead, 14 mm X 20 mm, TQFP w/ Heat Slug
- Pd_q \leq 125 mW / Channel; Pd_q \leq 1 W / Chip
- On-Chip Thermal Monitor



ISL55185 (Triton)

SOC Octal Wide Voltage PMU/Load

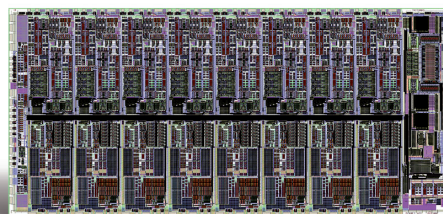
ELEVATE
SEMICONDUCTOR

The ISL55185 is a highly integrated SOC pin electronics solution incorporating 8 independent channels of:

PMU
Active load
External force/external sense

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per pin basis.



Features

- Per Channel Active Load

- 24mA Maximum Current
- MI capability
- Independent Source and Sink Current Levels
- Extremely low HiZ Leakage over a 32V Range
- 32V Input Compliance/28V Output Forcing Range

- Per Pin PMU

- FV/MI/MV
- 5 Current Ranges (24mA, 4mA, 400μA, 40μA, 4μA)
- FV Current Clamps
- 32V Input Compliance/28V Output Forcing Range
- Extremely Low Input Leakage over a 32V Range

- Monitor

- Differential Per Channel Monitor with HiZ
- Differential Central Monitor with HiZ

- External Force/Sense per Channel

- 3-bit Serial Port

- On-chip DAC to Generate DC Levels

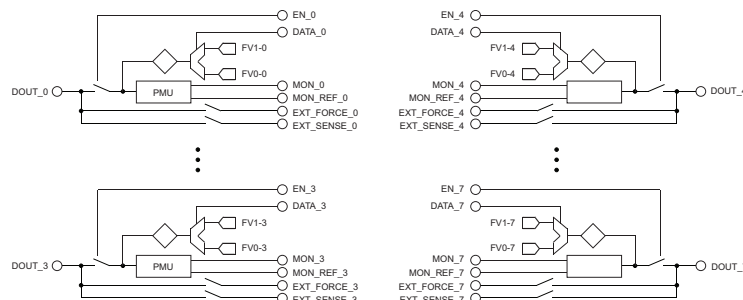
- 4 DC Levels Per Channel (16 bits/level)
- On-chip Offset and Gain Correction per Level

Applications

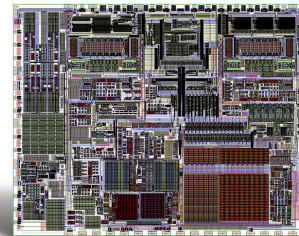
- Automated Test Equipment

- Instrumentation

- ASIC Verifier



Jupiter is a highly integrated SOC Device Under Test Power Supply (DPS) incorporating all analog and digital functionality required for a single DPS unit for Automatic Test Equipment. The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. One chip constitutes one complete DPS.



Features

- 1A DC Output Drive Capability

- 6 Current Ranges
 - (1,024 mA, 128 mA, 8 mA, 1 mA, 125 μ A, 15.625 μ A)
- Glitchless Current Range Changing
- HiZ Capability w/ Extremely Low Leakage

- Full Functionality

- FV, FI, MV, MI
- 4 Quadrant Operation
- Bump function

- Ganging Capability for Higher Current Applications

- Integrated External Force and Sense Switches

- Independent Power Supply for Output Stage

- Operating Voltage
- 24V Supply Range
- Adjustable Output Range
- 4 Voltage Ranges (4V, 8V, 16V, 24V)
- Adjustable Slew Rate
- External Precision DAC Drive Capability

- Programmable Clamps

- Voltage Clamps
- Current Clamps

- Ultra Low Noise External DAC Mode

- Programmable Alarms

- Over Current
- Over Voltage
- Over Temperature
- Kelvin Sense

- Dedicated Real Time DAC for Forcing Level

- Increment / Decrement Option
- Linear / Binary Increment / Decrement Option
- 16 Bit per Level Offset & Gain Correction

- Global External Force/Sense Connectable to any Channel

- On-Chip DC Support Levels

- 16 Bits per Level
- 16 Bit per Level Offset & Gain Correction

- 3 Bit Serial CPU Port

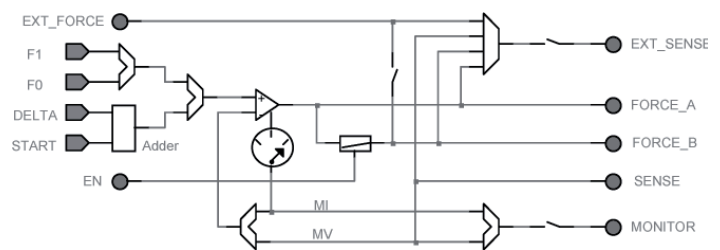
- Load Internal Registers and Memory
- Read Back Internal States

- Package

- Lead Free
- 64 Lead, 10 mm X 10 mm, TQFP w/ Heat Slug

- Power Dissipation

- Pdq (No Load) = 700 mW to 1.5 Watt



ISL55180 (Europa)

SOC 8-Channel DPS

ELEVATE
SEMICONDUCTOR

ISL55180 is a highly integrated SOC Device Under Test (DUT) power supply solution incorporating 8 independent DUT Power Supply (DPS) units.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per channel basis.

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. Real time control is accomplished via the central EN and DATA_# pins. Real time observation is accomplished via the central monitor



Features

- Per Channel DPS

- FV, FI, MV, MI, HiZ Capability
- 16V Measure Voltage Input Compliance Range
- 2 Force Voltage Ranges (8V, 16V)
- 3 Measure Voltage Ranges (4V, 8V, 16V)
- 6 Current Ranges: (256mA, 25.6mA, 2.56mA, 256μA, 25.6μA, 2.56μA)
- Programmable Current Clamps

- Power Management

- Independent Output Buffer Power Supply (VCCO)
- Ability to Exceed VCCO in Lower Current Ranges (Patent Pending)

- Flexible Ganging Capability

- No Restrictions on Maximum # DPS Units

- Protection

- On-Chip Junction Temperature Monitor
- Over-Temperature Shut Down per Chip
- Kelvin Connection Sensing/Alarm per Channel
- Over-Current Sensing/Alarm per Channel

- Global External Force/Sense Connectable to any Channel

- Monitor

- One General Purpose Central Monitor per Chip
 - Scaling and Shifting Capability
 - HiZ Capability
- One Dedicated Measure Current Monitor per Chip
 - Scaling and Shifting Capability
 - HiZ Capability

- 3-Bit Serial CPU Port

- On-Chip DAC to Generate DC Levels

- 2 Independent FV Levels/Channel
- Central Resource Mode w/16 Selectable Levels
- Independent Source and Sink Clamp Levels/Channel
- 16 bits/Level
- On-Chip Offset and Gain Correction per Level

- Package/Power Dissipation

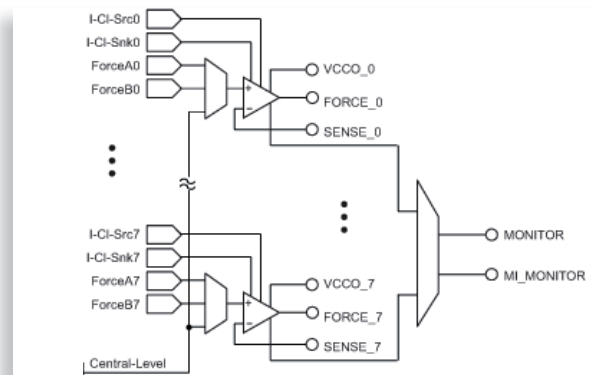
- Pb-Free (RoHS Compliant)
- 128 Lead, 14mm x 0mm, TQFP w/Exp Heat Slug
- Pd_q 100mW/Channel; Pd_q 800mW/Chip

Applications

- Automated Test Equipment

- Instrumentation

- Logic/ASIC Verifier



ELE58VE2A (Vesuvius)

SOC 8-Channel DPS

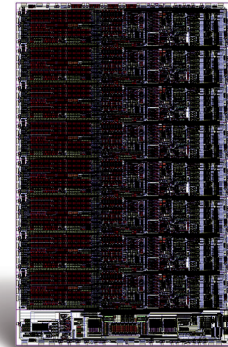
ELEVATE
SEMICONDUCTOR

Vesuvius is a highly integrated SOC Device Under Test (DUT) power supply solution incorporating 8 independent DUT Power Supply (DPS) units.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per channel basis.

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses. Real time control is accomplished via the central EN and DATA_# pins. Real time observation is accomplished via the central monitor.



Features

- Per Channel DPS

- FV, FI, MV, MI, HiZ Capability
- 16V Measure Voltage Input Compliance Range
- 2 Force Voltage Ranges (8V, 16V)
- 3 Measure Voltage Ranges (4V, 8V, 16V)
- 6 Current Ranges: (512mA, 25.6mA, 2.56mA, 256μA, 25.6μA, 2.56μA)
- Programmable Voltage and Current Clamps

- Power Management

- Independent Output Buffer Power Supply (VCCO)
- Ability to Exceed VCCO in Lower Current Ranges

- Flexible Ganging Capability

- No Restrictions on Maximum # DPS Units

- Protection

- On-Chip Junction Temperature Monitor
- Over-Temperature Shut Down per Chip
- Kelvin Connection Sensing/Alarm per Channel
- Over-Current Sensing/Alarm per Channel

- Global External Force/Sense Connectable to any Channel

- Monitor

- One General Purpose Central Monitor per Chip
 - Scaling and Shifting Capability
 - HiZ Capability
- One Dedicated Measure Current Monitor per Chip
 - Scaling and Shifting Capability
 - HiZ Capability
- Eight Independent V/I Monitors Per Chip
 - Maximum Measurement Throughput

- 3-Bit Serial CPU Port

- On-Chip DAC to Generate DC Levels

- 2 Independent FV Levels/Channel
- Central Resource Mode w/16 Selectable Levels
- Independent Source and Sink Clamp Levels/Channel
- 16 bits/Level
- On-Chip Offset and Gain Correction per Level

- Package/Power Dissipation

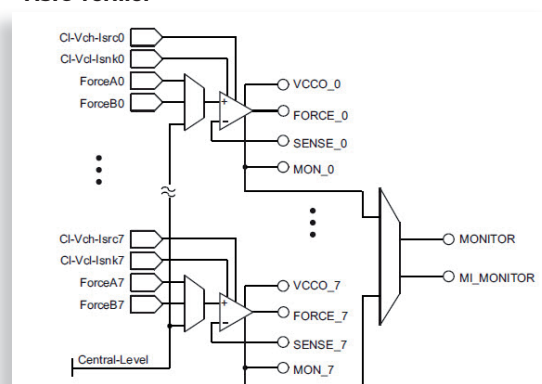
- Pb-Free (RoHS Compliant)
- 128 Lead, 14mm x 20mm, TQFP w/Exp Heat Slug
- Pdq 115mW/Channel; Pdq 920mW/Chip

Applications

- Automated Test Equipment

- Instrumentation

- ASIC Verifier



ELE58HOA (Hood)

SOC Octal High Density PPMU

ELEVATE
SEMICONDUCTOR

The Mt. Hood is a highly integrated System-on-a-Chip (SoC) High Density PPMU solution incorporating 8 independent channels of PPMU.

The interface and control are digital. All analog circuitry is inside the chip. Eight complete and independent channels are integrated into each chip.

For most tester applications, no additional analog hardware needs to be developed or used on a per-pin basis.

Features

- Per-Pin PMU

- FV, FI, MV, MI
- 4 Quadrant Operation
- -2V to 6.5V FV/MV Range
- 6 Current Ranges ($\pm 2\mu\text{A}$, $\pm 20\mu\text{A}$, $\pm 200\mu\text{A}$, $\pm 2\text{mA}$, $\pm 15\text{mA}$, $\pm 50\text{mA}$)
- Programmable Voltage and Current Clamps
- Resistive Load Function (12 Selectable Resistor Values)
- Reduced Glitch Current Range Changing

- Protection

- On-Chip Junction Temperature Monitor
- Over-Temperature Shutdown Per-Chip

- Global External FORCE/SENSE Connectable to any Channel

- Remote Sense from Adjacent Channel

- 100MHz SPI Interface

- On-Chip Independent DACs to Generate DC Levels

- 6 DC Levels per Channel
 - 2x 16-bit for Forcing Function
 - 2x 8-bit for Clamps
 - 2x 4-bit for Current Clamps
- On-Chip Offset and Gain Correction

- Monitor

- Two MV/MI Monitors (one for each 4 channels)
- Ability to Route any Channel to Either Monitor
- On-Chip Signal Preconditioning (Optimized for Direct Connection to AD7609B)

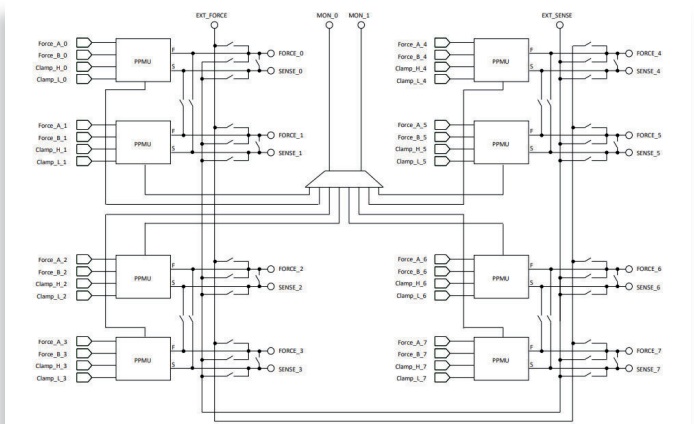
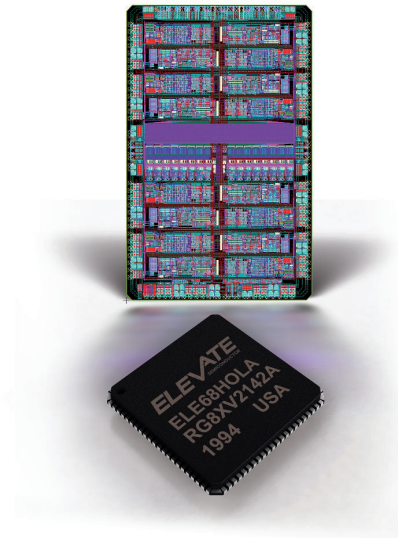
- Package/Power Dissipation

- 72 Pad, 10mm x 10mm TQFN
- Pdq 150mW/Channel
- Pstandby 75mW/Channel

Applications

- Automated Test Equipment

- Instrumentation





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