SOC 8-Channel DPS

Vesuvius

Vesuvius is a highly integrated System-on-a-Chip (SOC) Device Under Test (DUT) power supply solution incorporating 8 independent DUT Power Supply (DPS) units.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per channel basis.

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

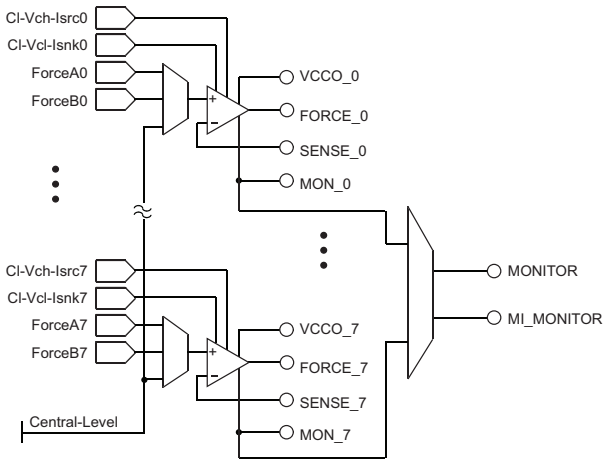
An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses.

Real time control is accomplished via the EN and DATA_# pins. Real time observation is accomplished via the per-pin or central monitor.

Applications

- Automated Test Equipment
- Logic/ASIC Verifiers
- Instrumentation

Block Diagram



Features

- Per Channel DPS
  - FV, FI, MV, MI, HiZ Capability
  - 16V Measure Voltage Input Compliance Range
  - 2 Force Voltage Ranges (8V, 16V)
  - 3 Measure Voltage Ranges (4V, 8V, 16V)
  - 6 Current Ranges: (512mA, 25.6mA, 2.56mA, 256µA, 25.6µA, 2.56µA)
  - Programmable Voltage and Current Clamps
- Power Management
  - Independent Output Buffer Power Supply (VCCO)
  - Ability to Exceed VCCO in Lower Current Ranges (Patent Pending)
- Flexible Ganging Capability
  - No Restrictions on Maximum # DPS Units
- Protection
  - On-Chip Junction Temperature Monitor
  - Over-Temperature Shut Down per Chip
  - Kelvin Connection Sensing/Alarm per Channel
  - Over-Current Sensing/Alarm per Channel
- Global External Force/Sense Connectable to any Channel
- Monitor
  - Per-pin Monitor for enhanced throughput
    - HiZ Capability
    - Scaling and Shifting Capability
  - One General Purpose Central Monitor per Chip
    - Scaling and Shifting Capability
    - HiZ Capability
  - One Dedicated Measure Current Monitor per Chip
    - HiZ Capability
- 3-Bit Serial CPU Port
- On-Chip DAC to Generate DC Levels
  - 2 Independent FV Levels/Channel
  - Central Resource Mode w/16 Selectable Levels
  - Independent Source and Sink Clamp Levels/Channel
  - 16 bits/Level
  - On-Chip Offset and Gain Correction per Level
- Package/Power Dissipation
  - Pb-Free (RoHS Compliant)
  - 128 Lead, 14mmx20mm, LQFP w/Exp Heat Slug
  - Pdq 115mW/Channel; Pdq 920mW/Chip

Block Diagram

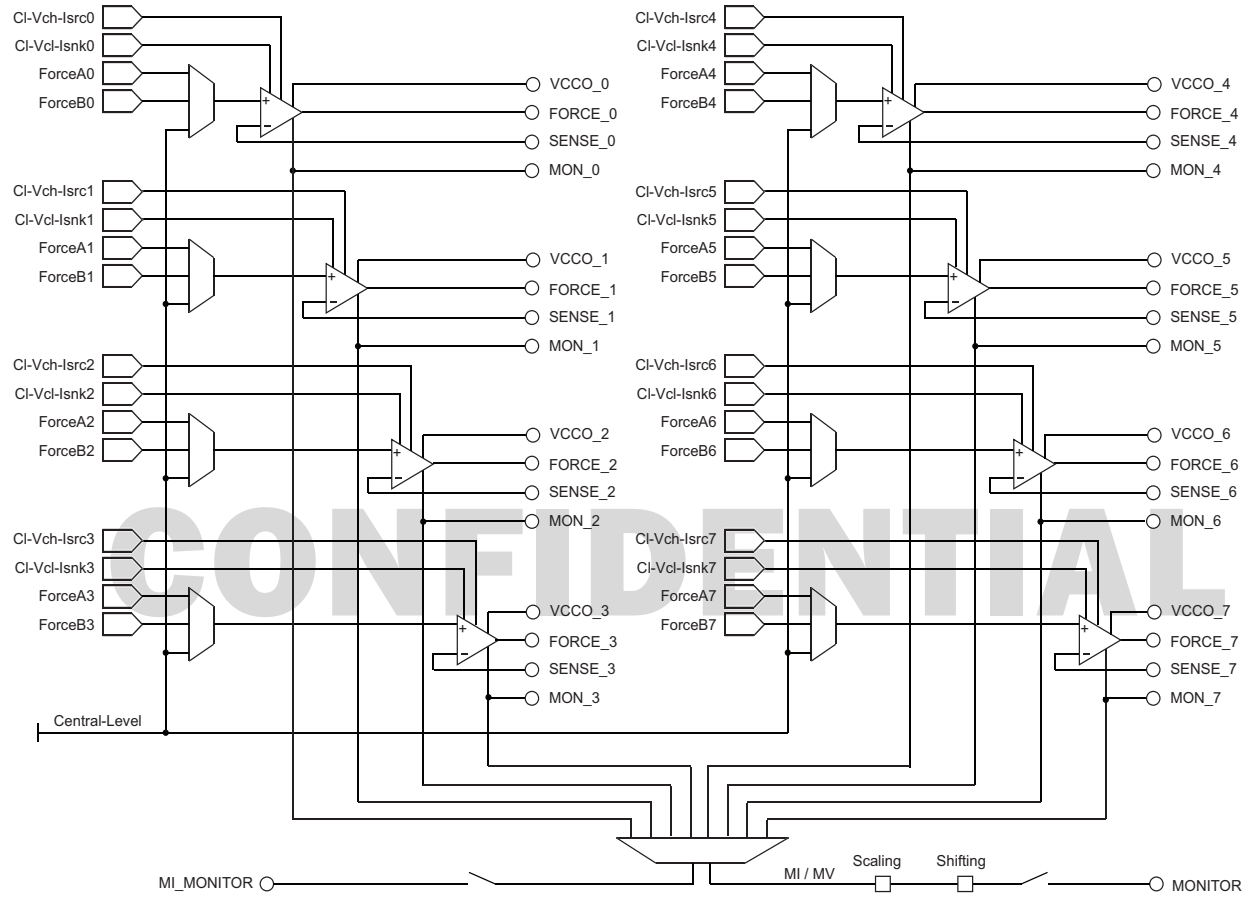


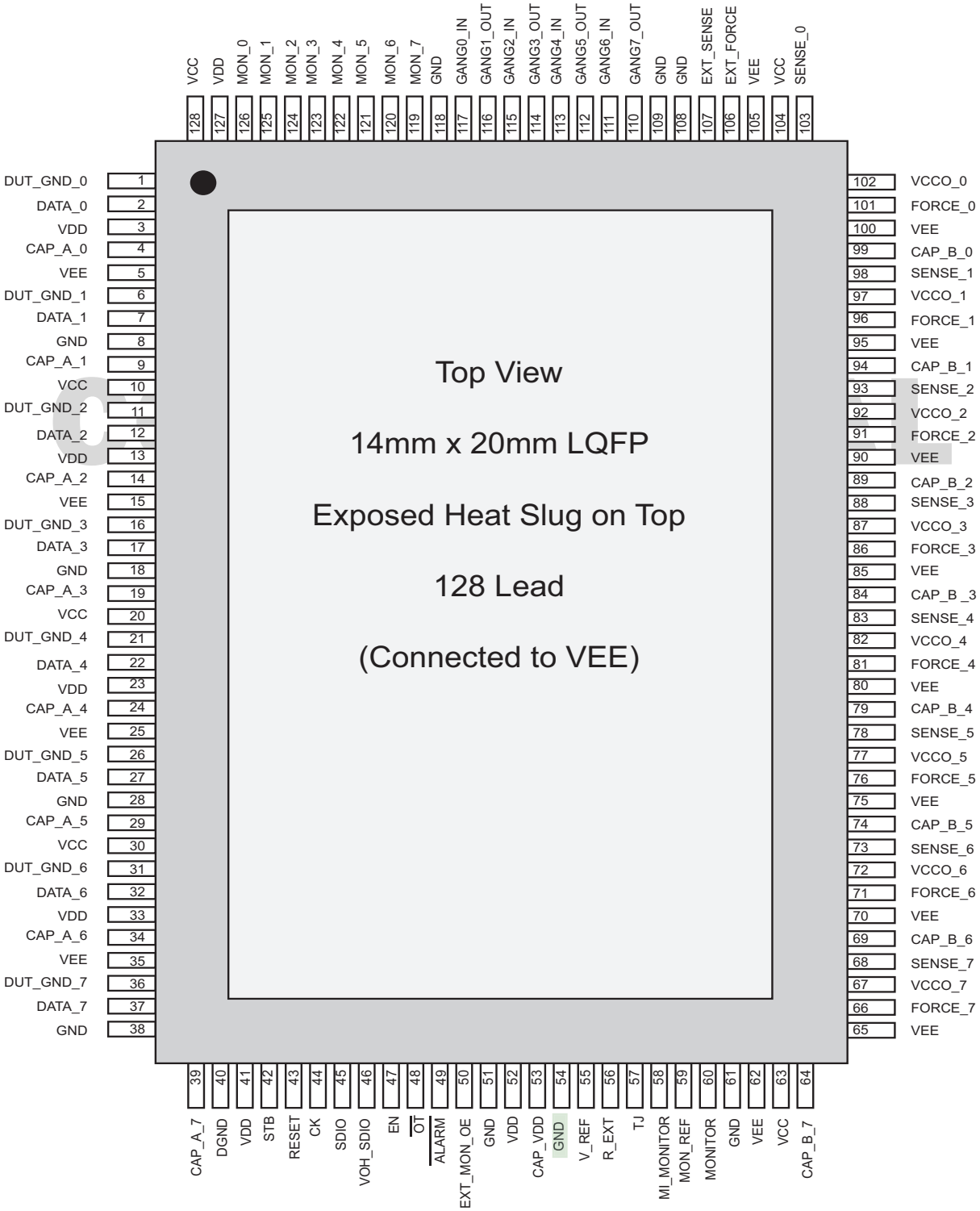
Table of Contents

Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
101, 103, 1	FORCE_0, SENSE_0, DUT_GND_0	Channel 0 force, sense, and DUT ground pins.
2	DATA_0	Channel 0 data input pin.
102	VCCO_0	Positive analog supply for the Channel 0 output stage.
4, 99	CAP_A_0, CAP_B_0	Channel 0 op amp compensation capacitor pins.
126	MON_0	Channel 0 V/I monitor output pin.
96, 98, 6	FORCE_1, SENSE_1, DUT_GND_1	Channel 1 force, sense, and DUT ground pins.
7	DATA_1	Channel 1 data input pin.
97	VCCO_1	Positive analog supply for the Channel 1 output stage.
9, 94	CAP_A_1, CAP_B_1	Channel 1 op amp compensation capacitor pins.
125	MON_1	Channel 1 V/I monitor output pin.
91, 93, 11	FORCE_2, SENSE_2, DUT_GND_2	Channel 2 force, sense, and DUT ground pins.
12	DATA_2	Channel 2 data input pin.
92	VCCO_2	Positive analog supply for the Channel 2 output stage.
14, 89	CAP_A_2, CAP_B_2	Channel 2 op amp compensation capacitor pins.
124	MON_2	Channel 2 V/I monitor output pin.
86, 88, 16	FORCE_3, SENSE_3, DUT_GND_3	Channel 3 force, sense, and DUT ground pins.
17	DATA_3	Channel 3 data input pin.
87	VCCO_3	Positive analog supply for the Channel 3 output stage.
19, 84	CAP_A_3, CAP_B_3	Channel 3 op amp compensation capacitor pins.
123	MON_3	Channel 3 V/I monitor output pin.
81, 83, 21	FORCE_4, SENSE_4, DUT_GND_4	Channel 4 force, sense, and DUT ground pins.
22	DATA_4	Channel 4 data input pin.
82	VCCO_4	Positive analog supply for the Channel 4 output stage.
24, 79	CAP_A_4, CAP_B_4	Channel 4 op amp compensation capacitor pins.
122	MON_4	Channel 4 V/I monitor output pin.
76, 78, 26	FORCE_5, SENSE_5, DUT_GND_5	Channel 5 force, sense, and DUT ground pins.
27	DATA_5	Channel 5 data input pin.
77	VCCO_5	Positive analog supply for the Channel 5 output stage.
29, 74	CAP_A_5, CAP_B_5	Channel 5 op amp compensation capacitor pins.
121	MON_5	Channel 5 V/I monitor output pin.
71, 73, 31	FORCE_6, SENSE_6, DUT_GND_6	Channel 6 force, sense, and DUT ground pins.
32	DATA_6	Channel 6 data input pin.
72	VCCO_6	Positive analog supply for the Channel 6 output stage.
34, 69	CAP_A_6, CAP_B_6	Channel 6 op amp compensation capacitor pins.
120	MON_6	Channel 6 V/I monitor output pin.
66, 68, 36	FORCE_7, SENSE_7, DUT_GND_7	Channel 7 force, sense, and DUT ground pins.
37	DATA_7	Channel 7 data input pin.
67	VCCO_7	Positive analog supply for the Channel 7 output stage.
39, 64	CAP_A_7, CAP_B_7	Channel 7 op amp compensation capacitor pins.

PIN #	PIN NAME	DESCRIPTION
119	MON_7	Channel 7 V/I monitor output pin.
55, 56	V_REF, R_EXT	External precision voltage and resistance reference.
57, 48, 49	TJ, $\overline{OT}$, $\overline{ALARM}$	On-chip die temperature monitor, OT flag and alarm outputs.
47	EN	Real time HiZ control pin.
60, 58	MONITOR, MI_MONITOR	Central monitor and measure current monitor analog outputs.
59, 50	MON_REF, EXT_MON_OE	Monitor negative reference output and external HiZ control pins.
44, 45, 42, 43	CK, SDIO, STB, RESET	Serial port control pins.
106, 107	EXT_FORCE, EXT_SENSE	Central external force and sense pins.
117, 116	GANG0_IN, GANG1_OUT	External ganging pins for Channels 0 and 1.
115, 114	GANG2_IN, GANG3_OUT	External ganging pins for Channels 2 and 3.
113, 112	GANG4_IN, GANG5_OUT	External ganging pins for Channels 4 and 5.
111, 110	GANG6_IN, GANG7_OUT	External ganging pins for Channels 6 and 7.
10, 20, 30, 63, 104, 128	VCC	Analog positive power supply.
5, 15, 25, 35, 62, 65, 70, 75, 80, 85, 90, 95, 100, 105	VEE	Analog negative voltage supply
3, 13, 23, 33, 41, 52, 127	VDD	Digital power supply.
8, 18, 28, 38, 51, 54, 61, 108, 109, 118	GND	Chip ground.
40	DGND	Digital ground.
46	VOH_SDIO	Positive supply rail to the SDIO output pin.
53	CAP_VDD	External filter capacitor for VDD.

Pin Configuration



Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	VDD – 0.5		+15	V
VCCO_#	–0.5		VCC + 0.5	V
VEE	–5		0.5	V
VDD	–0.5		+5	V
VCC – VEE	–0.5		17.5	V
VDD – VEE		+8		V
Digital Pins				
CK, SDIO, STB, RESET	GND – 0.5V		VDD + 0.5	V
SENSE	GND – 0.5V		VDD + 0.5	V
MONITOR	GND – 0.5V		VDD + 0.5	V
$\overline{\text{ALARM}}$, $\overline{\text{OT}}$	GND – 0.5V		VDD + 0.5	V
CENTRAL_D_#	GND – 0.5V		VDD + 0.5	V
EN	GND – 0.5V		VDD + 0.5	V
DATA_#	GND – 0.5V		VDD + 0.5	V
SDIO Output Current	–20		+20	mA
External References				
R_EXT		10		KΩ
V_REF	GND – 0.5V		VDD + 0.5	V
Analog Pins				
FORCE_#	VEE – 0.5		VCC + 0.5	V
SENSE_#	VEE – 0.5		VCC + 0.5	V
MONITOR	GND – 0.5	20	VDD + 0.5	V
MI_MONITOR	GND – 0.5	20	VDD + 0.5	V
EXT_SENSE	VEE – 0.5		VCC + 0.5	V
EXT_FORCE	VEE – 0.5		VCC + 0.5	V
GANG#_IN	VEE – 0.5		VCC + 0.5	V
GANG#_OUT	VEE – 0.5		VCC + 0.5	V
TEST+, TEST–	GND – 0.5	20	VDD + 0.5	V
TJ	GND – 0.5	20	VDD + 0.5	V
DUT_GND	VEE – 0.5		VCC + 0.5	V
Thermal Information				
Maximum Junction Temperature			150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supplies				
VCC	+8		+14	V
VCCO_#	FORCE_# +0.5		VCC	V
VEE	–4		–2	V
VDD	+3.25		3.45	V
VCC – VEE	+10		+16	V
VCCO_# – VEE	+6		+16	V
VDD – VEE	+.525		+7.4	V
Digital Pins				
CK, SDIO, STB, RESET	GND		VDD	V
EXT_MON_OE	GND		VDD	V
EN	GND		VDD	V
DATA_#	GND		VDD	V
CENTRAL_D_#	GND		VDD	V
$\overline{\text{ALARM}}$, $\overline{\text{OT}}$	GND		VDD	V
External References				
V_REF	+2.99		3.01	V
R_EXT	10KΩ ± 0.1% tempco = 25ppm			
Analog Pins				
FORCE_# (HiZ Compliance)	VEE		VCC	V
IR0 - IR5 (FV Mode# = 0) FORCE_# (Active, FV, I_{OUT} = 0) FORCE_# (Active, FV, $\pm I_{MAX,}$ ±512mA)	 VEE + 1.5 to Min of ((VCCO – 0.15) or (VCC – 1.0)) VEE + 4.0 to Min of ((VCCO – 1.5) or ((VCC – 3.0))			 V V
IR0 - IR4 (FV Mode# = 1) FORCE_# (Active, FV, I_{OUT} = 0) FORCE_# (Active, FV, $\pm I_{MAX}$)	 VEE + 1.5 VEE + 2.0		 VCC – 1.0 VCC – 1.5	 V V
IR5 (FV Mode# = 1) FORCE_# (Active, FV, $\pm I_{MAX}$)	N/A		N/A	N/A
SENSE_#	VEE		VCC	V
MONITOR	GND		VDD	V
MI_MONITOR	GND		VDD	V
EXT_SENSE	VEE		VCC	V
EXT_FORCE	VEE		VCC	V
GANG#_IN, GANG#_OUT	VEE + 1.5		VCC - 1.5	V
TEST+, TEST–	GND		VDD	V
TJ	GND		VDD	V
Miscellaneous				
Junction Temperature	+25		100	°C
CPU Port CK Frequency	10		25	MHz
Capacitive Load at DOUT_# (IR0 - IR5)	0		50	µF

DC Characteristics

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications – Power Supply Current

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	Pd (TYP) mW/Chip
NO LOAD, FV-Mode# = 0							
11100	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, FV-Mode = 0, IR5, FV = +3V, Bbias = 1..		100	150	mA	1250
11200	ICC_O			1.3	35	mA	5.5
11300	IEE		–160	–108		mA	378
11400	IDD			55	85	mA	190
11500	IOH_SDIO		–2.5	0	2.5	mA	0
NO LOAD, FV-Mode = 1							
11110	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, FV-Mode = 1, IR4, FV = +3V, Bbias = 0.		100	150	mA	1250
11210	ICC_O			0.5	3.5	mA	2125
11310	IEE		–160	–108		mA	378
11410	IDD			55	85	mA	190
11510	IOH_SDIO		–25	0	2.5	mA	0
+I_{MAX}, FV-Mode = 0							
11120	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, +I_{MAX}, IR5, FV-Mode = 0, FV = +3V, all 8 channels sourcing 512mA each, Bbias = 0.		188	195	mA	2086
11220	ICC_O			4.25	4.5	A	6039
11320	IEE		–365	–350		mA	1225
11420	IDD			55	85	mA	190
11520	IOH_SDIO		–2.5	0	2.5	mA	0
+I_{MAX}, FV-Mode = 1							
11130	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V VDD = +3.45V, +I_{MAX}, IR4, FV-Mode = 1, FV = +8V, all 8 channels sourcing 25.6mA each, Bbias = 0.		325	365	mA	2424
11230	ICC_O			0.5	30	mA	2.1
11330	IEE		–160	–123		mA	430.5
11430	IDD			55	85	mA	190
11530	IOH_SDIO		–2.5	0	2.5	mA	0
–I_{MAX}, FV-Mode = 0							
11121	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, –I_{MAX}, IR5, FV-Mode = 0, FV = +3V, all 8 channels sinking 512mA each, Bbias = 1.		341	350	mA	4263
11221	ICC_O			30	40	mA	128
11321	IEE		–4.5	–4.47		A	27933
11421	IDD			55	85	mA	190
11521	IOH_SDIO		–2.5	0	2.5	mA	0
–I_{MAX}, FV-Mode = 1							
11131	ICC	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V VDD = +3.45V, –I_{MAX}, IR4, FV-Mode = 1, FV = +8V, all 8 channels sinking 25.6mA each, Bbias = 1.		118	150	mA	1475
11231	ICC_O			0.5	30	mA	2.1
11331	IEE		–365	–325		mA	2828
11431	IDD			55	85	mA	190
11531	IOH_SDIO		–2.5	0	2.5	mA	0

NOTE: The total chip power values are based upon typical supply currents and power supply levels indicated in the test conditions. For proper sizing of power supplies in the application, power to the DUT or load being driven the Vesuvius must also be accounted for.

DC Electrical Specifications – Thermal Monitor and Alarm

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TJ, $\overline{OT}$						
10996	TJ HiZ Leakage	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, Tested at 0V and VDD	–500	0	+500	nA
	Over-Temperature Threshold	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V		135 ± 15	150	°C
10994	$\overline{OT}$ VOH (HiZ Leakage)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, Tested at 0V and VDD	–100	0	+100	nA
	$\overline{OT}$ VOL	VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V, Input current = 2mA			0.4	V

DC Electrical Specifications – CPU Port

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SDIO, CK, STB, RESET						
17100	VIH	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V	1.6			V
17110	VIL	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V			0.8	V
17120	I_{IN} (Input Leakage Current)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, tested at 0V and VDD	–1	0	+1	µA
17200	VOH (SDIO Only)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V, VOH_SDIO = VDD, I_{LOAD} = 8mA	2.4			V
17210	VOL (SDIO Only)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V, VOH_SDIO = VDD, I_{LOAD} = 8mA			0.8	V

DC Electrical Specifications – Digital Inputs

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
EN, DATA_#						
13260	VIH	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V	2.0			V
13261	VIL	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V			0.8	V
13262	I_{IN} (Input Leakage Current) (HiZ)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, tested at 0V and VDD	–1	0	+1	µA

DC Electrical Specifications –Digital Outputs

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ALARM						
13360	VOL (Sinking 4mA)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.3V			0.4	V
13361	VOH (HiZ Leakage)	VCC = +12.5V, VCCO_# = +4.25V, VEE = –3.5V, VDD = +3.45V, tested at 0V and VDD	–100		+100	nA

DC Electrical Specifications – Analog Pins

VCC = +12.5V, VCCO_# = 4.25V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Leakage/Input Currents						
10999	V_REF Input Current		–1		+1	µA
10998	DUT_GND Input Current	Tested at –1V, 0V and +1V	–15		+15	nA
10700	EXT_FORCE, EXT_SENSE in HiZ	Tested at 0V, VCC, VEE	–15		+15	nA
10800	GANG#_IN Input Current	Tested at VCC – 1.5V, VEE + 1.5V	–1		+1	µA
10801	GANG#_OUT HiZ Leakage Current	Tested at VCC – 1.5V, VEE + 1.5V, Sel-G#-OUT and Sel-G(#–1)– OUT = 1	–1		+1	µA
20210	CAP_A_#, CAP_B_# Leakage Current		–100		+100	nA
20560	CAP_VDD Leakage Current	Not production tested.	–15		+15	µA

Level DAC Calibration

All DC tests are performed after the DAC is first calibrated.The upper 5 bits of the DAC are calibrated in the sequence D11 to D15. The DAC Cal bits are adjusted to make the major carry error as small as possible.

DC Electrical Specifications – DAC Calibration

VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
16510	Level DAC D15 Step Error	(DAC@8000 - DAC@7FFF)/(8000 – 7FFF) – DAC LSB; VR0, Code 8000 – Code 7FFF – LSB; VR0	-2		+2	mV
16520	Level DAC D14 Step Error	(DAC @ 7000 - DAC @ 3000)/(7000 – 3000) – DAC LSB; VR0, Code 4000 – Code 3FFF – LSB; VR0	-2		+2	mV
16530	Level DAC D13 Step Error	(DAC @ 7000 - DAC @ 5000)/(7000 – 5000) – DAC LSB; VR0, Code 6000 – Code 5FFF – LSB; VR0	-2		+2	mV
16540	Level DAC D12 Step Error	(DAC @ 7000 - DAC @ 6000)/(7000 – 6000) – DAC LSB; VR0, Code 7000 – Code 6FFF – LSB; VR0	-2		+2	mV
16550	Level DAC D11 Step Error	(DAC @ 7800 - DAC @ 7000)/(7800 – 7000) – DAC LSB; VR0, Code 7800 – Code 77FF – LSB; VR0	-2		+2	mV
16560	LSB Step Error	8V Range, FV-Mode = 1, Post auto calibration		124		µV

There are 3 on-chip internal DACs used for:

1. DC Level
2. DC Level Offset Correction
3. DC Level Gain Correction

DAC testing is performed post DAC Cal Bit Calibration.

DC Electrical Specifications – DAC

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LEVEL DAC TEST						
16100	Span	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Span = DAC(FFFF) – DAC(0000), Notes 1, 2	7.5	8.9	9.5	V
16110	Linearity Error	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 3	–2	0.6	+2	mV
16120	Bit Test Error	Offset and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 4	–2	0.6	+2	mV
16190	Droop Test	Notes 1, 5	–1		+1	mV/ms
16400	DAC Noise	FV = 0V, Measured at FORCE_0, RMS measurement, Note 1			+1.0	mV
OFFSET DAC TEST						
16200	+ Adjustment Range	Level and Gain DACs both programmed to mid scale (Code 7FFF), Code 0000, FFFF relative to mid scale (7FFF), Notes 1, 2	+4.5	+5.4	+6.6	% of Span
16210	- Adjustment Range	Level and Gain DACs both programmed to mid scale (Code 7FFF), Code 0000, FFFF relative to mid scale (7FFF), Notes 1, 2	–6.6	–5.4	+4.5	% of Span
16220	Linearity Error	Level and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 3	–3	1.5	+2	mV
16230	Bit Test Error	Level and Gain DACs both programmed to mid scale (Code 7FFF), Notes 1, 2, 4	–3	1.5	+2	mV
GAIN DAC TEST						
16300	+ Adjustment Range	Level DAC = FFFF, Offset DAC = 7FFF, Code 0000, FFFF relative to mid scale (7FFF), Notes 2, 6	1.18	1.25	1.30	V/V
16300	- Adjustment Range	Level DAC = FFFF, Offset DAC = 7FFF, Code 0000, FFFF relative to mid scale (7FFF), Notes 2, 6	0.7	0.75	0.81	V/V
16310	Linearity Error	Level DAC = FFFF, Offset DAC = 7FFF, Notes 2, 3, 6	–3	0.5	+4	mV/V
16320	Bit Test Error	Level DAC = FFFF, Offset DAC = 7FFF, Notes 2, 4, 6	–3	0.5	+4	mV/V
16330	DUT_GND Error	DUT_GND forced to ±1V. Measured at the FORCE pin, Note 6	–6		+6	mV

NOTES:

1. VCC = +12V, VCCO_# = +4V, VEE = –4V, VDD = +3.3V
2. DAC tests performed using the DPS in FV mode and the MONITOR output. 8V Range, FV-Mode = 1.
3. Linearity Test - 17 equal spaced codes relative to a straight line determined by 1/8 and 7/8 measurement points: 0000, 0FFF, **1FFF**, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, **DFFF**, EFFF, FFFF. (Calibration points in **bold**.)
4. Bit Test - Walking 1 and walking 0 to determine the correct bit weight 1's: 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100, 0080, 0040, 0020, 0010, 0008, 0004, 0002, 00010's: 7FFF, BFFF, DFFF, EFFF, F7FF, FBFF, FDFF, FEFF, FF7F, FFBF, FFDF, FFEF, FFF7, FFFB, FFFD, FFFE.
5. CPU CK turned off. 66ms delay between measurements. Each DC level on the chip checked one at a time.
6. VCC = +12.9V, VCCO_# = +4V, VEE = –2.9V, VDD = +3.2V.

Force Voltage

Channel Configuration:

1. Feedback# = SENSE_#

The sequence of events performed for FV Testing is:

1. Program VF#
2. Force current at FORCE_# w/external resource
3. Measure the voltage at FORCE_#.

DC Electrical Specifications – FV

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV (POST CALIBRATION)						
14200	Output Force Error	VCC =+ 12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V, FV_MODE = 0 (8V range), Calibration points: 0V, 2.5V No-Load Test Points: –1.5V, +1V, +3.75V. Tested in IR3, IR4, and IR5 only. Full-Load Test Points ($\pm I_{MAX}$): 0V, 3V. Tested in IR3, IR4, and IR5 only.	–5		+5	mV
14201	Output Force Error	VCC =+ 12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V, FV_MODE = 1 (16V range), Calibration points: 0V, 10V No-Load Test Points: –2V, +5V, +12V. Tested in IR0 and IR4 only. Full-Load Test Points ($\pm I_{MAX}$): –1.5V, 11V. Tested in IR0, IR1, IR2, IR3, and IR4 only.	–10		+10	mV
FV TEMPERATURE COEFFICIENT						
	8V Range	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0		60		µV/°C
	16V Range	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0		200		µV/°C
HIZ LEAKAGE						
14090	FORCE_#, SENSE_#	VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, Tested at 0V, (VCC-1.5V), VEE, TightLoop*# = 1	–5	< 0.1	+5	nA
CAPACITANCE						
	FORCE_# Capacitance	VCC = +12.5V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0		400		pF
	SENSE_# Capacitance	VCC = +12.5V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0		15		pF
PROTECTION						
	Short Circuit Current	VCC = +12.5V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0, IR5, FV-Mode = 0, FV = +3V, output shorted to ground		768 ± 20%		mA

Measure Current

Post CME Adjust.

TABLE 1. OUTPUT SOURCING

RANGE	CAL POINTS	TPI	TPI2
IR0 FV-Mode = 1 VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/0.8 • Imax +5V/0.2 • Imax	+5V/+I_{MAX} +5V/(+I_{MAX}/2)	+5V/0
IR1 – IR4 FV-Mode = 1 VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/0.8 • Imax +5V/0.2 • Imax	+5V/+I_{MAX} +5V/(+I_{MAX}/2) +5V/0	
IR3 – IR5 FV-Mode = 0 VCC = +8V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/0.8 • Imax +2.5V/0.2 • Imax	+2.5V/+I_{MAX} +2.5V/(+I_{MAX}/2) +2.5V/0	

TABLE 2. OUTPUT SINKING

RANGE	CAL POINTS	TPI
IR0 – IR4 FV-Mode = 1 VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/–0.2 • Imax +5V/-0.8 • I_{MAX}	+5V/–I_{MAX} +5V/(–I_{MAX}/2) +5V/0
IR3 – IR5 FV-Mode = 0 VCC = +8V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/–0.2 • Imax +2.5V/–0.8 • Imax	+2.5V/–I_{MAX} +2.5V/(–Imax/2) +2.5V/0

DC Electrical Specifications – Measure Current

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FII and MI (POST CALIBRATION)						
14100A	Measure Current Error	TPI (See Tables 1 and 2), IR0, Bbias = 0, FV_MODE = 1	–0.1% FS		+0.1% FS	nA
14100B	Measure Current Error	TPI2 (See Tables 1 and 2), IR0, Bbias = 0, FV_MODE = 1	–0.3% FS		+0.3% FS	nA
14101	Measure Current Error	TPI (See Tables 1 and 2), IR1, Bbias = 0, FV_MODE = 1	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	nA
14102	Measure Current Error	TPI (See Tables 1 and 2), IR2, Bbias = 0, FV_MODE = 1	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	µA
14103A	Measure Current Error	TPI (See Tables 1 and 2), IR3, Bbias = 1, IOUT > ±256µA, FV_MODE = 1	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	µA
14103B	Measure Current Error	TPI (See Tables 1 and 2), IR3, Bbias = 1, –256µA ≤ IOUT ≤ 256µA, FV_MODE = 0	–1.25% FS		+1.25%FS	µA
14104	Measure Current Error	TPI (See Tables 1 and 2), IR4, Bbias = 1, IOUT > ±2.56mA, FV_MODE = 1	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	µA
14104B	Measure Current Error	TPI (See Tables 1 and 2), IR4, Bbias = 1, –2.56mA ≤ IOUT ≤2.56mA, FV_MODE = 0	–1.25% FS		+1.25%FS	mA
14105	Measure Current Error	TPI (See Tables 1 and 2), IR5, Bbias = 1, IOUT > ±25.6mA, FV_MODE = 0	–(0.1% FS + 0.1%MV)		+(0.1% FS + 0.1%MV)	mA
14105B	Measure Current Error	TPI (See Tables 1 and 2), IR5, Bbias = 1, –25.6mA ≤ IOUT ≤ 25.6mA, FV_MODE = 0	–1.25% FS		+1.25%FS	mA
	MI Temperature Coefficient	IR0		±0.025		nA/°C
	MI Temperature Coefficient	IR1		±0.335		nA/°C
	MI Temperature Coefficient	IR2		±1		nA/°C
	MI Temperature Coefficient	IR3		±0.340		µA/°C
	MI Temperature Coefficient	IR4		±2.03		µA/°C
	MI Temperature Coefficient	IR5		±4.18		µA/°C
Common Mode Error (CME)						
14140	Maximum CME Adjustment Range	VCC = +12.9V, VCCO_# =+ 4V, VEE = –2.9V, VDD = +3.2V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V	–0.0125		+0.0125	%FS Current/ V

Force Current

Post CME Adjust.

TABLE 3. OUTPUT SOURCING

	CAL POINTS	TPI
IR0 – IR4 FV-Mode = 1 VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/0.6 • Imax +5V/–0.6 • Imax	+5V/+I_{MAX} +5V/(+I_{MAX}/2) +5V/(+I_{MAX}/5) +5V/(+I_{MAX}/10)
IR3 – IR5 FV-Mode = 0 VCC = +8V, VCCO_# = +4V, VEE = -3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	**RANGE** +2.5V/0.6 • Imax +2.5V/–0.6 • Imax	+2.5V/+I_{MAX} +2.5V/(+I_{MAX}/2) +2.5V/(+I_{MAX}/5) +2.5V/(+I_{MAX}/10)

TABLE 4. OUTPUT SINKING

RANGE	CAL POINTS	TPI
IR0 – IR4 FV-Mode = 1 VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+5V/0.6 • Imax +5V/–0.6 • I_{MAX}	+5V/–I_{MAX} +5V/(–I_{MAX}/2) +5V/(–I_{MAX}/5) +5V/(-I_{MAX}/10)
IR3 – IR5 FV-Mode = 0 VCC = +8V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.25V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0	+2.5V/0.6 • Imax +2.5V/–0.6 • Imax	+2.5V/–I_{MAX} +2.5V/(–I_{MAX}/2) +2.5V/(–I_{MAX}/5) +2.5V/(-I_{MAX}/10)

DC Electrical Specifications – Force Current

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

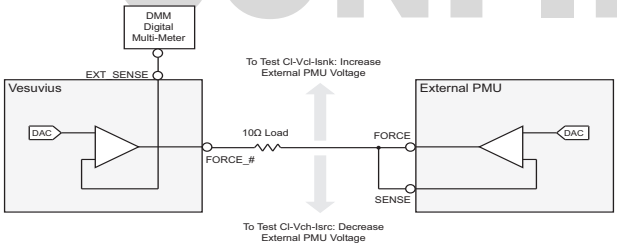
Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FII and MI (POST CALIBRATION)						
15100	Force Current Error	TPI (See Tables 3 and 4), IR0, Bbias = 0	–100		+100	nA
15101	Force Current Error	TPI (See Tables 3 and 4), IR1, Bbias = 0	–1		+1	µA
15102	Force Current Error	TPI (See Tables 3 and 4), IR2, Bbias = 0	–10		+10	µA
15103	Force Current Error	TPI (See Tables 3 and 4), IR3, Bbias = 0	–200		+200	µA
15104	Force Current Error	TPI (See Tables 3 and 4), IR4, Bbias = 0	–1		+1	mA
15105	Force Current Error	TPI (See Tables 3 and 4), IR5, Bbias = 0	–10		+10	mA
	FI Temperature Coefficient	IR0		±1.9		nA/°C
	FI Temperature Coefficient	IR1		±1.6		nA/°C
	FI Temperature Coefficient	IR2		±7.7		nA/°C
	FI Temperature Coefficient	IR3		±21.3		µA/°C
	FI Temperature Coefficient	IR4		±1		µA/°C
	FI Temperature Coefficient	IR5		±19.5		µA/°C
Common Mode Error (CME)						
15140	Maximum CME Adjustment Range	VCC = +12.9V, VCCO_# =+ 4V, VEE = –2.9V, VDD = +3.2V, VOH_SDIO = VDD, VREF = +3V, DUT_GND = 0V	–0.0125		+0.0125	%FS Current/ V

Current Clamps

Current clamps are tested in IR5 only.

The sequence of events to test the Source Current Clamps is as follows (this list is not an all-inclusive setup list). Please also refer to the figure below:

1. Program Cl-Vch-Isrc<15:0> to Test Point/Calibration Point.
2. Set Cl-En# = 1.
3. Set proper path to so that: Feedback# = Force_#.
4. Set Con-ES-F# = 1.
5. Set ForceA#<15:0> = 2V.
6. Measure Voltage at EXT_SENSE pin. (Initial FV Level)
7. Connect 10Ω load from FORCE_# on Vesuvius to External PMU.
8. Set External PMU voltage = 2V.
9. Decrease External PMU voltage until voltage measured at EXT_SENSE moves from the initial FV Level by the following amount: 15mV> (Initial FV Level - Measured FV Level) >5mV.
10. Use External PMU to measure current sourced by Vesuvius.



The sequence of events to test the Sink Current Clamps is as follows (this list is not an all-inclusive setup list). Please also refer to the figure below:

1. Program Cl-Vcl-Snk#<15:0> to Test Point/Calibration Point.
2. Set Cl-En# = 1.
3. Set proper path to so that: Feedback# = Force_#.
4. Set Con-ES-F# = 1.
5. Set ForceA#<15:0> = 2V.
6. Measure Voltage at EXT_SENSE pin. (Initial FV Level)
7. Connect 10Ω load from FORCE_# on Vesuvius to External PMU.
8. Set External PMU voltage = 2V.
9. Increase External PMU voltage until voltage measured at EXT_SENSE moves from the initial FV Level by the following amount: 15mV> (Initial FV Level - Measured FV Level) >5mV.
10. Use External PMU to measure current sunk by Vesuvius.

TABLE 5.

LEVEL	CAL POINTS	TP0
Cl-Vch-Isrc	+100mA +500mA	+300mA +768mA
Cl-Vcl-Isnk	−100mA −500mA	−300mA −768mA

DC Electrical Specifications – Current Clamps

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TP0 Test Points						
14500	Source Clamp Error	VCC = +12.9V, VCCO_# = +4V, VEE = −2.9V, VDD = +3.2V, VOH_SDIO = VDD, DUT_GND = 0V (See Table 3)	−2		+2	%FS
14520	Sink Clamp Error	VCC = +12.9V, VCCO_# = 4V, VEE = −2.9V, VDD = +3.2V, VOH_SDIO = VDD, DUT_GND = 0V (See Table 3)	−2		+2	%FS

DC Electrical Specifications – Voltage Clamps

Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14430	Voltage Clamp Post Calibration Error	See Table 6	−300		+300	mV
14428	Voltage Clamp Operating Range		VEE + 1.5		VCC − 2.5	V

TABLE 6.

MV RANGE	Vclamp CAL POINTS	Vclamp TEST POINTS
16V	–1V	–2V
	+11V	+5V
		+12V

Measure Voltage – Central Monitor

The sequence of events performed for testing the MONITOR is:

1. Program Channel 0 in FV to the desired voltage (IR3, I_{LOAD} = 0)
2. Measure the voltage at FORCE_0
3. Measure the voltage at MONITOR
4. Calculate the difference to determine the error.

DC Electrical Specifications– Monitor

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MONITOR, MON_# Measure Voltage Error						
14800	4V Range	Note 1, Table 7	–2	1	+2	mV
14801	8V Range	Note 1, Table 7	–3		+3	mV
14802	16V Range	Note 1, Table 7	–6		+6	mV
MV Temperature Coefficient						
	4V Range	Note 1, Table 7		50		µV/°C
	8V Range	Note 1, Table 7		100		µV/°C
	16V Range	Note 1, Table 7		150		µV/°C
Uncalibrated MONITOR, MON_# MV Offset						
14830	4V Range	Note 1, Table 7	0.475		0.525	V
14831	8V Range	Note 1, Table 7	0.95		1.05	V
14832	16V Range	Note 1, Table 7	0.72		0.78	V
Uncalibrated MONITOR, MON_# MV Gain						
14840	4V Range	Note 1, Table 7	0.47		0.53	V/V
14841	8V Range	Note 1, Table 7	0.235		0.265	V/V
14842	16V Range	Note 1, Table 7	0.115		1.135	V/V
Output Impedance and Leakage						
19112	MONITOR, MON_# Output Impedance	Tested at +2.5V, IOUT = 0µA/+100µA and 0µA/–100µA; Note 1, Table 7	75		1,000	Ω
14710	MONITOR, MON_# HiZ Leakage Current	VCC = +12.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V, tested at MONITOR = 0V	–10	< 0.1	+10	nA
14711	MON_REF Output Impedance	VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V	75	70	150	Ω
14712	MON_REF HiZ Leakage	VCC = +13.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V	–10	< 0.1	+10	nA
14713	MI_MONITOR Output Impedance	Note 1	100		200	Ω

DC Electrical Specifications– Monitor

VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
14714	MI_MONITOR HiZ Leakage	VCC = +13.5V, VCCO_# = +4V, VEE = –3.5V, VDD = +3.45V	–10	< 0.1	+10	nA
14715	MONITOR, MON_# Short Circuit Current	IR5, FV-Mode = 0, FV = +3V, output shorted to ground; Note 1	5		15	mA
14716	MI_MONITOR Short Circuit Current	IR5, FV-Mode = 0, FV = +3V, output shorted to ground; Note 1	5	10	15	mA
NOTES: 1. VCC = +13V, VCCO_# = +4V, VEE = –3V, VCC = +3.3V.						

TABLE 7.

MV RANGE	MV CAL POINTS	MV TEST POINTS
4V	+0.5V	0V
	+3.5V	2V
		4V
8V	–1V	–2V
	+5V	+2V
		+6V
16V	–1V	–2V
	+11V	+5V
		+12V

DC Electrical Specifications – Switch Resistance Values

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
On-Chip Switches						
	Tj-En		100		175	kΩ
	Con-ES-F#		0.75		1.65	kΩ
	Con-EF-F#		11		35	Ω
	Con-ES-S#		1.75		3	kΩ
	Con-FS#		0.75		1.25	kΩ

DC Electrical Specifications – Kelvin Alarms

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Kelvin Alarm High and Low						
14400	Gain	All codes tested vs their nominal program values	50	150	300	mV/code
14410	Offset	All codes tested vs their nominal program values	40	150	350	mV
14420	Linearity Error	All codes tested vs their nominal program values	-100		+100	mV
14425	Hysteresis		10	40	100	mV

DC Electrical Specifications – Central Level Gain and Offset

VCC = +13V, VCCO_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gain Test						
16390	MaximumGain	AV#<7:0> = 7F Hex; Note 1	960		985	mV/V
16391	Minimum Gain	AV#<7:0> = FF Hex; Note 1	1010		1050	mV/V
16392	Linearity	Note 2		0.25		mV/V
16294	Bit Test	Note 3		0.25		mV
16295	Resolution	Note 4		185		µV/V
	Span	(AV Gain Max) – Av Gain Min)		90		mV
Offset Test						
16290	Maximum Offset	OS#<15:0> = FF Hex; Note 1	–100		–60	mV
16291	Minimum Offset	OS#<15:0> = 7F Hex; Note 1	60		100	mV
16292	Linearity	Note 5		0.05		mV
16294	Span Test	(OS Max) – (OS Min)		170		mV
16296	Resolution	Note 6		650		µV

NOTES:

1. Central DAC tests performed in FV mode tested and at Force A at 2V.
2. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and7/8 codes: 7F, 6F, 5F, 4F, 3F, 2F, 1F, 0F, 8F, 9F, AF, BF, CF, DF, EF, FF. Actual measurement vs. straight line determined by the calibration points.
3. B it Test - Walking 1 and walking 0 to determine the bit weight. 1's - 40, 20, 10, 08, 04, 02, 01, C0, A0, 90, 88, 84, 82, 81. 0's - 3F, 5F, 6F, 77, 7B, 7D, 7E, BF, DF, EF, F7, FB, FD, FE. Actual measurement vs. straight line determined by the calibration points.
4. Gain Resolution Test: (AV-Gain<4C> – AV-Gain <CC>/ 152..
5. Linearity Test - 16 equal spaced codes relative to a straight line determined by 1/8 and 7/8 codes: 0000, 0FFF, 1FFF, 2FFF, 3FFF, 4FFF, 5FFF, 6FFF, 7FFF, 8FFF, 9FFF, AFFF, BFFF, CFFF, DFFF, EFFF, FFFF. Actual measurement vs. straight line determined by the calibration points.
6. Offset resolution test –(Offset at level <4C> – Level <CC> / 152.

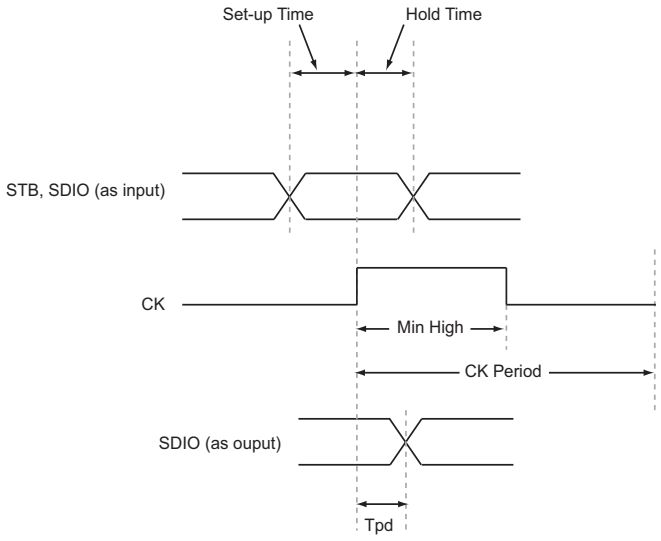
AC Characteristics

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications– CPU Port

VCC = +13V, VCC0_# = +4V, VEE = –3V, VDD = +3.3V, DUT_GND = 0V. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

SPEC #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
	Setup Time					
2136	SDIO to Rising CK		11			ns
27139	STB to Rising CK		10			ns
	Hold Time					
	SDIO to Rising CK		10			ns
	STB to Rising CK		10			ns
	CK Minimum Pulse Width High		20			ns
	CK Minimum Pulse Width Low		20			ns
	CK Period		40		100	ns
	Propagation Delay					
	Rising CK to SDIO Out				15	ns
	Reset Minimum Pulse Width		100			ns



AC Electrical Specifications – DPS

VCC +13V, VCCO_# = +5V, VEE = –3V, VDD = +3.30V, VOH_SDIO = VDD, V_REF = +3V, DUT_GND = 0. Parameters with MIN and/or MAX limits are 100% tested at TA = +25°C, unless otherwise specified. Settling times measured from 50% of final value to within 2% of final value. Temperature limits established by characterization and are not production tested.

Spec #	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FV SETTLING TIME						
	IR0			8		µs
	IR1 - IR5	0V to 3V step using DATA_# pin to switch between ForceA# and ForceB#. Con-Cap# = 0, Con-Res# = 0. Bbias# = 1. Resistive Load = 0Ω. Capacative Load = 10nF.		5		µs
MV SETTLING TIME						
	4V Range	MV		3		µs
	8V Range	MV		3		µs
	16V Range	MV		3		µs
MI SETTLING TIME						
	IR0	FV Mode. Load step from 0 to +Imax. Capacative Load = 1nF. Con-Cap#<0,1,2> = 1. Con-Res# = 0. Bbias = 0.		130		µs
	IR1			65		µs
	IR2			35		µs
	IR3	FV Mode. Load step from 0 to +Imax. Capacative Load = 10nF. Con-Cap# = 0. Con-Res# = 0. Bbias = 0.		9		µs
	IR4			5		µs
	IR5			5		µs

Chip Overview

Vesuvius is a highly integrated SOC DUT power supply solution incorporating 8 independent DPS units.

The interface, the control, and the I/O are digital; all analog circuitry is inside the chip. For most tester applications, no additional analog hardware needs to be developed or used on a per channel basis.

CPU Control

All configuration setup and the writing to and reading back of the internal registers are controlled through the 3-bit serial data CPU port. The CPU port is typically used to setup the operating conditions of each channel prior to executing a test, or to change modes during a test.

An internal register chart (Memory Map), listed later in the data sheet, lists all programmable control signals and their addresses.

Real Time Control

Real time control is accomplished via the EN and DATA_# pins. Real time observation is accomplished via the central or per-pin monitors..

Analog References

All on chip analog levels are related to off-chip precision voltage and resistance references:

- V_REF
- R_EXT

These external references are used to provide accurate and stable analog circuit performance with minimal variation over time, temperature, supply voltage, part-to-part, or process changes.

External Signal Nomenclature

All input and output pins, when referred to in the data sheet or in any circuit diagram, use the following naming conventions:

1. All capital letters (i.e. FORCE_0, CK, SDIO)
2. Underscores for clarity (i.e. SENSE_0)
3. Shown next to an I/O circle in any schematic

CPU Programmed Control Line Nomenclature

Any internal signal, DAC level, or control signal which is programmed via the CPU port uses a different nomenclature:

1. The first letter in a word is always a capital letter
2. Subsequent letters within the same word are small
3. Dashes *(but never an underscore)* for clarity
4. NOT shown with an I/O circle in any schematic

Control lines, internal registers, and other internal signals, which are programmable by the CPU port, are listed in the Memory Map table.

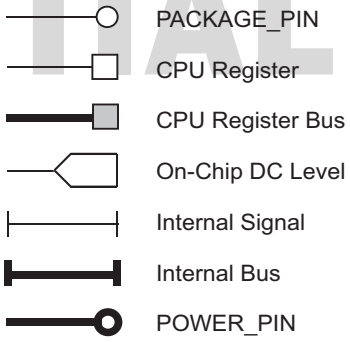


FIGURE 1.

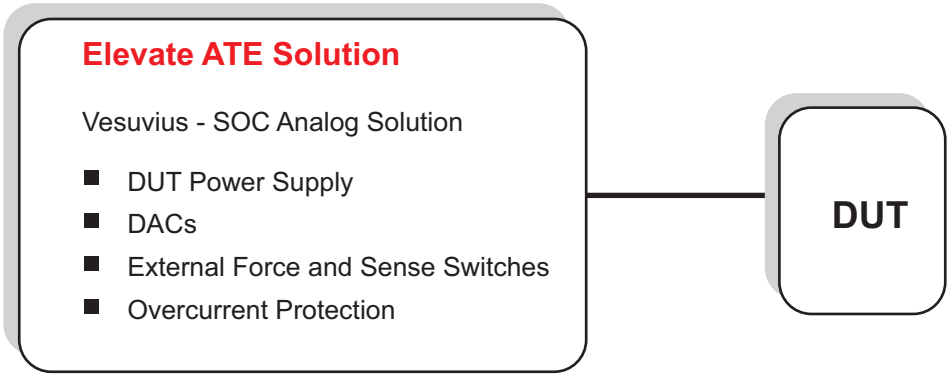
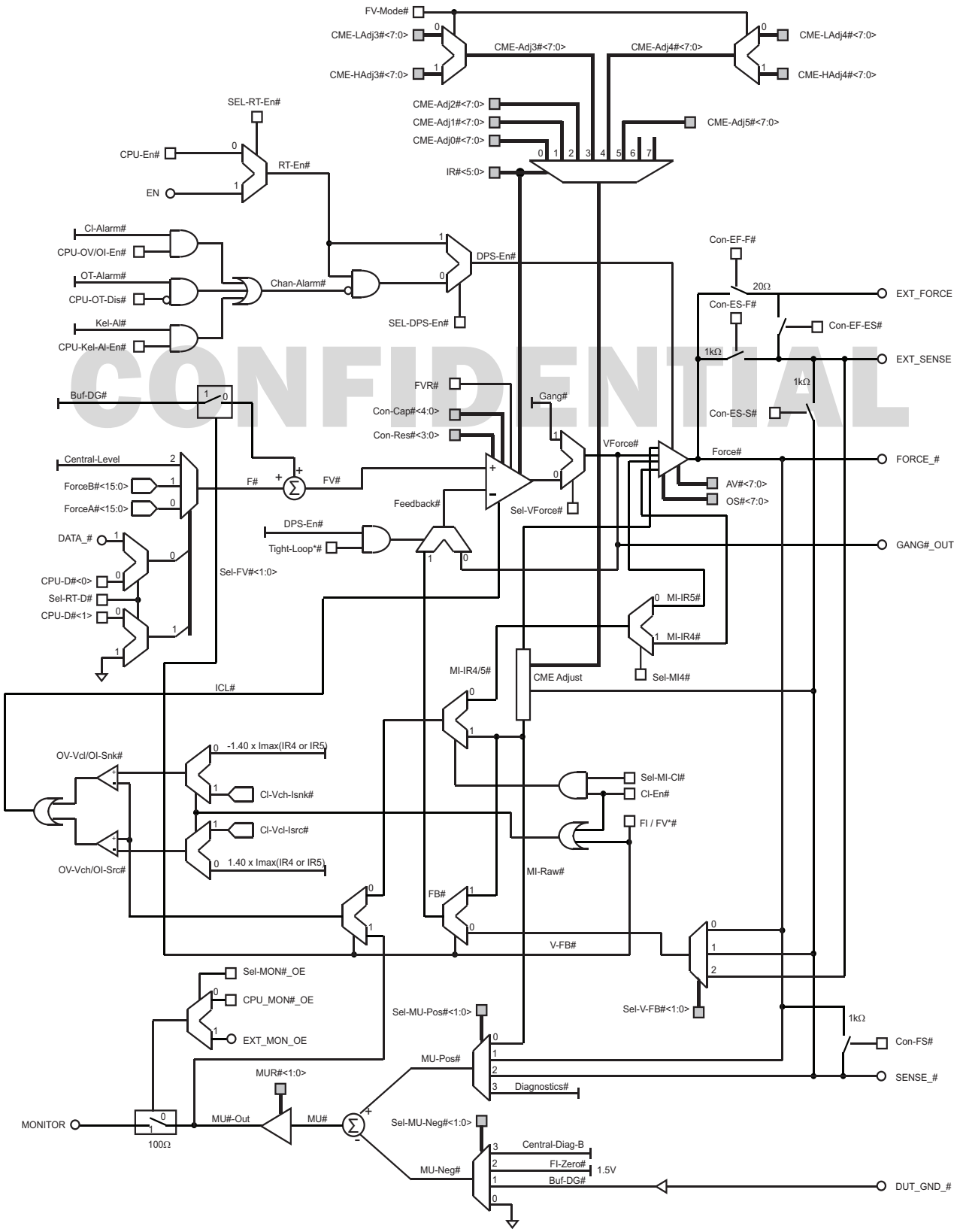


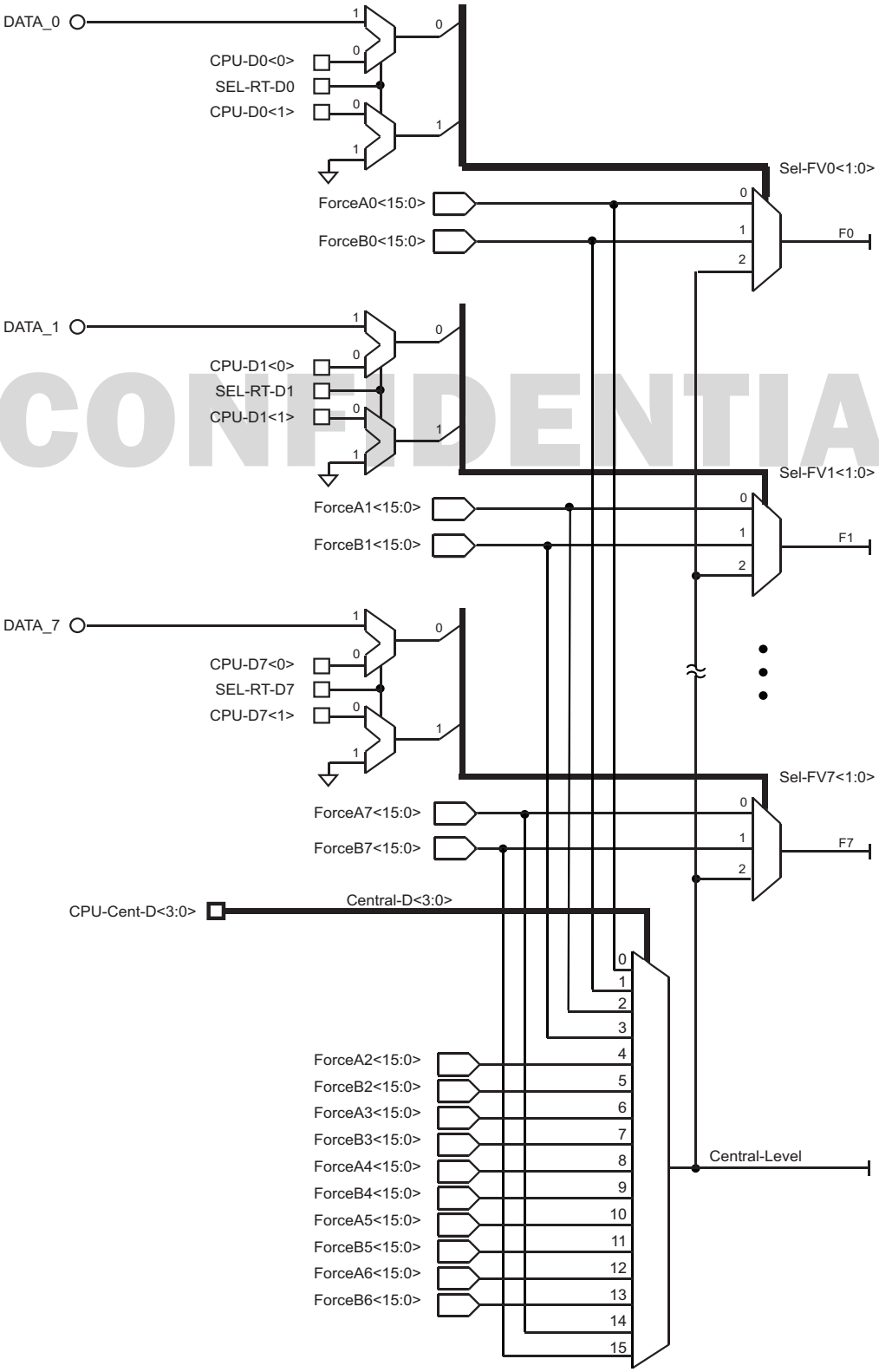
FIGURE 2.

Circuit Diagrams

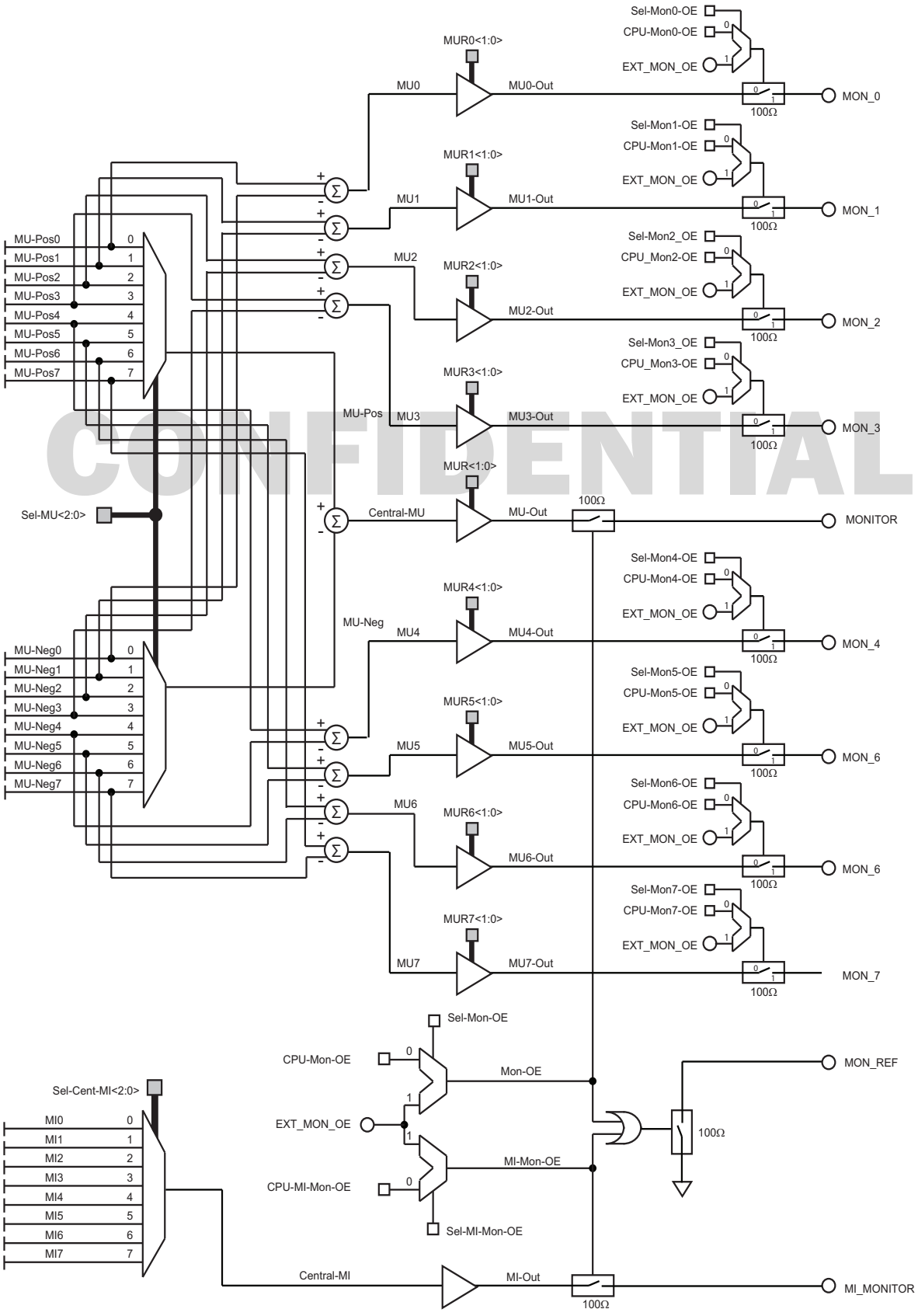
Per Channel Diagram



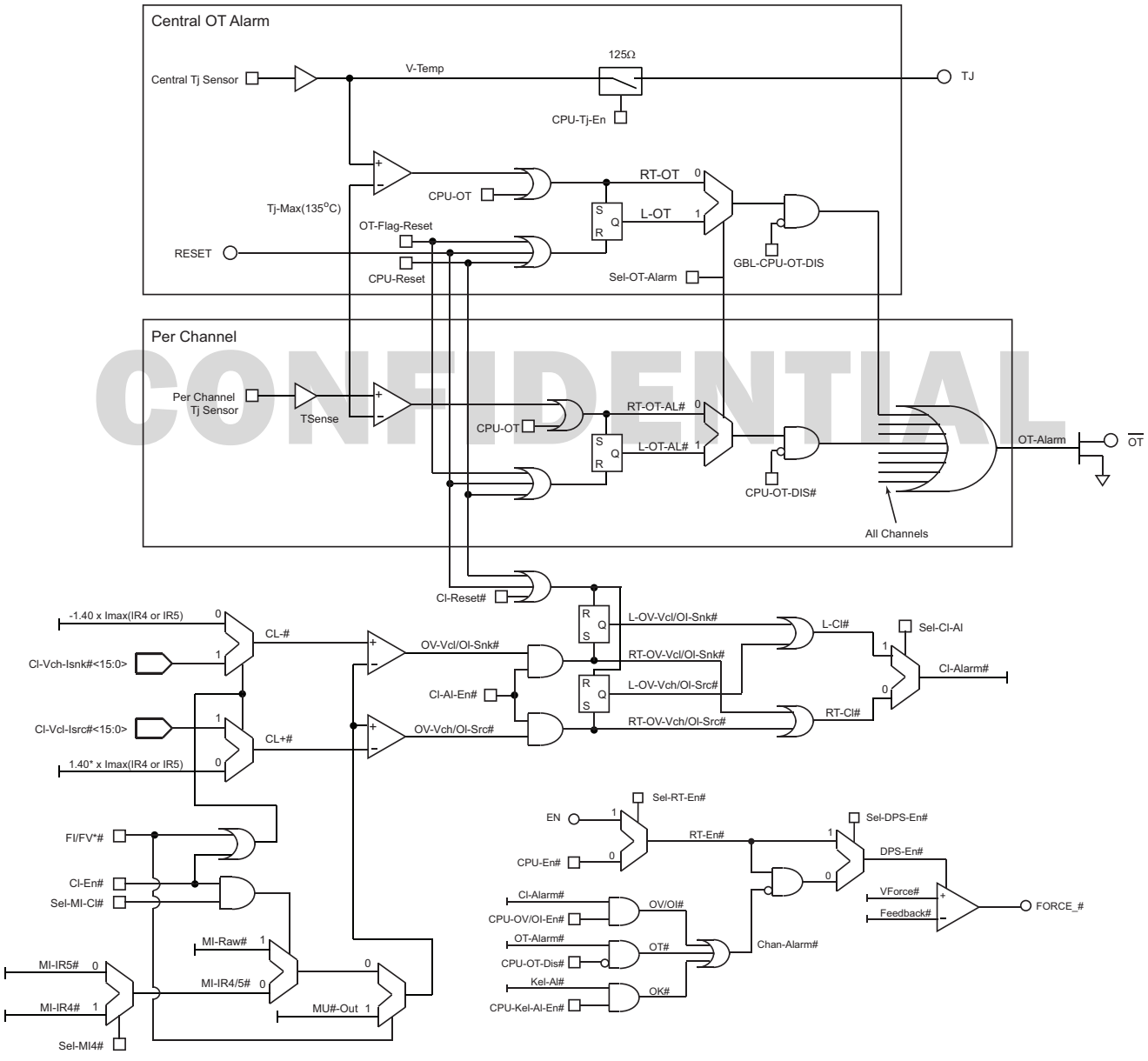
Central Resource vs. Channel Mode



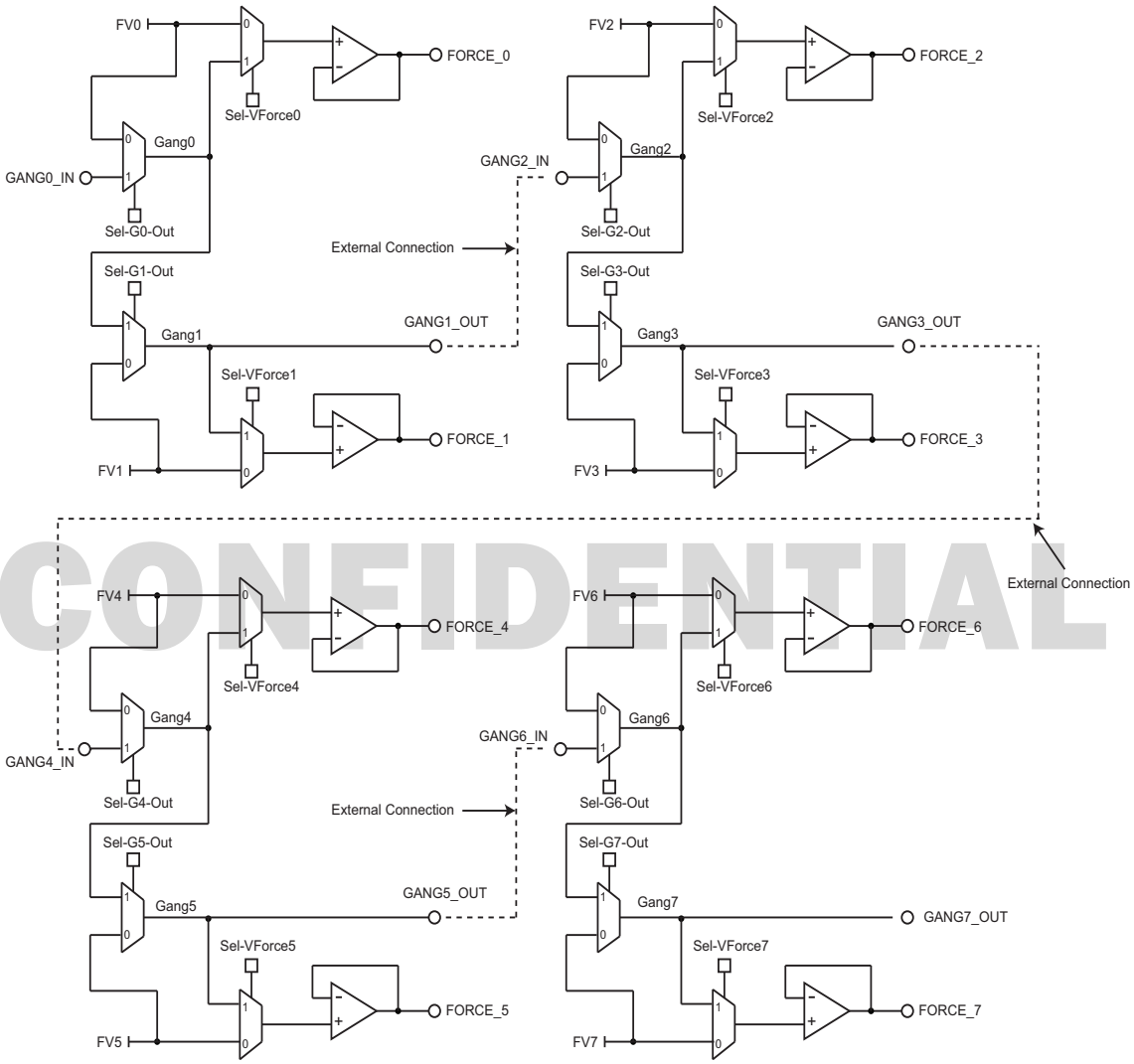
Measurement Unit



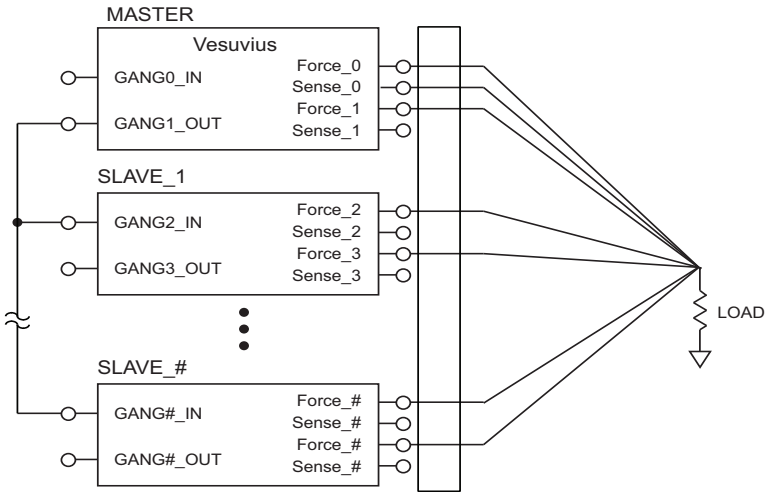
OI, OT and Kelvin Alarm



Serial Ganging with One Chip



Ganging Across Multiple Vesuvius's



Overview

Each channel is independent and has the ability to:

Force:

- Force Voltage (FV)
- Force Current (FI)
- Go into a HiZ state

Measure:

- Measure Voltage (MV)
- Measure Current (MI)

Gang:

- Gang with other channels for extended current capability

There are no restrictions between which parameter is being forced and which is being measured.

Mode Selection

The CPU port establishes the operating mode of the chip.

TABLE 1. FORCE MODE

Sel-VForce#	MODE	VForce#	FI/FV*#	CI-En#
0	FV	FV#	0	0, 1
1	Gang	Gang#	0	N/A
0	FI	FV#	1	N/A

Current Ranges

The CPU port selects the current range. Each range is set independently, allowing flexibility in “make-before-break” options.

TABLE 2. CURRENT RANGES

RANGE	IR#<5:0>	IMAX
IR0	000001	±2.56µA
IR1	000010	±25.6µA
IR2	000100	±256µA
IR3	001000	±2.56mA
IR4	010000	±25.6mA
IR5	100000	±512mA

There is a transfer function between the current at the force pin and the voltage measuring the current at the MONITOR or MI_MONITOR pin. It is important to note that Imax (maximum current) is not the maximum current that the DPS can output at each current range. Imax is the full-scale current that can be measured in each current range. The maximum current of the per-channel DPS can be output on any current range (approximately 768mA).

TABLE 3. MEASURE CURRENT

CURRENT @ FORCE_#	MI# (Measure Current)
+Imax	+2.033V V(MI(+Imax))
0	+1.5V FI-Zero#
-Imax	+0.967V V(MI(-Imax))

High Impedance

Each channel may be placed in a HiZ state where it maintains an extremely low leakage as long as the FORCE_# output pin remains between the analog power supply rails.

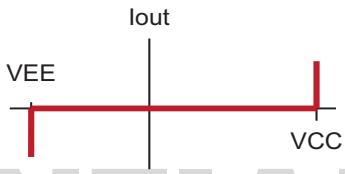


FIGURE 1. LEAKAGE CURRENT ACROSS VOLTAGE RANGE

TABLE 4. HIZ MODE SELECTION

DPS-En#	CHANNEL # DPS STATUS
0	HiZ
1	Active

TABLE 5. HIZ MODE CONTROL

Sel-RT-En#	Sel-DPS-En#	DPS-En#
0	1	CPU-En#
1	1	EN
X	0	RT-En# • $\overline{\text{Chan-Alarm\#}}$

HiZ can be controlled by the CPU port, an external real time input pin, or alarm signal. The EN pin is common for all channels. The alarm signal is unique for each channel. The CPU port exercises enable control on a per channel basis.

Channel Alarm

Each channel may be placed into HiZ based upon:

- an overcurrent situation
- an over-temperature situation
- a Kelvin alarm

OV/OI# = CI-Alarm# • CPU-OV/OI-En#

OT# = OT-Alarm# • CPU-OT-Dis#

OK# = Kel-AI# • CPU-Kel-AI-En#

Chan-Alarm# = OV/OI# + OT# + OK#

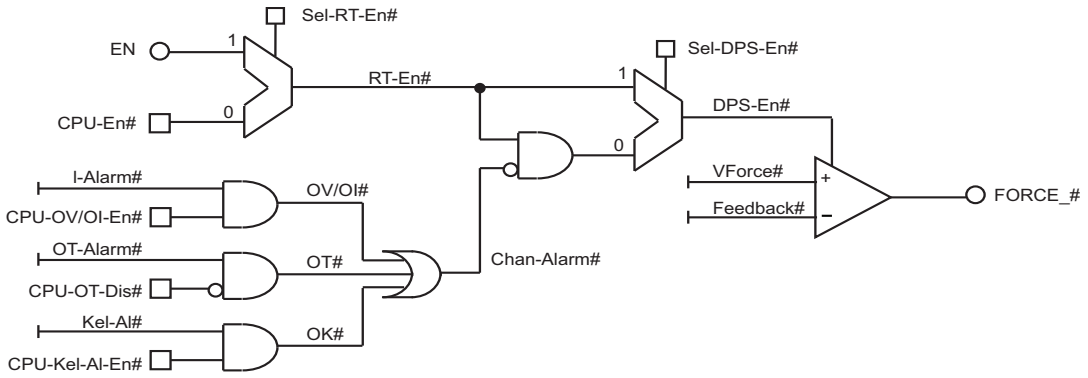


FIGURE 2. DPS FORCING CIRCUITRY

Force Voltage

The CPU port can place the DPS in FV mode. In FV mode, the voltage at FORCE_# is offset by and will track any changes in DUT_GND#.

The resulting forcing voltage is FV# = F# + Buf-DG#

TABLE 6. DPS MODE CONTROL

Sel-VForce#	DPS MODE
0	FV
1	Gang

Forcing Op Amp Input Source

The Vesuvius supports a wide variety of inputs that are used to drive the main forcing op amp. This selection can be made by the CPU Port or by an external real-time pin which controls the Sel-FV#<1:0> bits. Sel-FV#<1:0> can also be read back through the CPU Port.

TABLE 7. DAC LEVEL SELECTION

Sel-RT-D#	Sel-FV#<1:0>
0	CPU-D#<1:0>
1	<0, DATA_#>

TABLE 8. DAC LEVEL ROUTING

Sel-FV#<1:0>	MODE	F#
00	Per Channel	ForceA#<15:0>
01	Per Channel	ForceB#<15:0>
10	Central Resource	Central-Level
11	Restricted	N/A

Per Channel Mode

In per-channel mode, each channel has two independent levels, ForceA# and ForceB#, that may be selected as the input to the forcing op amp.

The ForceA#/ForceB# selection may be made by the CPU port or by an external real-time pin.

Central Resource Mode

In central resource mode, each channel may select any of the 16 levels on the chip as the input to the forcing op amp via the serial interface.

The central level is selected from all of the per-channel DC levels.

TABLE 9. CENTRAL DAC LEVEL SELECTION

Central-D<3:0>	Central-Level
0000	ForceA0
0001	ForceB0
0010	ForceA1
0011	ForceB1
•	•
1110	ForceA7
1111	ForceB7

The central DC level selection can be made by the CPU port.

Central Level Calibration

Each channel has a separate offset and gain correction that is independent from the gain and offset associated with each DC level. This additional calibration path allows for accurate outputs when in the central resource mode.

TABLE 10. CENTRAL DAC OFFSET CALIBRATION REGISTERS

OS#<7:0>	CH# OFFSET (16V)	CH# OFFSET (8V)
11111111	–160mV	–80mV
11111110	-126mV	-63mV
•	•	•
10000000	0mV	0mV
00000000	0mV	0mV
•	•	•
01111110	+126mV	+63mV
01111111	+160mV	+80mV
Resolution	1.26mV	0.63mV

TABLE 11. CENTRAL DAC GAIN CALIBRATION REGISTERS

AV#<7:0>	GAIN ADJ (16V)	GAIN ADJ (8V)
11111111	.9492	.9746
11111110	.9496	.9748
•	•	•
10000001	.9996	.9996
10000000	1.000	1.000
00000000	1.0000	1.0000
00000001	1.0004	1.0002
•	•	•
01111110	1.0504	1.0252
01111111	1.0508	1.0254
Resolution	400µV/V/Code	200µV/V/Code

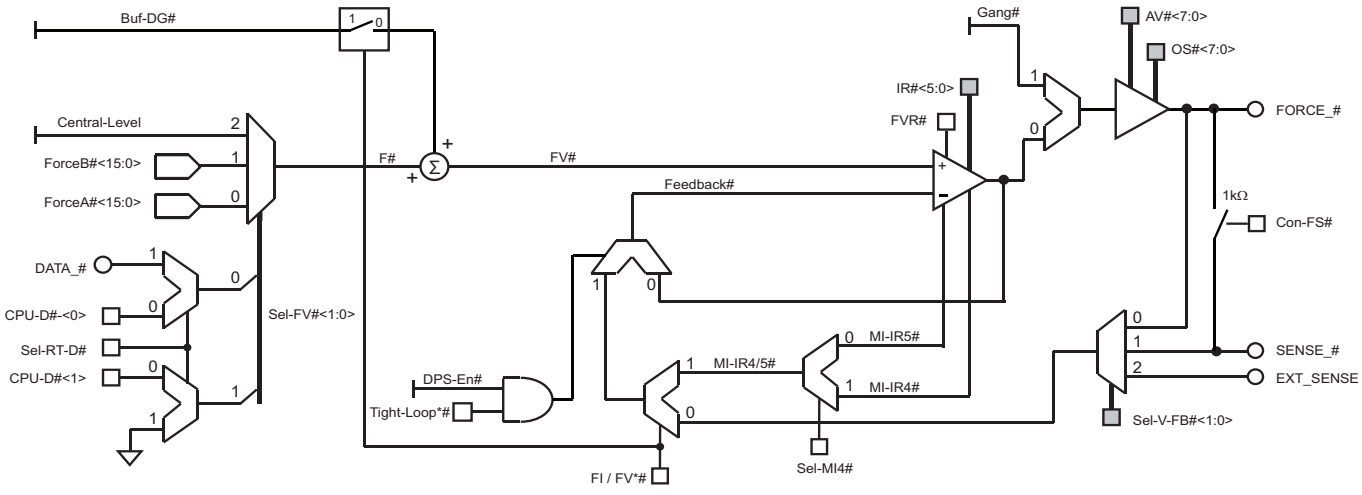


FIGURE 3. DPS CHANNEL USING CENTRAL LEVEL

FV Mode

The CPU port can establish the force voltage mode of the DPS on a per-channel basis.

TABLE 12. FV MODE SELECTION

FV-MODE#	DPS MODE
0	High Current (uses VCCO_#)
1	Low Current (uses VCC)

In the high curent range, the DPS supports all current ranges. In the low current range, the DPS supports all but the highest current range but over a wider voltage range (patented).

TABLE 13. FV MODE VS IRANGE SELECTION

FV-MODE#	I RANGE	Iout = ±Imax	Iout = 0
0	IR0 to IR5	VEE +4.0 to min of (VCCO – 1.5) or (VCC – 2.5)	VEE + 1.5 to min of (VCCO – 0.15) or (VCC – 1.0)
1	IR0 to IR4	(VEE + 2.0V) to (VCC – 1.5)	VEE + 1.5 to VCC – 1.0
1	IR5	N/A	N/A

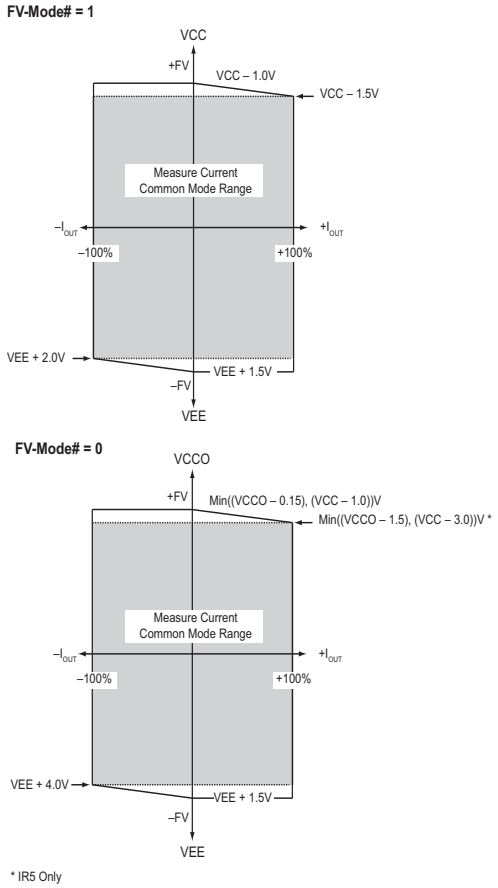


FIGURE 4.

VCCO_#

VCCO_# is the per-channel positive power supply of the output stage for high current operation. In order to minimize power consumption in high current, low voltage applications, VCCO_# should be as low as possible while still maintaining adequate headroom.

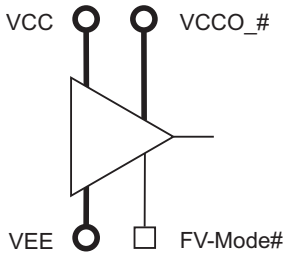


FIGURE 5. EACH DPS CHANNEL HAS A DEDICATED SUPPLY INPUT PIN, VCCO_#

BBIAS

The Vesuvius is a multi-stage output DPS consisting of a low current and a high current stage. Using the CPU port, the BBias# bit can control the turn-on point for the high current output stage. Under normal usage (BBias# = 0), the high current stage will start to automatically turn on when the low current stage reaches between 0.5mA to 1.0mA. With the BBias# bit set high, the second stage is turned on under all conditions. This will lower the AC output impedance, thus improving the load transient response when going from a low current state to a high current stage.

NOTE: The output is virtually glitchless when switching from BBias# = 0 to BBias# = 1 or BBias# = 1 to BBias# = 0 and takes approximately 50µs. Setting BBias# = 1 also adds approximately 3mA to the VCCO# supply per channel.

TABLE 14. BBIAS RECOMMENDED MEASURE CURRENT RANGES

BBias#	Output	Recommended Measure Current Ranges
0	High current stage becomes Active when low current stage reaches 0.5mA to 1.0mA	IR0, IR1, IR2, IR4, IR5
1	High current and low current stage Active at all times	IR3, IR4, IR5

Measure current can be performed in IR4 and IR5 with BBias# set to 0 or 1, although the user should calibrate and measure with the same BBias# setting.

VOLTAGE FEEDBACK OPTIONS

There are multiple voltage feedback nodes to the inverting input of the forcing op amp. The forcing op amp is automatically protected against going open loop when the DPS goes into HiZ. The default condition upon power-up or chip reset is tight loop.

TABLE 15. VOLTAGE FEEDBACK OPTIONS

Tight-Loop*#	DPS-En#	Sel-V-FB#<1:0>	FI/FV*#	Feedback#	Mode
0	X	X	X	VForce#	Tight Loop
X	0	X	X	VForce#	Tight Loop
1	1	00	0	FORCE_#	Local Sense
1	1	01	0	SENSE_#	Remote Sense
1	1	10	0	EXT_SENSE	Calibration
1	1	11	0	N/A	N/A

VOLTAGE RANGE SELECTION

The CPU port may select one of two voltage ranges.

TABLE 16. VOLTAGE RANGE SELECTION

FVR#	VOLTAGE RANGE (V)
0	8
1	16

TABLE 17. 8V RANGE DAC MAPPING

8V RANGE	PROGRAMMED DC LEVEL (V)
0000 Hex	-2
FFFF Hex	+6

NOTE: DAC Resolution = 122µV

TABLE 18. 16V RANGE DAC MAPPING

16V RANGE	PROGRAMMED DC LEVEL (V)
0000 Hex	-2
FFFF Hex	+14

NOTE: DAC Resolution = 244µV

Voltage and Current Clamps

Each channel has current and voltage clamps that limit the amount of current flow (FV mode) or clamp voltage between desired levels (FI mode). In FV mode (FI/FV*# = 0), the current clamps are active, and the current flow is limited internally by reducing the force voltage level until the current is within the programmed levels. There are independent clamps for both sourcing and sinking. The CPU port controls the clamp function.

TABLE 19. VOLTAGE AND CURRENT CLAMPS

FI/FV*#	Cl-En#	CLAMPS	CLAMP LEVELS
0	0	Disabled (Current Clamps)	1.5 x Imax(IR4 or IR5)#/–1.5 x Imax(IR4 or IR5)#
0	1	Enabled (Current Clamps	Cl-Vch-Isrc#/Cl-Vcl-Isnk#
1	N/A	Enabled (Voltage Clamps)	Cl-Vch-Isrc#/Cl-Vcl-Isnk#

Short Circuit Limit

When the current clamps are disabled, the forcing op amp will limit its current flow to 150% Imax of IR4 or 150% of IR5. This selection is made using Sel-MI4#.

Programmable Current Clamps

If the current flow exceeds the clamp limit, the forcing op amp will go into current limit mode.

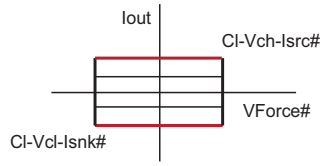


FIGURE 6. CURRENT CLAMP FUNCTIONALITY

The current clamp may be programmed to 150% of the maximum current flow in any range.

TABLE 20. CURRENT CLAMP DAC MAPPING

Cl-Vch-Isrc#<15:0> Cl-Vcl-Isnk#<15:0>	ICLAMP SOURCE	ICLAMP SINK
FFFF	+1.5 • Imax	-1.5 • Imax
•	•	•
8000	+0.75 • Imax	-0.75 • Imax
•	•	•
0000	0µA	0µA

Current Clamp Source

The CPU port selects the signal source for the current clamps.

TABLE 21. CURRENT CLAMP SIGNAL SOURCE SELECTION

Cl-En#	Sel-MI-CL#	Sel-MI4#	Cl#
0	X	0	MI-IR5#
0	X	1	MI-IR4#
X	0	0	MI-IR5#
X	0	1	MI-IR4#
1	1	X	MI-Raw

MI-Raw# is a voltage that tracks current in the selected MI current range.

If Sel-MI-Cl# or Cl-En# = 0, the current clamps will track either MI-IR4# or MI-IR5# regardless of the MI current range. MI-IR4# or MI-IR5# is chosen using Sel-MI4#. This selection is useful when the clamps are used to protect the DUT and the DPS and when the measured current varies over a wide range. The DPS can measure a small current while still being able to source a large current with protection.

If MI-Raw# is selected, the current clamps will track the measure current range. This selection is useful when the clamps need to be programmed to a small value or when the DPS is used as a current source in FI mode.

TABLE 22. CURRENT CLAMP RANGES

CURRENT RANGE	ICLAMP RESOLUTION	±ICLAMP MAX
IR0	58.6pA	±3.84µA
IR1*	586pA	±38.4µA
IR2**	5.86nA	±384µA
IR3	58.6nA	±3.84mA
IR4	586nA	±38.4mA
IR5	11.72µA	±768mA

* IR1 not recommended for use due to stability issues.
** Must use CAP_A when using IR2 (set the Con-Cap# bits to 3).

Programmable Voltage Clamps

When the voltage clamps are enabled, the clamp levels are programmed using the Cl-Vch-Isrc# and Cl-Vcl-Isnk# DACs. These DAC levels are shared by the voltage clamp and current clamp circuits. These DACs require different offset and gain calibration factors depending upon if they are setting the levels for the voltage clamps or current clamps. These calibration factors need to be managed externally to the Vesuvius.

The voltage clamp circuit compares the output of the measurement unit to the Cl-Vch-Isrc# and Cl-Vcl-Isnk# DAC levels. When the measurement unit output exceeds these threshold levels, a voltage clamping event occurs.

The measurement unit has 3 programmable voltage ranges, so the clamp level DAC code will need to be adjusted as a function of which measurement range is selected (measurement range is controlled by the MUR <1:0> bits). Please see Table 29 in this datasheet in order to determine the voltage range associated with each setting of the MUR<1:0> bits.

The DAC code to programmed DC level transfer functions can be calculated for the Voltage Clamp High and Voltage Clamp Low using Table 23 and Table 24 below.

NOTE: Functionality is only guaranteed for MUR#<1:0> = 3(16V range)

TABLE 23. VOLTAGE CLAMP HIGH DAC MAPPING (MUR#<1:0> = 3 (16V range))

Cl-Vch-Isrc##<15:0>	PROGRAMMED DC LEVEL (V)
FFFF Hex	+25.2V
0000 Hex	-8.4V
Note: The above DC levels are outside the voltage supply range of Vesuvius but are the values used to calculate a code to voltage transfer function.	

TABLE 24. VOLTAGE CLAMP LOW DAC MAPPING (MUR#<1:0> = 3 (16V range))

Cl-Vcl-Isnk##<15:0>	PROGRAMMED DC LEVEL (V)
FFFF Hex	-13.13V
0000 Hex	+19.57V
Note: The above DC levels are outside the voltage supply range of Vesuvius but are the values used to calculate a code to voltage transfer function.	

TABLE 25. VOLTAGE CLAMP OFFSET ADJUSTMENT RANGE (MUR#<1:0> = 3 (16V range))

CODE	VALUE
OFFSET	
0000H	-2V
7FFFH	0
FFFFH	+2V

Force Current

There are two ways to create a programmable current using the Vesuvius:

1. Using current clamps
2. Using MI feedback to the FORCE amplifier.

METHOD 1: USING CURRENT CLAMPS TO CREATE FI

Force Current mode is implemented by placing the part in Force Voltage mode and using the current clamps to set the Force Current value supplied to the DUT. In this situation, the Force Voltage output level is used as a voltage clamp level and protects the DUT from an over-voltage situation.

To configure in Force Current mode, perform the following:

- Disable Vesuvius (put in HiZ)
- Enable current clamps and set Current Clamp Level to Force Current required
- Set the Force Voltage level to the ground reference of the DUT
- Place the part in Force Voltage mode
- Connect Force Output to DUT
- Enable Vesuvius
- Place the part in Force Voltage mode
- Set Force Voltage Level to the Voltage Clamp Level required. This wil allow current to flow, which will be limited by the current clamps.

METHOD 2: USING MI FEEDBACK

An alternative method for using Vesuvius to provide a programmable current is to feedback the output of the MI instrumentation amplifier to the forcing amplifier. This method provides traditional FI functionality and improved force current accuracy vs. method 1.

When using method 2, the programmable output current, Iout_#, is controlled by the ForceA#, ForceB#, or Central-Level DAC as determined by the setting of the Sel-FV#<1:0> bits. To configure a channel for FI mode, set DPS-EN# = 1, Tight-Loop*# = 1, and FI/FV*# = 1. This will establish a feedback path where MI-Raw# is fed back to the force amplifier. Under this condition, ±Imax is determined by the current measurement range that is selected using the IR#<5:0> bits. Programmable current is mapped as shown in Table 26.

TABLE 26.

DAC Code	Iout_#
FFFF	+Imax (Sourcing)
0000	–Imax (Sinking)

To configure in Force Current mode using MI feedback, perform the following:

- Disable Vesuvius (put in HiZ)
- Put in force voltage mode (FI/FV=0)
- Put the part in tight loop (Tight-Loop*=0)
- Set ForceA to be used as the forcing DAC level
- Set the current range.
- Program compensation network as needed.
- Measure the voltage on the FORCE pin that will be connected to using the Monitor Measure voltage path.
  - Program this measured voltage into the ForceA RAM location

  Or
  - Set the ForceA RAM voltage level to the ground reference of the DUT
- Connect FORCE_# to SENSE_# (Con-FS#=1)
- Sel-MU-POS# = FORCE
- Sel-MU-Neg# = GND
- Sel-MUR# = 16V
- Set the ForceB RAM location to hex value 0x7FFF. This equates to 0 current.
- Set the Clamp RAM locations to the desired value for voltage clamps desired.
- Enable Vesuvius
- Set Tight-Loop*= 1. This will change the feedback from tight loop.
- Change to FI mode/Set ForceB to be the forcing DAC level. These two write registers should be performed during the same register write. Both registers are located at address 0.
- Program ForceB to desired current.

ForceA and ForceB can be interchanged in this setup.

Ganging

Individual DPS units may be ganged with sequential channels in a chain. The first DPS in the string is the master DPS. All subsequent DPS channels are slave units.

To create a high current DPS in FV mode the following steps are taken:

- Select a master DPS and place it in FV mode
- Connect the Gang# signal of the master channel to the input of all slave channels.

NOTE: Connection resistance should be minimized for best AC response.

Master DPS:

- Sel-VForce# = 0 (FV Mode)
- Sel-G#-Out = 0 (Master unit Gang# signal as forcing value)
- All Subsequent Slave Units:
  - Sel-G#-Out = 1 (Master unit Gang# signal as forcing value)
  - Sel-VForce# = 1 (Gang Mode)

NOTE: When ganging from an odd numbered channel to an even numbered channel, an external connection needs to be made as shown in Figure 8.

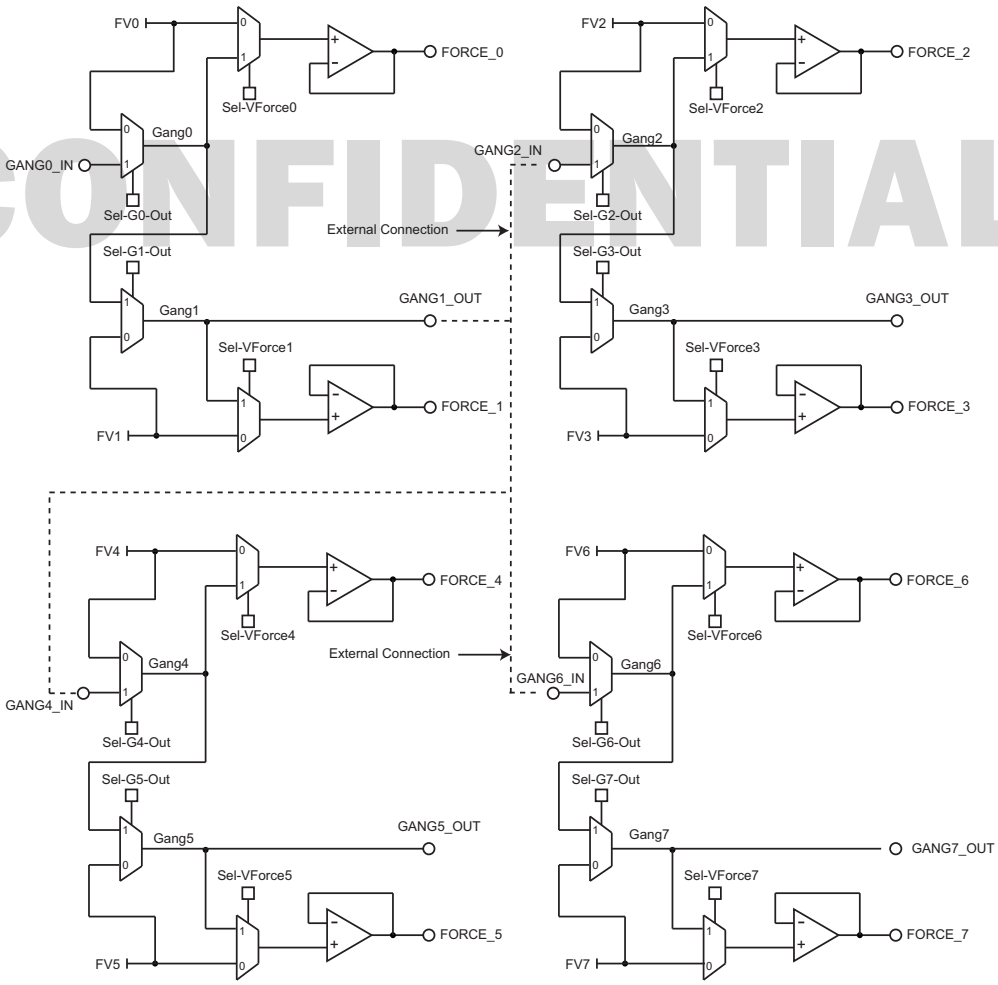


FIGURE 7. GANGING WITH ONE CHIP

Serial Chip-to-Chip Ganging

Ganged DPS strings may extend across multiple chips by connecting the GANG#_OUT pin of one chip to the GANG#_IN pin of the next chip in the chain.

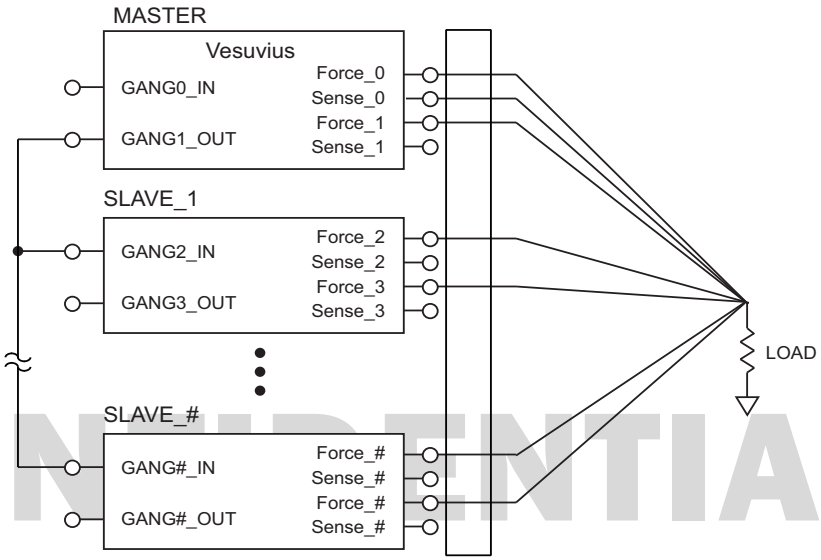


FIGURE 8. GANGING ACROSS MULTIPLE VESUVIUS'

Measurement Unit

There is a per-channel and central measurement unit per chip that can track:

- The voltage at FORCE_#
- The voltage at SENSE_#
- The current at FORCE_#
- An internal diagnostic node

The measurement unit output is a voltage that is proportional to the current or voltage of the selected channel.

Measurement Unit Input Sources

Each channel generates a differential analog signal and sends it to the measurement unit. The positive and negative inputs may be selected from several potential sources.

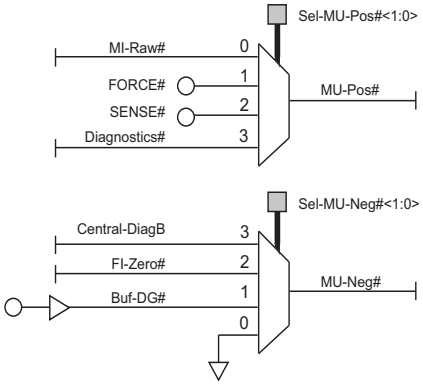


FIGURE 9. MEASUREMENT UNIT

TABLE 27. MEASUREMENT UNIT MODES

	MU-POS#	MU-NEG#	MODE
Sel-MU-Pos#<1:0>			
00	MI-Raw#		MI
01	FORCE_#		MV
10	SENSE_#		MV
11	Diagnostics#		Test & Cal
Sel-MU-Neg#<1:0>			
00		Chip Ground	Diagnostics
01		Buf-DG#	MV
10		FI-Zero#	MI
11		Central-Diag-B	Diagnostics

Measurement Unit Source Selection

The CPU port selects the channel to be used as the input to the measurement unit.

TABLE 28. MEASUREMENT UNIT SOURCE SELECTION

Sel-MU<2:0>	Central-MU
000	MU-Pos0 – MU-Neg0
001	MU-Pos1 – MU-Neg1
010	MU-Pos2 – MU-Neg2
011	MU-Pos3 – MU-Neg3
100	MU-Pos4 – MU-Neg4
101	MU-Pos5 – MU-Neg5
110	MU-Pos6 – MU-Neg6
111	MU-Pos7 – MU-Neg7

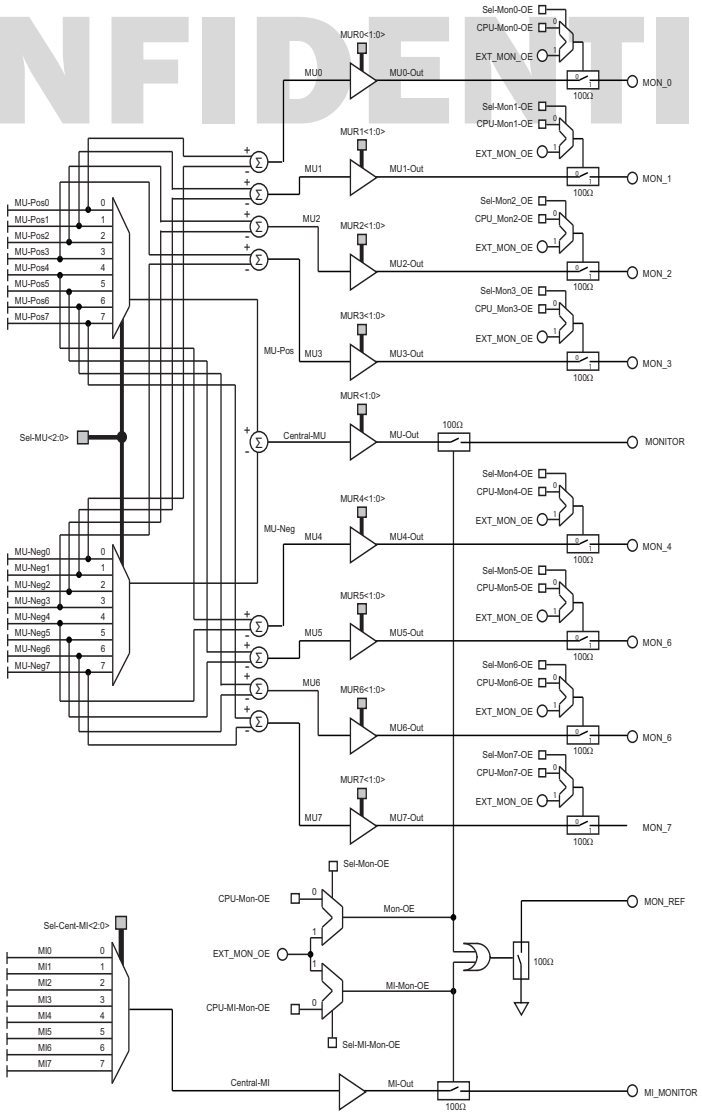


FIGURE 10. MEASUREMENT UNIT TO MONITOR ROUTING

Measure Voltage

The CPU port selects one of three MV ranges or the MI range.

TABLE 29. MV MAPPING

MUR<1:0>	00	01	10	11
Mode	MI	MV	MV	MV
VRange	N/A	4V	8V	16V
Input Range	±1.5 • Imax	0V/+4V	-2V/+6V	-2V/+14V
Monitor	1.5 ±0.8V	+0.5V/+2.5V	+0.5V/+2.5V	+0.5V/+2.5V
Av	1.3	0.5	0.25	0.125
Vos	1.5V	+0.5V	+1.0V	+0.75V

The MV ranges are designed to map the input voltage span to a 1.5V ±1V output voltage at the monitor. This mapping is useful when connecting to an external low voltage, positive input only ADC.

The central monitor has the transfer function:

MONITOR = Av • Central-MU + Vos

The per-pin monitors have the transfer function:

MONITOR = Av • MU# + Vos

Measure Current

The DPS supports 6 current ranges per channel, capable of measuring current accurately over the following common mode voltage range, VCM.

FV mode# = 0 (VEE + 3V) .≤ (VCCO – 1.5V)

FV mode# = 1 (VEE + 2V) ≤ (VCC – 1.5V)

TABLE 30. MI MAPPING

RANGE	IR#<5:0>	IMAX
IR0	000001	±2.56µA
IR1	000010	±25.6µA
IR2	000100	±256µA
IR3	001000	±2.56mA
IR4	010000	±25.6mA
IR5	100000	±512mA

The current sense line has the following transfer function.

TABLE 31. MI TRANSFER CHARACTERISTIC

IOUT#	MI-Raw#
+1.5 • Imax	+2.3V
+Imax	+2.033V
0	+1.5V (FI-Zero#)
-Imax	+0.967V
-1.5 • Imax	+0.7V

FI-Zero# is a per-channel DC reference voltage that corresponds to 0 current flow at the FORCE_# pin. MI-Raw# is a voltage that tracks the current in any given range. The current may exceed ±Imax and MI-Raw# will continue to track the current flow until the signal eventually saturates and will no longer accurately track the current flow.

To measure current for the region –10% to +10% of Imax in IR4 and IR5, switching to the next lower current range is recommended. This will provide the best MI performance.

Changing Current Ranges

When measuring current in the highest 5 ranges (IR1 – IR5) the forcing op amp does not react to changing the current range. Changing current ranges in between these selections will not cause any glitch or disturbance at the force output pin.

A small disturbance may be present at the output when changing ranges into or out of IR0.

CME (Common Mode Error) Calibration

The current measure (MI) transfer function will have some small amount of common mode voltage error as the FORCE output varies. Each current range on each channel has its own independent CME adjust code that is automatically selected by the current range selection.

TABLE 32. COMMON MODE ERROR ADJUSTMENT

FV-MODE#	IR#<5:0>	CME-Adj#<7:0>
X	000001	CME-Adj0#<7:0>
X	000010	CME-Adj1#<7:0>
X	000100	CME-Adj2#<7:0>
0	001000	CME-LAdj3#<7:0>
1	001000	CME-HAdj3#<7:0>
0	010000	CME-LAdj4#<7:0>
1	010000	CME-HAdj4#<7:0>
0	100000	CME-Adj5#<7:0>

The CME gain correction is superimposed on the nominal pre-calibration CME error in an effort to cancel each other out.

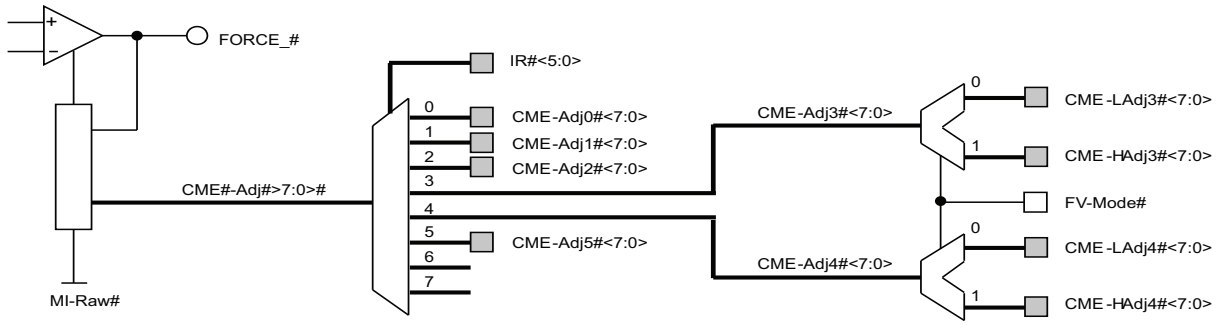


FIGURE 11. COMMON MODE ERROR CORRECTION CIRCUIT

IR3 and IR4

There are two separate ranges for IR3 and IR4; one for high current (FV-Mode = 0) and one for low current (FV-Mode = 1). Each range requires its own CME and MI calibration.

TABLE 33. COMMON MODE ERROR ADJUST RANGE

CME-ADJ#<7> (PARITY)	CME-ADJ#<6:0> (CODE)	CME ADJUSTMENT
0	1111111	1.0082677
0	1111110	1.0082026
•	•	•
0	0000010	1.0001302
0	0000001	1.0000651
0	0000000	1.0000
1	0000000	1.0000
1	0000001	0.9999349
1	0000010	0.9998698
•	•	•
1	1111110	0.9917974
1	1111111	0.9917323

NOTE: Resolution = 0.00651%/V (of Full Scale Current Range)

The default state is 00 Hex, which results in no CME calibration. By setting CME-Adj#<7:0> correctly, the actual transfer function can more closely track the ideal transfer function.

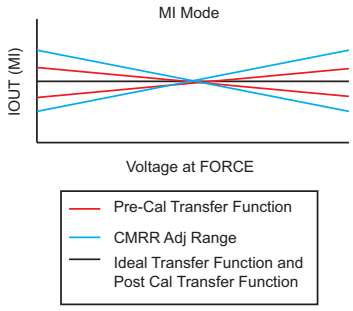


FIGURE 12. COMMON MODE ERROR ADJUSTMENT

Monitor Output Current Limiting

The monitor output is designed to mate directly with an ADC. To prevent damage to the ADC in cases where the monitor voltage exceeds in the input compliance of the ADC the monitor output current is limited to ~20mA.

Monitor High Impedance

The MONITOR output pin may be placed in a HiZ state where it maintains an extremely low leakage between GND and VDD. HiZ is useful to support the ganging of multiple MONITOR pins all connecting to the same external ADC.

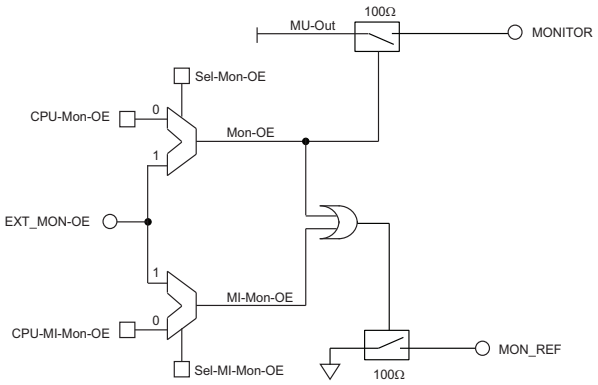


FIGURE 13. MONITOR CIRCUIT

TABLE 34. MONITOR FUNCTIONALITY

Mon-OE	MONITOR
0	HiZ
1	MU-Out

Monitor output enable may be controlled by the CPU port or by a real time monitor output enable pin.

TABLE 35. MONITOR CONTROL

Sel-Mon-OE	Mon-OE
0	CPU-Mon-OE
1	EXT_MON_OE

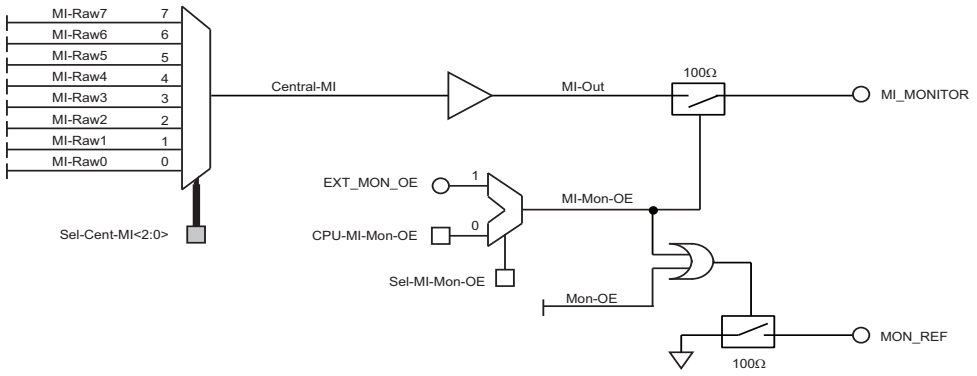


FIGURE 14. CENTRAL MONITOR CIRCUIT

Monitor Reference

MONITOR is always with respect to chip ground. MON_REF is the local chip ground and can be used as the reference signal if the ADC is far away and its ground level is not stable relative to the chip ground.

MON_REF is active whenever the MONITOR is active.

TABLE 36. MONITOR REFERENCE

MI-Mon-OE	Mon-OE	MON_REF
0	0	HiZ
X	1	Active
1	X	Active

Measurement Current Monitor

There is a low voltage central monitor dedicated to the measure current function. The measure current monitor can be used in conjunction with the general-purpose monitor to capture both the voltage and the current at any channel simultaneously.

The CPU selects the source.

TABLE 37. CENTRAL MONITOR SELECTION

Sel-Cent-MI<2:0>	Central-MI
000	MI0
001	MI1
010	MI2
011	MI3
100	MI4
101	MI5
110	MI6
111	MI7

MI Monitor High Impedance

The MI_MONITOR output pin may be placed in a HiZ state where it maintains an extremely low leakage between the VDD and GND. HiZ is useful to support the ganging of multiple MI_MONITOR pins all connecting to the same external ADC.

FIGURE 15. MONITOR HiZ CURRENT

TABLE 38. MI_MONITOR FUNCTIONALITY

MI-Mon-OE	MI_MONITOR
0	HiZ
1	MI-Out

The measure current monitor output enable may be controlled by the CPU port or by a real time monitor output enable pin.

TABLE 39. MI_MONITOR CONTROL

Sel-MI-Mon-OE	MI-Mon-OE
0	CPU-MI-Mon-OE
1	EXT_MON_OE

MI Monitor Reference

MI_MONITOR is always with respect to chip ground. MON_REF is the local chip ground and can be used as the reference signal if the ADC is far away and its ground level is not stable relative to the chip ground.

MON_REF is active whenever the MONITOR is active.

TABLE 40. MI_MONITOR REFERENCE FUNCTIONALITY

MI-Mon-OE	Mon-OE	MON_REF
0	0	HiZ
X	1	Active
1	X	Active

External Force and Sense

There are external force and external sense pins that bypass the DPS completely and provide direct access to the FORCE and SENSE pins, which is useful for:

- Connecting an external PMU to the DUT
- Direct measurement of the DUT voltage
- DC Calibration

EXT_FORCE

Each channel may be connected to the EXT_FORCE pin through an on-chip switch.

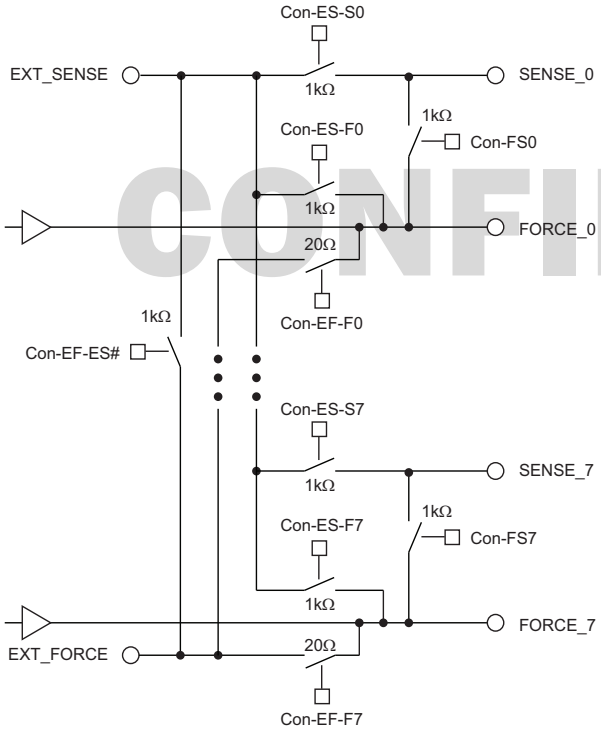


FIGURE 16. EXTERNAL FORCE/SENSE CIRCUITRY

TABLE 41. EXTERNAL FORCE-TO-FORCE SWITCH FUNCTIONALITY

Con-EF-F#	EXT_FORCE to FORCE_#
0	Disconnected
1	Connected

EXT_SENSE

Each channel may have its FORCE_# or SENSE_# pin connected to the EXT_SENSE pin.

TABLE 42. EXTERNAL SENSE-TO-FORCE SWITCH FUNCTIONALITY

Con-ES-F#	EXT_SENSE TO FORCE_#
0	Disconnected
1	Connected

TABLE 43. EXTERNAL SOURCE-TO-SENSE SWITCH FUNCTIONALITY

Con-ES-S#	EXT_SENSE TO SENSE_#
0	Disconnected
1	Connected

EXT_FORCE/EXT_SENSE SWITCH

The CPU port can connect EXT_FORCE and EXT_SENSE together. This connection may be useful for calibration.

TABLE 44. EXTERNAL FORCE TO EXTERNAL SENSE SWITCH FUNCTIONALITY

Con-EF-ES	EXT_FORCE to EXT_SENSE
0	Disconnected
1	Connected

Force/Sense Connect Switch

The CPU port can connect the force and sense pins via an on-chip switch. This connection may be useful for calibration.

TABLE 45. FORCE-TO-SENSE WITCH FUNCTIONALITY

Con-FS#	FORCE_# to SENSE_#
0	Disconnected
1	Connected

Programmable Compensation Network

In order to be stable over a wide range of load conditions, a compensation network is available for each channels output forcing op-amp. The network is shown in Figure 18, and the connections are controlled by the CPU port. The compensation network is not limited to the internal resistor/capacitor network shown, but can be expanded by connecting either an external component or an external network to the CAP_A_# pin.

TABLE 46. COMPENSATION NETWORK VALUES

Component	Value
Cmin	29pF
Con-Cap#<0>	58pF
Con-Cap#<1>	123pF
Con-Cap#<2>	142pF
Con-Res*#<0>	500Ω
Con-Res#<1>	10kΩ
Con-Res#<2>	30kΩ
Con-Res#<3>	90kΩ

The maximum capacitance for which the DPS remains unconditionally stable may be set with the compensation network using both internal and external components. Using the CPU port, the user can connect the compensation network for large capacitance load applications and disconnect it for small load applications. There is a trade-off between stability and transient response performance. The larger the compensation capacitors, the more stable the DPS will be. However, the response and settling times will be slower.

The values of resistor/capacitors components can also be chosen to add a zero to the output transfer function of the main forcing op-amp in order to cancel the dominant output pole created by the load capacitance on the FORCE_# pin and internal resistance of the part. The poles created by several typical bypass capacitors (100nF, 1µF, and 10µF) are used as an example below. After the poles frequencies are calculated, a zero can be introduced based on configuration of the compensation network.

Calculation of Output Poles for Typical Bypass Capacitors

To calculate the output pole the following equation was used:
Pole = 1 / (2*π*R*C)

R = Internal resistance of forcing op-amp (assumed to be 3Ω)

C = Load capacitance at FORCE_# pin

TABLE 47. CALCULATED OUTPUT POLE LOCATIONS

Load Capacitance on FORCE_#	Output Pole (kHz)
100nF	531
1µF	53
10µF	5.3

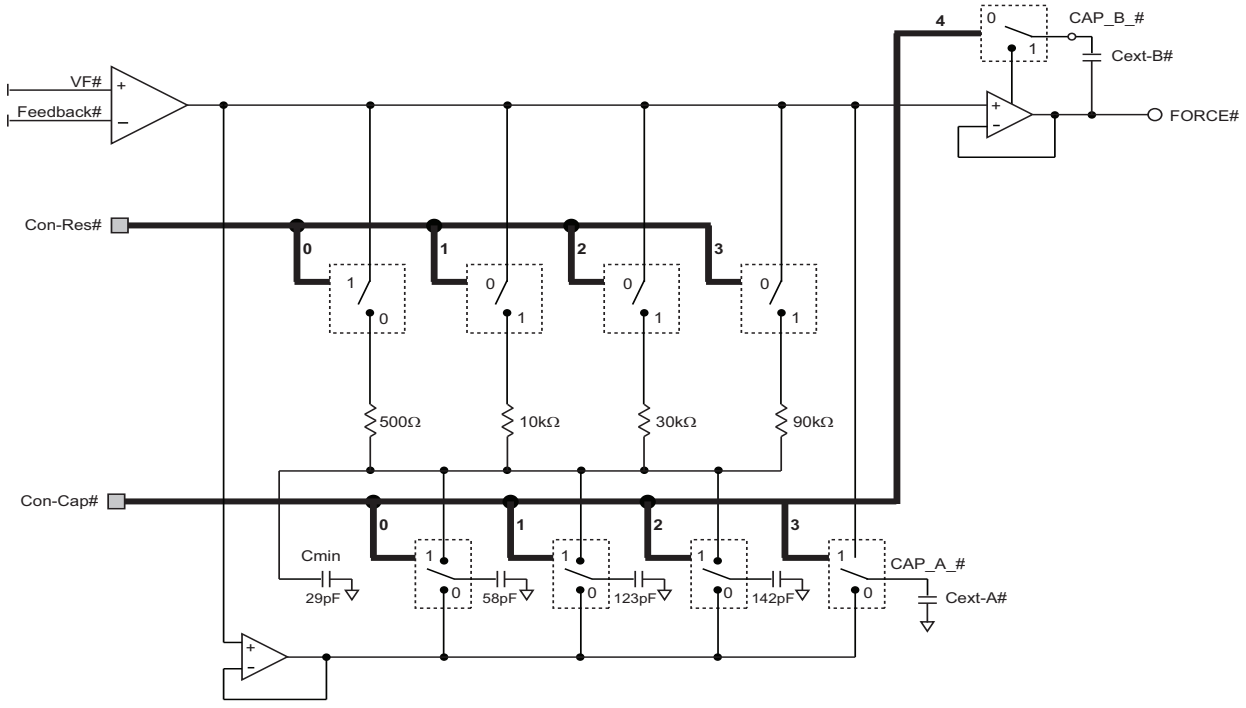


FIGURE 17. PER CHANNEL PROGRAMMABLE COMPENSATION NETWORK

Note: The Con-Res*#<0> bit is active low and therefore to connect this resistor, the bit should be set low. This will ensure that a resistor is connected following a reset.

After calculating the output pole frequency, the user can use the following equation to select the desired compensation network combination to add a zero.

Calculation of Zeros based on Internal Capacitors and Resistors

To calculate zero locations, the following equation was used: Zero = 1 / (2*π*R*C)

R = Total internal compensation resistance chosen using Con-Res#

C = Total internal compensation capacitance chosen using Con-Cap#

Using the example of 100nF in Table 47, an output pole of 531 kHz exists. The user would then search for this frequency in Table 48. Based on this frequency, a combination of Con-Cap#<2:0>=0x0 and Con-Res#<3:0> = 0x3 which gives a frequency of 549 kHz, would be chosen. As noted earlier, Table 48 can be expanded with other combinations of components to meet specific needs.

All capacitor connection switches may be opened and closed independently. The addition of a Cext-B# capacitor to the CAP_B_# pin is recommended to improve transient performance in the current range IR0. for stability, CAP_B_# ≥ Cload/10.

The typical external compensation capacitor value is:

Cext-A# = 4.7nF

Cext-B# = 100nF

However, different capacitor values can be used to trade off stability under a capacitive load vs. settling time.

There is an internal buffer to pre-charge all unconnected compensation capacitors to the Force Voltage output level. This facilitates switching compensation settings with minimal disturbance to the output voltage.

TABLE 48. ZERO LOCATIONS BASED ON INTERNAL CAPACITORS AND RESISTORS (kHz)

Con-Cap#<2>	Con-Cap#<1>	Con-Cap#<0>	Sum of Con-Cap# Capacitors Ccomp(pF)	Con-Res*#<0>=1 Con-Res#<1>=0 Con-Res#<2>=0 Con-Res#<3>=0	Con-Res*#<0>=1 Con-Res#<1>=1 Con-Res#<2>=0 Con-Res#<3>=0	Con-Res*#<0>=1 Con-Res#<1>=0 Con-Res#<2>=1 Con-Res#<3>=0	Con-Res*#<0>=1 Con-Res#<1>=0 Con-Res#<2>=0 Con-Res#<3>=1
0	0	0	29	10982	549	183	61
0	0	1	87	3661	183	61	20
0	1	0	152	1095	105	35	12
0	1	1	210	1517	76	25	8
1	0	0	171	1862	93	31	10
1	0	1	229	1391	70	23	8
1	1	0	294	1083	54	18	6
1	1	1	352	905	45	15	5

NOTE: Ccomp = sum of selected Con-Cap# capacitors. The table above calculates a zero for only one internal resistor selected at a time and using only internal capacitors. Resistors can all be chosen in parallel and external components can be used to add almost endless possibilities to zero locations.

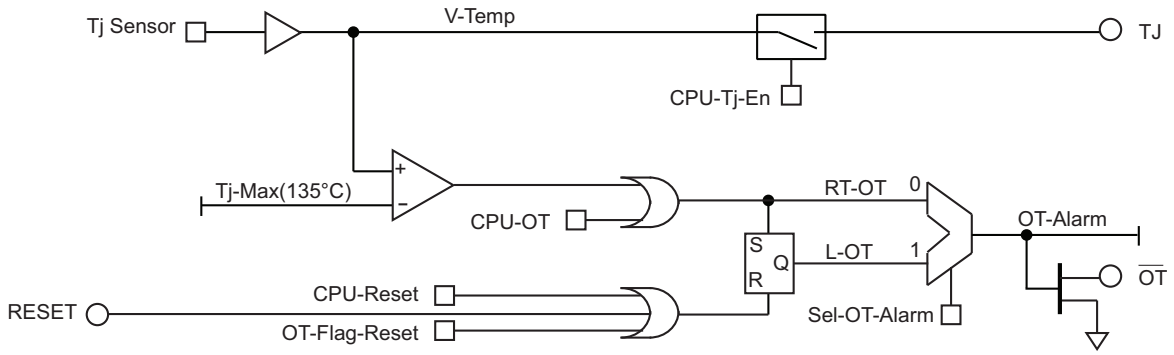


FIGURE 18. OVER-TEMPERATURE ALARM AND THERMAL MONITOR CIRCUITRY

Over-temperature Protection

An on-chip thermal monitor allows the chip to protect itself from an over temperature situation. An on-chip reference establishes the threshold for the over-temperature comparator.

TABLE 49. THERMAL MONITOR FUNCTIONALITY

INPUT CONDITION	OUTPUT CONDITION
V-Temp < Tj-Max (+135°C)	Normal Operation
V-Temp > Tj-Max (+135°C)	OT Fault

Over-temperature Alarm

$\overline{OT}$ is an open drain output that indicates when the junction temperature exceeds +135°C. The CPU port can also directly force the over temperature flag to be active.

The over-temperature alarm can be latched or real time..

TABLE 50. OVER-TEMPERATURE ALARM FUNCTIONALITY

CPU-OT	JUNCTION TEMPERATURE	RT-OT
0	V-Temp < Tj-Max (+135°C)	0
0	V-Temp > Tj-Max (+135°C)	1
1	X	1

TABLE 51. OVER-TEMPERATURE ALARM MODES

Sel-OT-Alarm	OT-Alarm	MODE
0	RT-OT	Real Time
1	L-OT	Latched

Sel-OT-Alarm is a programmable bit that sets the alarm configuration for all channels. Its functionality is described in Table 51.

Once L-OT is set, it will remain high until cleared by the CPU port or a chip level reset. OT-Flag-Reset and CPU-Reset are write only transactions that generate a one-shot pulse and may not be read back. RT-OT and L-OT may be read back by the CPU port.

TABLE 52. OVER-TEMPERATURE ALARM INDICATOR

OT-Alarm	$\overline{OT}$
0	1 (HiZ)
1	0 (Active - 100Ω to ground)

OT-Alarm is a global indicator bit that activates when any channel exceeds the over-temperature threshold. Individual channels can then be polled to identify which channel(s) are over-temperature.

CPU-OT-DIS is a programmable bit that can be used to disable the global over-temperature alarm when it is programmed to logic “1”. This bit should be programmed to logic “0” when using the global over-temperature alarm.

Temperature Monitor

TJ is a voltage output that tracks the junction temperature.

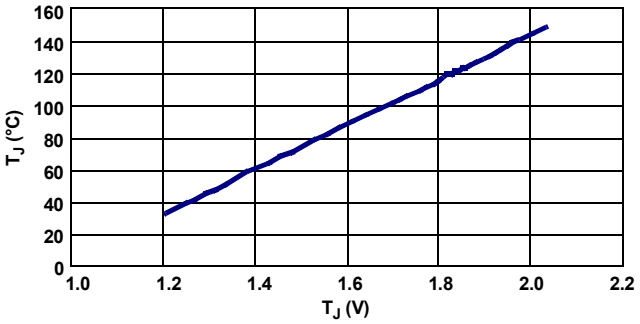


FIGURE 19. THERMAL MONITOR VOLTAGE TO TEMPERATURE MAPPING

TJ has HiZ capability under CPU port control.

TABLE 53. THERMAL MONITOR PIN MODES

CPU-TJ-En	TJ
0	HiZ
1	V-Temp

Clamp Alarm

The CPU port controls the current alarm circuitry.

TABLE 54. OVER-CURRENT ALARM FUNCTIONALITY

CI-AI-En#	Alarm Status
0	Alarm Disabled
1	Alarm Enabled

The clamp alarms can be enabled independently from the current clamps, even though they share a common CI# input and common threshold values.

The current alarm can be latched or be a real time signal.

TABLE 55. OVER-CURRENT ALARM MODES

Sel-CI-AI#	CI-Alarm#
0	RT-CI#
1	L-CI#

Once latched, the alarm remains high until cleared by the CPU port or a chip level reset. CI-Reset# and CPU-Reset are write only transactions that generate a one-shot pulse and cannot be read back through the CPU port.

Clamp Alarm Readback

L-OV-Vch/OI-Src#, L-OV-Vcl/OI-Snk#, RT-OI-Src# and RT-OI-Snk# may be read back through the CPU port.

Current Clamps vs Current Alarms

The current clamps are used for a variety of functions.

1. Protect the DPS

The current clamps protect the DPS when it faces a short circuit or an overcurrent situation.

2. Protect the DUT

The current clamps protect the DUT from excessive current flow.

3. FI Mode

The current clamps are used to support FI mode.

Current Alarms are used to identify an overcurrent situation and raise a flag. That flag may be used to place the DPS in HiZ or may be ignored.

There are 3 possible configurations for the current clamps and alarms:

1. Clamps and alarm off
2. Clamps on and alarm off
3. Clamps and alarm on

It is NOT possible to have the alarms active and the clamps off.

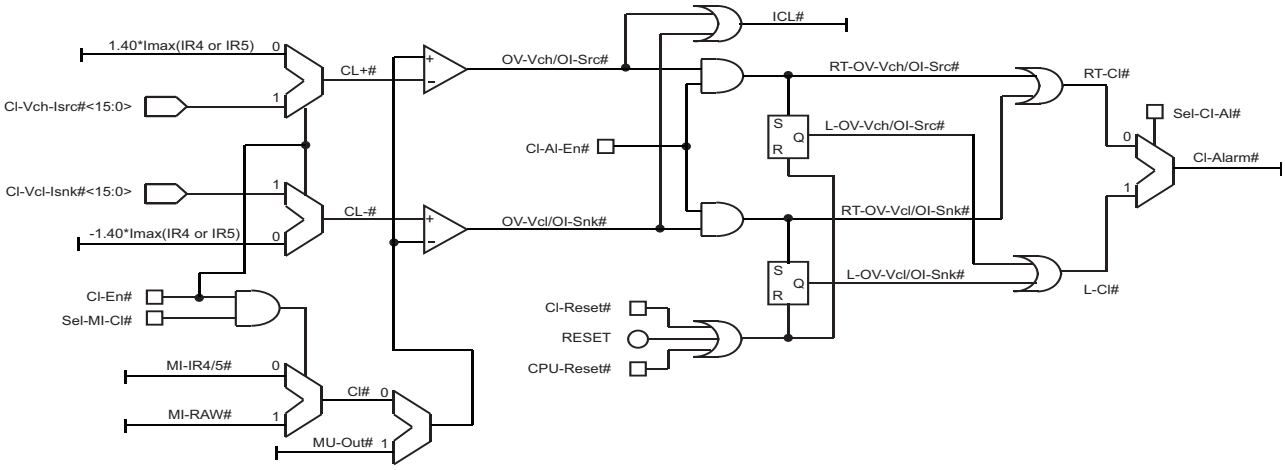


FIGURE 20. OVER-CURRENT/VOLTAGE ALARM STATUS VOLTAGE CLAMP ALARM CIRCUITRY

Kelvin Alarm

Each channel has its own independent Kelvin Alarm detector to guarantee that a proper sense path is connected to the forcing op amp. The CPU selects the voltage difference between the force and sense pins that define a Kelvin connection.

TABLE 56. KELVIN ALARM THRESHOLDS

Kelvin-Th#<3:0>	Kel-Thresh#±
0000	±175mV
0001	±350mV
•	•
1110	±2.625V
1111	±2.8V
Resolution	175mV

When the difference between the force and sense pins exceeds the threshold, a Kelvin fault state is detected.

TABLE 57. KELVIN FAULT STATE INDICATORS

LOOP CONDITION	Kelvin-Fault#
FORCE_# - SENSE_# > Kel-Thresh+	1
FORCE_# - SENSE_# < Kel-Thresh-	1
Kel-Thresh- < FORCE_# - SENSE_# and FORCE_# - SENSE_# < Kel-Thresh+	0

A real time Kelvin alarm is signaled when an open loop condition occurs when the DPS is enabled. The alarm turn on time will be filtered to avoid potential glitches and false alarms when the op amp comes into and goes out of HiZ.

TABLE 58. REAL-TIME KELVIN ALARM FUNCTIONALITY

Kelvin-Fault#	DPS-En#	RT-Kel-Al#
0	X	0
X	0	0
1	1	1

Any occurrence of a Kelvin alarm is captured by the latched Kelvin alarm signal. The CPU port selects the source of the channel Kelvin alarm. Kel-Al# and L-Kel-Al# may be read back through the CPU port.

TABLE 59. KELVIN ALARM INDICATOR FUNCTIONALITY

Sel-Kel-Al#	Kel-Al#
0	RT-Kel-Al#
1	L-Kel-Al#

Once a Kelvin alarm has been latched, it remains latched until cleared by the CPU port or a chip level reset. CPU-Reset and Kel-Al-Reset# are write only transactions that generate a one-shot pulse and therefore cannot be read back.

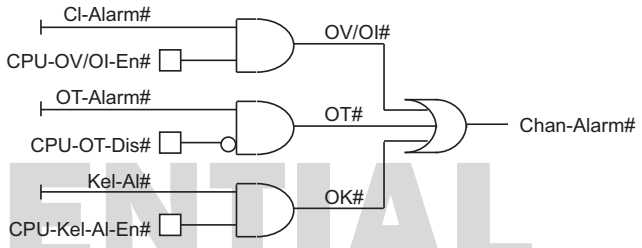


FIGURE 21.

Chip Alarm

The ALARM* pin indicates that an over temperature, over current or Kelvin alarm has occurred.

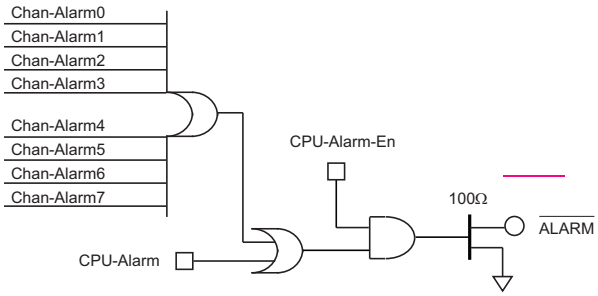


FIGURE 23. CHIP ALARM CIRCUITRY

$\overline{\text{ALARM}}$ may be gated off or forced active by the CPU port.

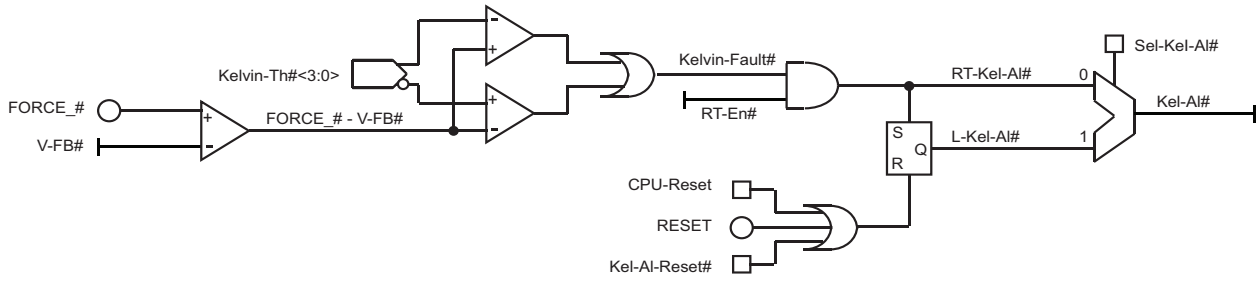


FIGURE 22. OVER-CURRENT/ALARM STATUS AND KELVIN ALARM CIRCUITRY

TABLE 60. CHIP ALARM FUNCTIONALITY

CPU-ALARM	CPU-ALARM-EN	CHAN-ALARM#	$\overline{\text{ALARM}}$
1	1	X	0 (Active)
X	0	X	1 (HiZ)
0	1	0	1 (HiZ)
X	1	1	0 (Active)

$\overline{\text{ALARM}}$ is an open drain active low output that pulls current when active.

Diagnostics

Each channel has access to internal per-channel nodes for diagnostic support.

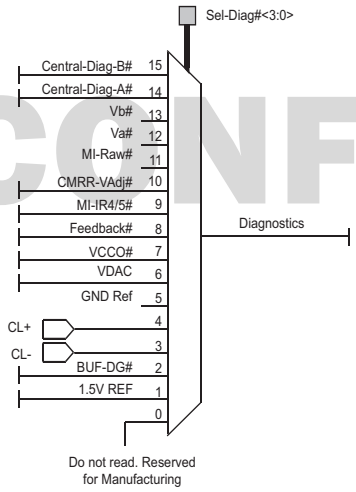


FIGURE 24. DIAGNOSTIC CIRCUITRY

The central diagnostic nodes are routed out to the individual channels with each channel having up to 2 central nodes.

TABLE 61. DIAGNOSTIC MUX CONNECTIONS

CHANNEL	Central-Diag-A	Central-Diag-B
0	N/A	N/A
1	Central-Level+	Central-Level–
2	V1	V2
3	VDD	GND
4	VCC/2	VEE/2
5	VDD	GND
6	GND	V-Temp
7	DAC_P	DAC_N

DAC_P and DAC_N are per-chip internal differential voltages used by the Sample and Hold circuitry to set the DAC levels.

MI_Raw# is a voltage that tracks current in the selected current range and is used as an input to the comparator for the current clamp and current alarm features.

Temperature Sensing

The Vesuvius has its own independent temperature sense capability.

A global temperature sensor, along with per channel temperature sensors, are available. All sensors behave in a similar manner, and TJ can be calculated with the equation below. The per channel temperature sensors are physically located in the measure current circuit. This is because they are meant to be used for MI tempco correction.

Global Temperature: There are two internal voltages

1. V1
2. V2

which, when measured, may be used to calculate the junction temperature as expressed in the equation:

$$Tj[c] = \{(V2 - V1) \cdot 1987\} - 267$$

Per Channel Temperature: There are two internal voltages

1. Va
2. Vb

which, when measured, may be used to calculate the junction temperature as expressed in the equation:

$$Tj[c] = \{(Va - Vb) \cdot 1880\} - 260$$

Below is an example showing the process for calibrating the MI (Measure Current) Tempco:

1. Calculate Offset TempCo: Measure current with no load (using the MONITOR or MI_MONITOR path) and the Tj on a particular channel with the Vesuvius in thermal equilibrium. Next, load an ADJACENT channel with a current load which will cause the temperature of the channel being calibrated to change. Wait for thermal equilibrium and again measure the current with no load and the Tj of the channel. ΔTj can now be calculated and can be used to correct the MI offset change due to local channel temperature change.
2. Calculate Gain Tempco: Two different load currents (calibration points) are needed for the channel being calibrated. The loading on the ADJACENT channel can be changed to give measurements at two cal points with the same Tj value for both. Then change the ADJACENT channel loading to product a different Tj and repeat the measurements at the two cal points. This will permit calculating a gain Tempco.

Required Off-Chip Components

A precision voltage reference level and external resistor is required per chip. In addition, each channel may require external capacitors in order to support CPU selectable stability under different capacitive loads.

There may be a need for decoupling capacitors on the power supply pins. The need for decoupling capacitors is dependent upon the particular application, and is therefore system dependent.

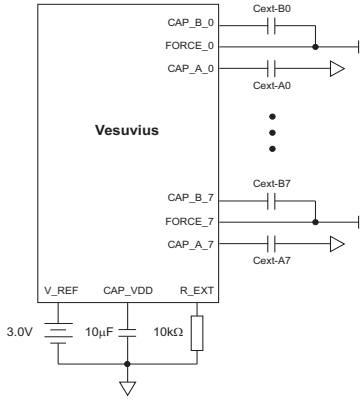


FIGURE 25. EXTERNAL COMPONENT CONNECTIONS

V_REF

V_REF is an analog input voltage that is used to program the on-chip DC levels. V_REF should be held at +3.0V with respect to GND. There is one V_REF pin shared by all channels on the same chip.

V_REF SENSITIVITY

The previous equations that predict the DAC output assume that V_REF = 3.000V. Any variation in V_REF at the input pin will affect the Level by a 1:1 ratio before being multiplied by the gain.

Offset adjust has ample range to correct for deviations in V_REF. As long as V_REF is held stable after calibration, any deviation in V_REF from 3.0V will not affect DC accuracy.

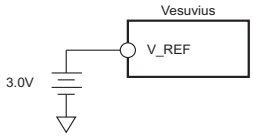


FIGURE 26. EXTERNAL VOLTAGE REFERENCE

Device Under Test Ground

The DUT-GND_# pin is a per channel ground reference input that provides a means of tracking the ground level at the DUT and making additional voltage offsets inside the chip so that the voltage levels generated on-chip are with respect to the ground level at the DUT.

BUF_DG# is the internal buffered version of DUT_GND#.

DUT_GND_# is NOT added into the DC level when forcing or measuring a current. The inputs to the DUT_GND_# pins should be stable, filtered, and reflect the actual ground level at the DUT.

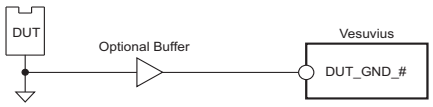


FIGURE 27. DUT GROUND SENSE CONNECTION

VOH_SDIO

VOH_SDIO is the positive power supply of the output stage of the SDIO pin and used to set the voltage level for a logical 1 at the output such that it is consistent with voltage compliance at the destination.

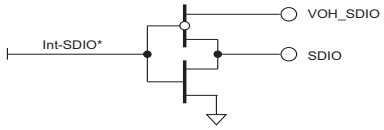
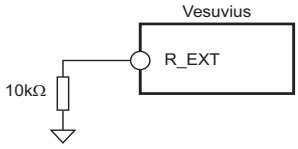


FIGURE 28. SERIAL DATA LOGIC LEVEL SETTING

R_EXT

R_EXT is a precision external resistor used to control various internal bias currents.



EXTERNAL REFERENCE RESISTOR CONNECTION

CAP_VDD

C_EXT is used to filter VDD on-chip.

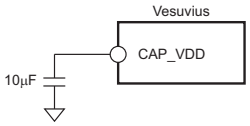


FIGURE 29. EXTERNAL CAPACITOR CONNECTION

Chip Reset

RESET is an external hardware reset signal that places all internal registers into a low state. Reset must be executed after a power-up sequence. **RESET does NOT place the DAC level memory into a known state, so this information must always be loaded after a power-up sequence.** RESET is active high.

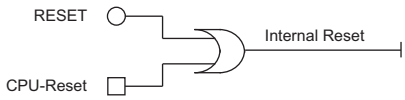


FIGURE 30. CHIP RESET

In addition, the CPU port can execute a reset (as a write only transaction). If the CPU-Reset address is written to, regardless of the value of any of the SDIO bits, CPU-Reset will fire off a one shot pulse that performs the same function as an external RESET.

Power Supply Restrictions

The following guidelines must be met to support proper operation:

1. VCC ≥ VDD, VOH_SDIO, VCCO_#
2. VEE ≤ GND
3. VDD ≥ VOH_SDIO, GND
4. VCCO_# ≥ GND

Schottky diodes are recommended on a once per board basis to protect against a power supply restriction violation.

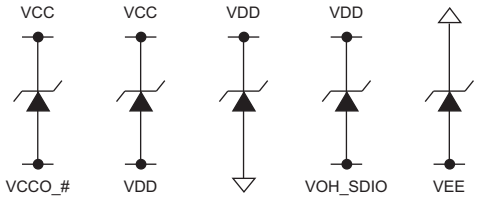


FIGURE 31. EXTERNAL SCHOTTKY DIODE SUPPLY CLAMPS

Power Supply/Analog Voltage Sequence

Ideally, all power supplies would become active simultaneously while also meeting the power supply restrictions. However, since it is difficult to guarantee simultaneous levels, the following sequence is recommended:

1. VEE
2. VCC
3. VCCO_#
4. VDD
5. VOH_SDIO
6. V_REF

DC Levels

Each channel requires several DC levels in order to function properly. The levels are all generated on-chip with a 16-bit DAC that is programmed through the CPU port.

Voltage Level Programming

The CPU port may select 1 of 2 voltage range options.

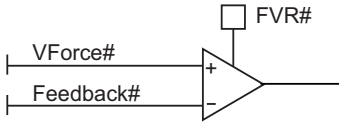


FIGURE 32. VOLTAGE LEVEL PROGRAMMING

The voltage range that is achievable is restricted by the power supply levels and headroom limitations. If a level is programmed beyond the power supply rails, saturation will occur and the actual DC level will not match the desired programmed level.

TABLE 62. VOLTAGE RANGE OPTIONS

MODE	FVR#	FULL SCALE (FS) (V)	VOLTAGE SWING (V)	RESOLUTION (LSB) (µV)	VMID (V)
FV	0	8	-2 to +6	122	+2
FV	1	16	-2 to +14	244	+6

Level Programming

When generating a voltage, use:

V_{OUT} = (Value – V_{MID}) • Gain

+ V_{MID}

+ Offset

+ DUT_GND

Value is described by:

Value = {(DAC Code)/(2^N–1)} • FS + V_{MIN}

where:

V_{MIN} = – 2V

N = 16,

2^N – 1 = 65,535

Current Clamp Programming

When programming current clamp values, use:

IOUT = (I_{DAC} – I_{MID}) • Gain + I_{MID} + Offset

I_{MID} = (I_{MAX} * 1.5)/2

I_{DAC} = ((DAC Code) / (2^N–1)) • I_{MAX} • 1.5

I-Cl+ = positive current flow out of the part

I-Cl– = negative current flow into the part

Imax = Dependent on current range selected for use in current clamp comparator

Offset and Gain

Each individual DC level has an independent offset and gain correction. These correction values allow the desired output level to be programmed at their true post calibrated value and to be loaded simultaneously across multiple pins without having to correct for per pin errors. The range of possible offset voltage correction is a % of the full-scale voltage range of each particular voltage group. In Force Current Mode for this calculation, Full-Scale (FS) Current is equal to 2 * Imax for each current. For example, in IR5, FS = 1.024A.

TABLE 63. OFFSET AND GAIN ADJUSTMENT RANGE

CODE	VALUE
OFFSET	
0000H	-5.4% of FS
7FFFH	0
FFFFH	+5.4% of FS
GAIN	
0000H	0.75 (-25%)
7FFFH	1.0
FFFFH	1.25 (+25%)

DC Calibration and Level Test Procedure

The part is designed and tested to meet its DC accuracy specifications after a calibration is performed. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks. The calibration and test points are listed in the DC Electrical Specifications Section.

The test points are broken into two categories:

1. inner test
2. outer test

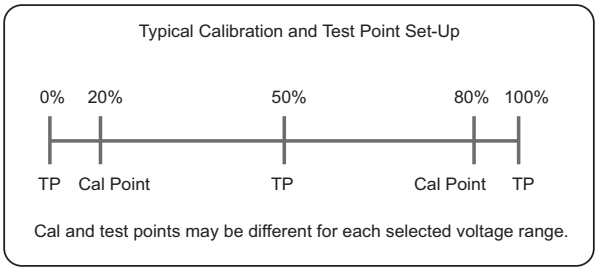


FIGURE 33.

The inner test is one specific test point (typically) at 50% of the full scale value of the particular range. The outer test is usually taken at the end points of the voltage range, or 0% and 100% of the full scale value.

Every part shipped will be calibrated and tested against the limits in the specification section, and is guaranteed to perform within those limits under the documented calibration techniques, which are located in Appendix A.

CALIBRATION PROCEDURE

1. Calibrate Monitor
2. Perform DAC LSB Calibration
3. Calibrate DAC Cal Bits
4. Calibrate Offset DAC
5. Calibrate Gain DAC
6. Calibrate Per Channel Central Offset/Gain
7. Calibrate the DC Level (FV, ICL)
8. Calibrate CME
9. Calibrate MI

LEVEL CALIBRATION

Initialize

- Select desired voltage range (VR0, VR1) (8V, 16V)
- Set Gain = 1.0; Offset = 0.0V

Measure

- Set Level 1 = Cal Point 1. Measure Output1' (low)
- Set Level 2 = Cal Point 2. Measure Output2' (high)

Calculate

- Gain' = (Output2' - Output1') / (Level 2 - Level1)
- Offset' = (Output2' - Vmid) - Gain' o (Level2 - Vmid)

Finish

- Set Offset = - Offset' / Gain'
- Set Gain = 1.0 / Gain'

DAC Calibration

A 16-bit DAC is used to generate all of the required DC levels. To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs as well as an LSB auto-calibration procedure. The default condition of these adjustment bits is the zero correction state.

DAC LSB (LEAST SIGNIFICANT BIT) AUTO-CALIBRATION

The CPU port can initiate an auto-calibration sequence to adjust the DAC LSB. Setting the register bit high initiates the sequence. When the bit is subsequently read back as a 0, the calibration is complete. Once the calibration sequence has been started, wait at least 50ms before polling,

LSB calibration values are stored in the DAC-N/DAC-P registers (central resource address 6).

TABLE 64. LSB AUTO CALIBRAITON

LSB-AUTO-CAL	LSB CAL STATUS
1	LSB calibration in progress
0	LSB calibration complete

DAC MSB CALIBRATION

To facilitate superior DC accuracy, the DAC supports the ability to independently calibrate the top 5 MSBs. The default condition of these adjustment bits is the zero correction state.

The magnitude of the bit correction is an integer count of LSB voltage added or subtracted from the individual bit weighting, and is therefore a function of the particular voltage range selected for each level. The DAC MSB adjustment is applied to the DC level after the LSB calibration but prior to the gain and offset correction.

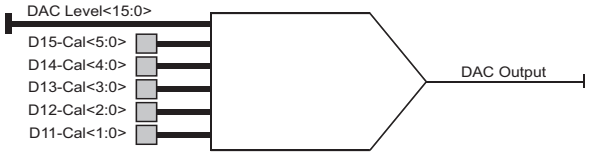


FIGURE 34.

TABLE 65. CAL RANGE VS VOLTAGE RANGE VS DAC BITS

	8V	16V
D15	±7.564mV	±15.128mV
D14	±3.66mV	±7.32mV
D13	±1.708mV	±3.416mV
D12	±732µV	±1.464mV
D11	±244µV	±488µV

TABLE 66. D15 CALIBRATION

D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	D15 Adjustment
0	1	1	1	1	1	+62 LSB
			•			•
0	0	0	0	0	1	+2 LSB
0	0	0	0	0	0	No Adjustment
1	0	0	0	0	0	No Adjustment
1	0	0	0	0	1	-2 LSB
			•			•
1	1	1	1	1	1	-62 LSB

TABLE 67. D14 CALIBRATION

D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	D14 Adjustment
0	1	1	1	1	+30 LSB
		•			•

TABLE 67. D14 CALIBRATION

D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	D14 Adjustment
0	0	0	0	1	+2 LSB
0	0	0	0	0	No Adjustment
1	0	0	0	0	No Adjustment
1	0	0	0	1	-2 LSB
		•			•
1	1	1	1	1	-30 LSB

TABLE 68. D13 CALIBRATION

D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>	D13 Adjustment
0	1	1	1	+14 LSB
	•			•
0	0	0	1	+2 LSB
0	0	0	0	No Adjustment
1	0	0	0	No Adjustment
1	0	0	1	-2 LSB
	•			•
1	1	1	1	-14 LSB

TABLE 69. D12 CALIBRATION

D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	D12 Adjustment
0	1	1	+6 LSB
0	1	0	+4 LSB
0	0	1	+2 LSB
0	0	0	No Adjustment
1	0	0	No Adjustment
1	0	1	-2 LSB
1	1	0	-4 LSB
1	1	1	-6 LSB

TABLE 70. D11 CALIBRATION

D11-Cal<1>	D11-Cal<0>	D11 Adjustment
0	1	+2 LSB
0	0	No Adjustment
1	0	No Adjustment
1	1	-2 LSB

CPU Port

All on-chip DACs and registers are controlled through the CPU serial data port, which is capable of both writing to the chip as well as reading back from the chip.

Address

Address words for every CPU transaction are all 16 bits in length and contain the destination of the data word for a write cycle, or the source to be read back for a read cycle. Address bits are shifted in LSB first, MSB last.

Data

Data words for every CPU transaction are all 16 bits in length and are loaded or read back LSB first, MSB last. The timing for data is different for a read cycle vs. a write cycle, as the drivers on the SDIO alternate between going into high impedance and driving the line.

Control Signals

There are 3 CPU interface signals - SDIO, CK, and STB. SDIO is a bidirectional data pin through which information is either loaded or written back.

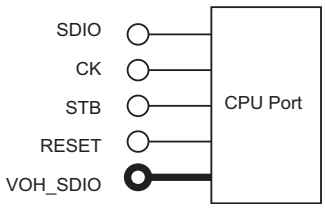


FIGURE 35. CPU PORT

CK is the CPU port clock signal. When data is going into the part, SDIO is latched on a rising edge of CK. When data is coming out of the part, SDIO is again updated on a rising edge of CK. STB is the control signal that identifies the beginning of a CPU transaction and remains high for the duration of the transaction. STB must go low before another transaction may begin.

Clock Requirements

It is recommended that the CK be running at all times as it refreshes the DC levels throughout the chip.

Write Enable

Various register bits in the memory map tables require a write enable (WE) to allow those bits to be updated during a CPU write cycle. WE control allows some bits within an address to be changed, while others are held constant. Each WE applies to all lower data bits, until another WE is reached.

If WE = 1, the registers in the WE group will be written to. If WE = 0, the registers will not be updated but all data bits associated with that field must also be programmed to 0.

WE is read back as a don't care (X) value.

Read vs Write Cycle

The first SDIO bit latched by CK in a transaction identifies the transaction type. Unused data bits are read back as a don't care (X) state.

TABLE 71. CPU TRANSACTION TYPES

1ST SDIO BIT	CPU TRANSACTION TYPE
0	Read - Data flows out of the chip
1	Write - Data flows into the chip

"Any Channel" Write

The CPU port can write to any or all selected channels with one write transaction by setting the selected channel bit in the address. Setting the channel bit hit high results in that channel being written to. Setting the channel bit low means the channel will not be written to.

TABLE 72. MULTI-CHANNEL ADDRESSING

A13	A12	A11	A10	A9	A8	A7	A6
Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0

Channel Read Back

When performing a read transaction, exactly one channel must be selected and programmed to a 1, with the remaining channel bits all programmed to 0.

Chip ID

Chip ID (see memory map tables) is a read only function that identifies the product and the die revision.

TABLE 73. CHIP ID REGISTER

D15:D4	D3:D0
Product-ID<11:0> F10 Hex (3856)	Die-Rev<3:0>

Address Space

Address Description

Information is stored on chip in two ways:

1. DC Level Memory
2. Registers

Each storage mechanism is then broken into two categories:

1. Per channel resources
2. Central resources.

The address space is partitioned into several different segments to clearly mark the resource type and function.

DAC Sample and Hold (S/H) State Machine

The internal DAC's used in the Vesuvius are S/H DACs. To update a single DAC level, it takes 387 clocks cycles. The clock used for this operation is the CPU interface clock. The first 256 clocks are used to select the desired level and let the DAC level settle. The next 128 clocks are needed to refresh the S/H. The 3 remaining clock cycles are used to control the state machine. To calculate the time to refresh one DAC level, multiply the CPU clock time by the number of clocks needed to update one level. If using a 25Mhz clock the time needed is:

$$40ns \cdot 387 \text{ cycles} = 15.48\mu s.$$

There are 32 total internal levels to the S/H DAC, therefore to update the entire DAC the time would be:

$$32 \cdot 40ns \cdot 387 \text{ cycles} = 495.36\mu s.$$

The order the state machine uses to refresh the DAC matches the RAM address mapping: ForceA0, ForceA1, ..., ForceA7, ForceB0, ForceB1, etc. This order allows several channels to update whenever a multi-channel write is performed for the same level.

Whenever writing to a specific level, the state machine will complete the current level already being processed and then jump to the level just written. After the selected level is written, the state machine then proceeds in the normal order from this level forward (i.e. it doesn't jump back). Therefore you should assume that, at worst case, it takes 774 clocks to update a single level after being written, 387 to complete the current level, plus 387 to update the desired level. One caveat to this is with a multi-channel write. There will still be, at worst case, 774 clocks to update the first (lower numbered) channel of the multi-channel write. The other channels in the multi-channel write will be updated in sequence after the first one. That means that if channel 0 and channel 7 are written as part of a multi-channel write, then channel 0 could take 774 clocks to update (worst case) and then channel 7 will update 7x387 clocks later.

Care should be taken when continuously writing to a particular level such that other levels are not starved of being refreshed by the CPU clock. If this happens, levels can droop out of specification.

TABLE 74. Vesuvius REGISTER MAP

PER CHANNEL RESOURCE REGISTER STORAGE																
REGISTER BIT	CENTRAL BIT	CHANNEL ADDRESS								PER CHANNEL RESOURCE ADDRESS						DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	0	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0	A5	A4	A3	A2	A1	A0	Register Data

CENTRAL RESOURCE REGISTER STORAGE																
REGISTER BIT	CENTRAL BIT	UNUSED BITS							CENTRAL RESOURCE ADDRESS							DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	1	0	0	0	0	0	0	0	A6	A5	A4	A3	A2	A1	A0	Register Data

CHANNEL # DC LEVEL STORAGE																
REGISTER BIT	CENTRAL BIT	CHANNEL DESTINATION SELECTION								DAC FUNCTION		DC LEVEL ADDRESS				DESCRIPTION
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0	0	0	0	0	0	0	ForceA#<15:0> Level
0	0									0	0	0	0	0	1	ForceB#<15:0> Level
0	0									0	0	0	0	1	0	CI-Vch-Isrc#<15:0> Level
0	0									0	0	0	0	1	1	CI-Vcl-Isnk#<15:0> Level
0	0									0	0	4 - 15				Not Used

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0	0	1	0	0	0	0	ForceA#<15:0> Offset
0	0									0	1	0	0	0	1	ForceB#<15:0> Offset
0	0									0	1	0	0	1	0	CI-Vch-Isrc#<15:0> Offset
0	0									0	1	0	0	1	1	CI-Vcl-Isnk#<15:0> Offset
0	0									0	1	4 - 15				Not Used

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Chan 7	Chan 6	Chan 5	Chan 4	Chan 3	Chan 2	Chan 1	Chan 0	1	0	0	0	0	0	ForceA#<15:0> Gain
0	0									1	0	0	0	0	1	ForceB#<15:0> Gain
0	0									1	0	0	0	1	0	CI-Vch-Isrc#<15:0> Gain
0	0									1	0	0	0	1	1	CI-Vcl-Isnk#<15:0> Gain
0	0									1	0	4 - 15				Not Used

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	Ch 7	Ch 6	Ch 5	Ch 4	Ch 3	Ch 2	Ch 1	Ch 0	1	1	0 - 15				Not Used

NOTE: Do not write to or read from any of the unused locations.

Protocol Timing Diagram

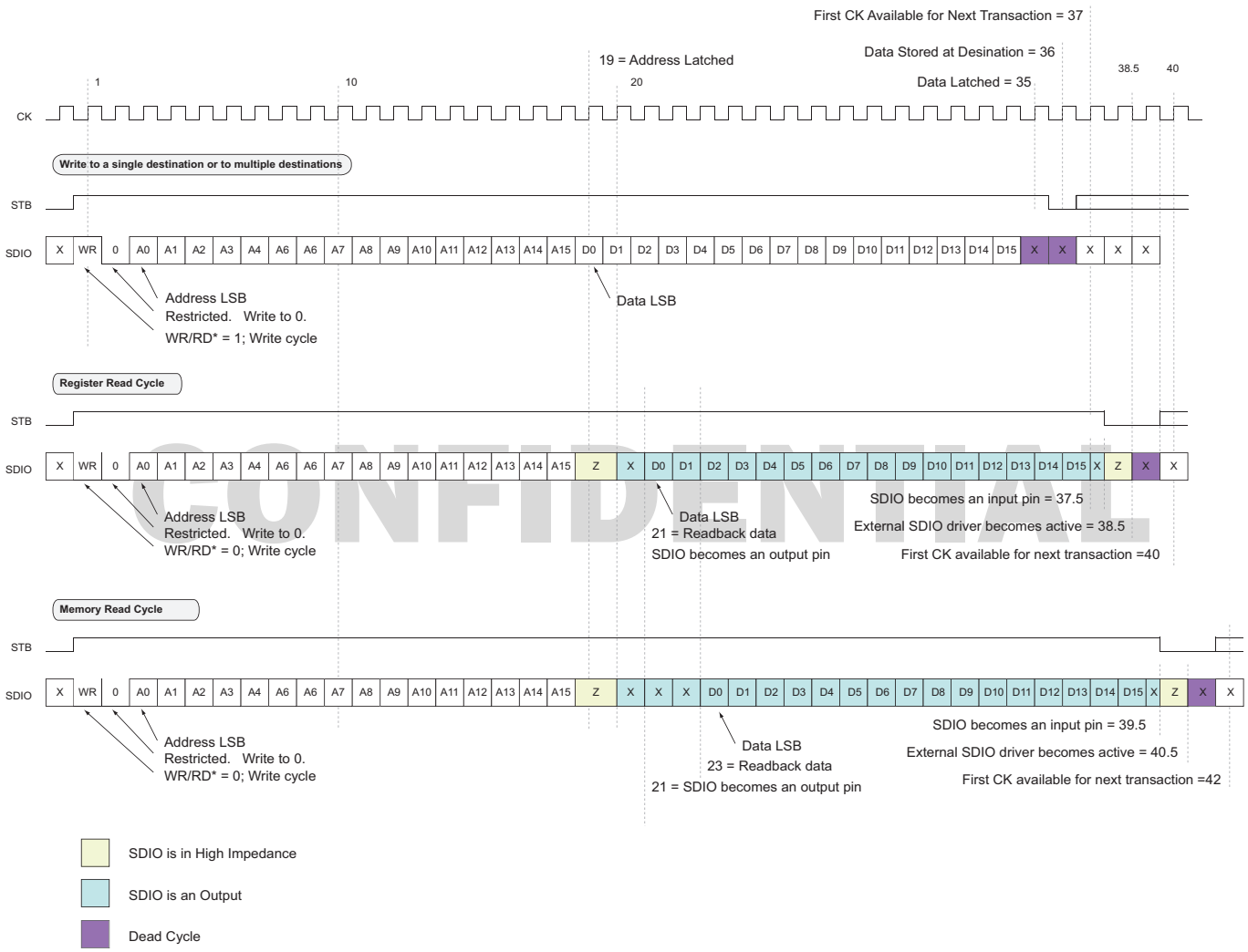


FIGURE 36. PROTOCOL TIMING DIAGRAM

Per Pin Registers

CHANNEL # CONTROL REGISTERS (0 ≤ # ≤ 7)																			
A15	A14	A<13:6>	A<5:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	#	0		WE	Sel-RT-D#	CPU-D#<1>	CPU-D#<0>	WE	FVR#	WE	FI/FV*#	WE	Sel-V-FB#<1>	Sel-V-FB#<0>	WE	Sel-VForce#	WE	Tight-Loop*#	Source and Feedback Selection
1	0	#	1	WE	Con-Res#<3>	Con-Res#<2>	Con-Res#<1>	Con-Res*#<0>	Con-Cap#<4>	Con-Cap#<3>	Con-Cap#<2>	Con-Cap#<1>	Con-Cap#<0>	WE	FV-Mode#	WE	Sel-DPS-En#	Sel-RT-En#	CPU-En#	DPS Control/Miscellaneous
1	0	#	2		WE	Kel-AI-Reset#	CI-Reset#	WE	Sel-Kel-AI#	WE	CPU-OV/OI-En#	CPU-Kel-AI-En#	CPU-OT-Dis#	WE	Sel-MI4#	Sel-MI-CI#	CI-AI-En#	CI-En#	Sel-CI-AI	Clamp and Alarm Control
1	0	#	3			L-OT-AI	RT-OT-AI	Sel-FV<1>	Sel-FV<0>	DPS-En#	Chan-Alarm#	L-OV-Vch/OI-Src#	RT-OI-Src#	OV-Vch/OI-Src#	L-OV-Vcl/OI-Snk#	RT-OI-Snk#	OI-Snk#	L-Kel-AI#	RT-Kel-AI#	Status Read Back
1	0	#	4	WE	Kelvin-Th#<3>	Kelvin-Th#<2>	Kelvin-Th#<1>	Kelvin-Th#<0>	WE	Con-EF-ES#	Con-FS#	Con-ES-F#	Con-ES-S#	Con-EF-F#	WE	Sel-Diag#<3>	Sel-Diag#<2>	Sel-Diag#<1>	Sel-Diag#<0>	Diagnostics and Calibration
1	0	#	5	WE	Bbias#	Sel-G#-Out	WE	IR#<5>	IR#<4>	IR#<3>	IR#<2>	IR#<1>	IR#<0>	WE	Sel-MU-Neg#<1>	Sel-MU-Neg#<0>	WE	Sel-MU-Pos#<1>	Sel-MU-Pos#<0>	Measurement Unit Source Selection
1	0	#	6								WE	OS#<7>	OS#<6>	OS#<5>	OS#<4>	OS#<3>	OS#<2>	OS#<1>	OS#<0>	Offset Adjust
1	0	#	7								WE	Av#<7>	Av#<6>	Av#<5>	Av#<4>	Av#<3>	Av#<2>	Av#<1>	Av#<0>	Gain Adjust

Read Only

Write Only

Per Pin Registers (continued)

CHANNEL # CONTROL REGISTERS (0 ≤ # ≤ 7)																				
A15	A14	A<13:6>	A<5:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	#	8								WE	CME-Adj0#<7>	CME-Adj0#<6>	CME-Adj0#<5>	CME-Adj0#<4>	CME-Adj0#<3>	CME-Adj0#<2>	CME-Adj0#<1>	CME-Adj0#<0>	CME Adjust IR0
1	0	#	9								WE	CME-Adj1#<7>	CME-Adj1#<6>	CME-Adj1#<5>	CME-Adj1#<4>	CME-Adj1#<3>	CME-Adj1#<2>	CME-Adj1#<1>	CME-Adj1#<0>	CME Adjust IR1
1	0	#	10								WE	CME-Adj2#<7>	CME-Adj2#<6>	CME-Adj2#<5>	CME-Adj2#<4>	CME-Adj2#<3>	CME-Adj2#<2>	CME-Adj2#<1>	CME-Adj2#<0>	CME Adjust IR2
1	0	#	11								WE	CME-LAdj3#<7>	CME-LAdj3#<6>	CME-LAdj3#<5>	CME-LAdj3#<4>	CME-LAdj3#<3>	CME-LAdj3#<2>	CME-LAdj3#<1>	CME-LAdj3#<0>	CME Adjust IR3 Low Voltage
1	0	#	12								WE	CME-HAdj3#<7>	CME-HAdj3#<6>	CME-HAdj3#<5>	CME-HAdj3#<4>	CME-HAdj3#<3>	CME-HAdj3#<2>	CME-HAdj3#<1>	CME-HAdj3#<0>	CME Adjust IR3 High Voltage
1	0	#	13								WE	CME-HAdj4#<7>	CME-HAdj4#<6>	CME-HAdj4#<5>	CME-HAdj4#<4>	CME-HAdj4#<3>	CME-HAdj4#<2>	CME-HAdj4#<1>	CME-HAdj4#<0>	CME Adjust IR4 Low Voltage
1	0	#	14								WE	CME-Adj4#<7>	CME-Adj4#<6>	CME-Adj4#<5>	CME-Adj4#<4>	CME-Adj4#<3>	CME-Adj4#<2>	CME-Adj4#<1>	CME-Adj4#<0>	CME Adjust IR4 High Voltage
1	0	#	15								WE	CME-Adj5#<7>	CME-Adj5#<6>	CME-Adj5#<5>	CME-Adj5#<4>	CME-Adj5#<3>	CME-Adj5#<2>	CME-Adj5#<1>	CME-Adj5#<0>	CME Adjust IR5

CHANNEL # CONTROL REGISTERS (0 ≤ # ≤ 7)																				
A15	A14	A<13:6>	A<5:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	0	#	16																	Not Used
1	0	#	17								WE	MUR#<1>	MUR#<0>	WE	Sel-Mon#-OE	CPU-MON#-OE				Per-Channel Measurement Unit Control/Ganging
1	0	#	18-63																	Not Used

Central Resource Registers

CENTRAL RESOURCE CONTROL REGISTERS																				
A15	A14	A<13:7>	A<6:0>	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DESCRIPTION
1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	CPU-Reset (Blue = Write Only)
1	1	0	1			WE	Reserved	Reserved	Reserved	WE	MUR<1>	MUR<0>	WE	Sel-Mon-OE	CPU-Mon-OE	WE	Sel-MU<2>	Sel-MU<1>	Sel-MU<0>	Measurement Unit Control/Ganging
1	1	0	2					WE	CPU-Cent-D<3>	CPU-Cent-D<2>	CPU-Cent-D<1>	CPU-Cent-D<0>	WE	Sel-MI-Mon-OE	CPU-MI-Mon-OE	WE	Sel-Cent-MI<2>	Sel-Cent-MI<1>	Sel-Cent-MI<0>	Measure Current Monitor/Central Level Select
1	1	0	3	L-OT	RT-OT	OT-Alarm	WE	OT-Flag-Reset	WE	GBL-CPU-OT-DIS	CPU-Alarm	WE	CPU-Alarm-En	WE	CPU-OT	WE	CPU- Tj-En	WE	Sel-OT-Alarm	Alarm Control
1	1	0	4				WE	D14-Cal<4>	D14-Cal<3>	D14-Cal<2>	D14-Cal<1>	D14-Cal<0>	WE	D15-Cal<5>	D15-Cal<4>	D15-Cal<3>	D15-Cal<2>	D15-Cal<1>	D15-Cal<0>	Upper DAC Bit Calibration
1	1	0	5			WE	LSB-Auto-Cal	WE	D11-Cal<1>	D11-Cal<0>	WE	D12-Cal<2>	D12-Cal<1>	D12-Cal<0>	WE	D13-Cal<3>	D13-Cal<2>	D13-Cal<1>	D13-Cal<0>	Mid DAC Bit Calibration
1	1	0	6		DAC-N<6>	DAC-N<5>	DAC-N<4>	DAC-N<3>	DAC-N<2>	DAC-N<1>	DAC-N<0>		DAC-P<6>	DAC-P<5>	DAC-P<4>	DAC-P<3>	DAC-P<2>	DAC-P<1>	DAC-P<0>	DAC-N/DAC-P
1	1	0	7 – 126																	Not Used
1	1	0	127	Product-ID<11>	Product-ID<10>	Product-ID<9>	Product-ID<8>	Product-ID<7>	Product-ID<6>	Product-ID<5>	Product-ID<4>	Product-ID<3>	Product-ID<2>	Product-ID<1>	Product-ID<0>	Die-Rev<3>	Die-Rev<2>	Die-Rev<1>	Die-Rev<0>	Die ID (Yellow = Read only)

Read Only

Write Only

After being set high, will remain high until autocal sequence is complete.

Thermal Analysis

Junction Temperature

Maintaining a low and controlled junction temperature is a critical aspect of any system design. Lower junction temperatures translate directly into superior system reliability. A more stable junction temperature translates directly into superior AC and DC accuracy.

The junction temperature follows Equation 1:

$$T_J = P_D \bullet \theta_{JA} + T_A \quad \text{(EQ. 1)}$$

where:

T_J = Junction Temperature

P_D = Power Dissipation

θ_{JA} = Thermal Resistance (Junction to Ambient)

T_A = Ambient Temerature

Heat can flow out of the package through two mechanisms:

- conduction
- convection

Conduction

Conduction occurs when power dissipated inside the chip flows out through the leads of the package and into the printed circuit board. While this heat flow path exists in every application, most of the heat flow will NOT occur with thermal conduction into the PCB.

Conduction also occurs in applications using liquid cooling, in which case most of the heat will flow directly out of the top of the package through the exposed heat slug and into the liquid cooled heat sink. The heat sink represents a low thermal resistance path to a large thermal mass with a controlled temperature.

The total thermal resistance is the series combination of the resistance from the junction to case (exposed paddle) (θ_{JC}) plus the resistance from the case to ambient (θ_{CA})

Convection

The most common cooling scheme is to use airflow and (potentially) a heat sink on each part. In this configuration, most of the heat will exit the package via convection, as it flows through the die, into the paddle, and off the chip into the surrounding air flow.

Thermal Resistance

Each system will have its own unique cooling strategy and overall θ_{JA}. However, the resistance between the junction and the case is a critical and common component to the thermal analysis in all designs.

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \text{(EQ. 2)}$$

θ_{CA} is determined by the system environment of the part and is therefore application specific. θ_{JC} is determined by the construction of the part.

θ_{JC} Calculation

$$\theta_{JC} = \theta(\text{silicon}) + \theta(\text{dieattach}) + \theta(\text{paddle}) \quad \text{(EQ. 3)}$$

$$\theta_{JC} = 0.072°C/W + 0.61°C/W + 0.006°C/W$$

$$\theta_{JC} = 0.688°C/W$$

The calculation is based upon ideal assumptions and it should be treated as a best-case value.

The thermal resistance of any material is defined by Equation 4:

$$\theta = (\text{Intrinsic material resistivity}) \bullet \text{Thickness}/\text{Area}$$

or

$$\theta = \text{Thickness}/(\text{Intrinsic material conductivity} \bullet \text{Area}) \quad \text{(EQ. 4)}$$

Intrinsic Thermal Conductivity

Die Attach Thermal Conductivity = 1.4W/M °K

Silicon Thermal Conductivity = 141.2W/M °K

Paddle Thermal Conductivity = 263W/M °K

Plastic Thermal Conductivity = 0.88W/M °K

(Although some heat will flow throw the plastic package, the molding compound conductivity is not specifically used in the calculation of θ_{JC} through the paddle. The assumption is that all heat flow will go through the paddle and none through the surrounding plastic).

Manufacturing Information

Moisture Sensitivity

The Vesuvius is a Level 3 (JEDEC Standard 033A) moisture sensitive part. All Pre Production and Production shipments will undergo the following process post final test:

- Baked @ +125°C ± 5°C for a duration ≥ 16 hours
- Vacuum sealed in a moisture barrier bag (MBB) within 30 minutes after being removed from the oven.

PCB Assembly

The floor life is the time from the opening of the MBB to when the unit is soldered onto a PCB.

- Product Floor Life ≤ 168 Hours

Units that exceed this floor life must be baked before being soldered to a PCB.

Solder Profile

The recommended solder profile is dependent upon whether the PCB assembly process is lead-free or not.

TABLE 73. Solder Profile

Profile Feature	Pb-Free Assembly
Average ramp up rate (T_L to T_P)	3°C/sec (max)
Preheat • Min Temp (Ts min) • Max Temp (Ts max) • Time (min to max) (ts)	 150°C 200°C 60 – 180 sec
Ts max to T_L • Ramp Up Rate	 3°C/sec (max)
Time above • Temperature (T_L) • Time (t_L)	 217°C 60 – 150 sec
Peak Temperature (T_P)	260°C
Time within 5°C of actual peak temp (tp)	20 sec – 40 sec
Ramp down rate	6°C/sec (max)
Time 25°C to peak temperature	8 minutes (max)

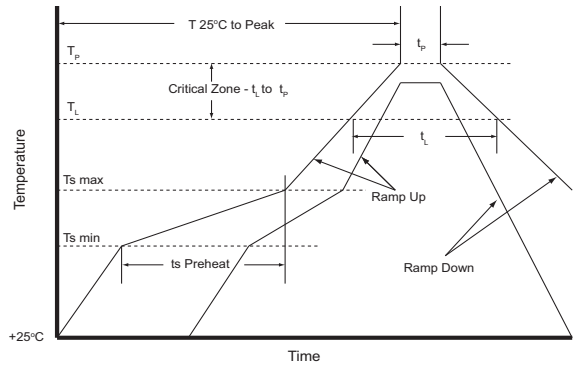
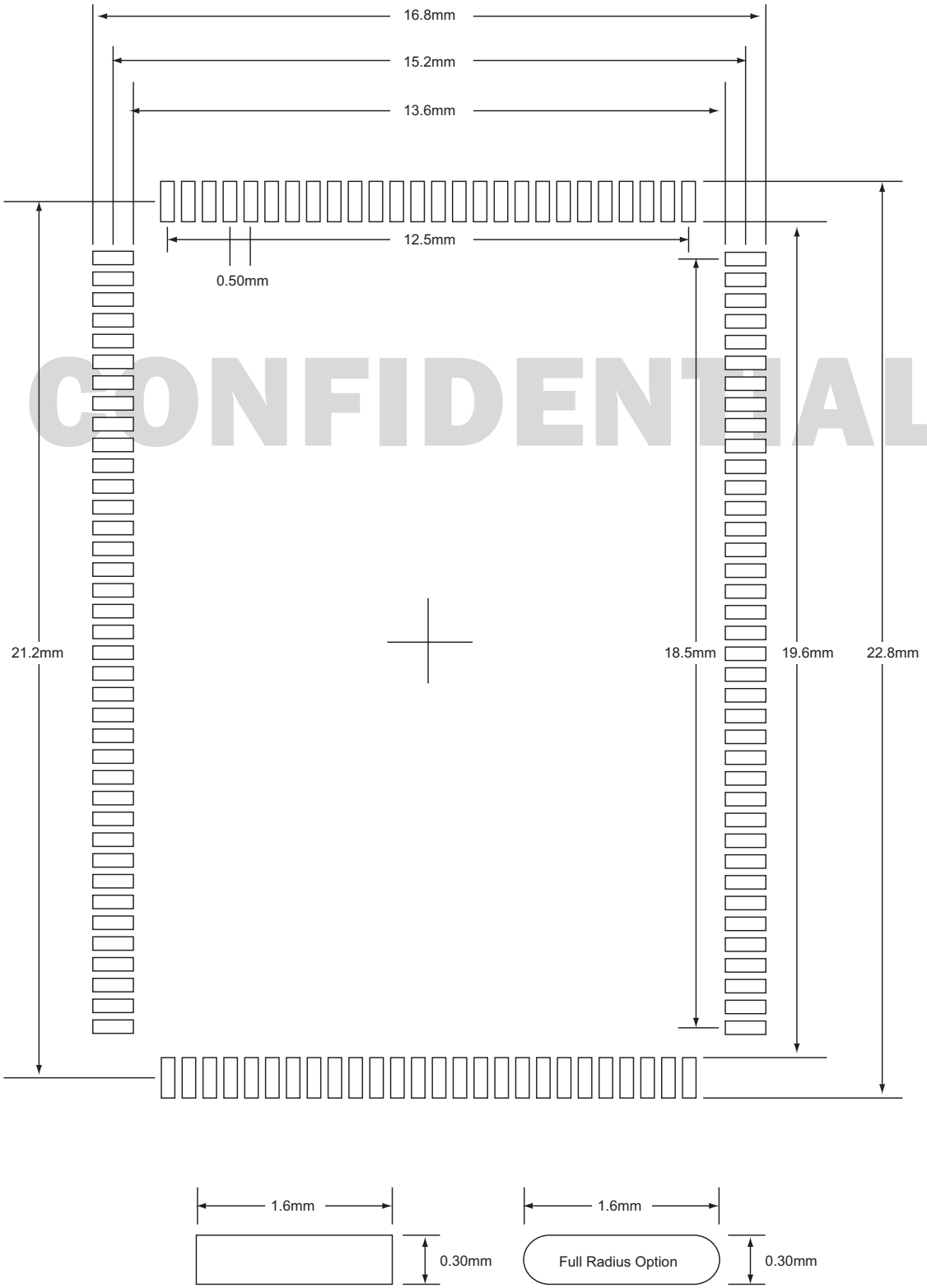
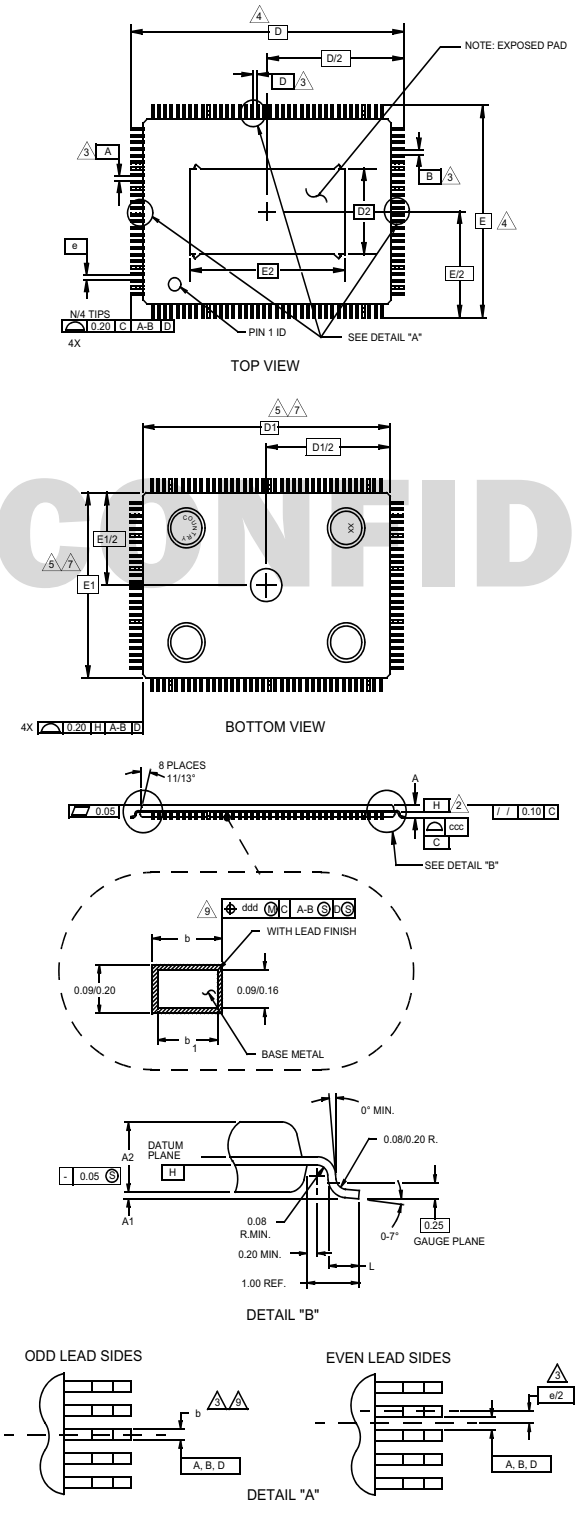


FIGURE 37.

Recommended PCB Footprint



Package Outline Drawing



Q128.14x20A

128 Lead Thin Quad Flatpack with Top Exposed Pad

SYMBOL	MILLIMETERS BHB MIN	NOM	MAX	NOTES
A	-	-	1.60	
A1	0.05	-	0.15	13
A2	1.35	1.40	1.45	
D		22 BSC		4
D1		20 BSC		7, 8
D2		(12.81-0.76) BSC		14
E		16 BSC		4
E1		14 BSC		7, 8
E2		(8.38-0.76) BSC		14
L	0.45	0.60	0.75	
N		128		
e		0.50 BSC		
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

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NOTES:

1. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
2. Datum plane H located at mold parting line and coincident with lead, where lead exits plastic body at bottom of parting line.
3. Datums A-B and D to be determined at center lines between leads where leads exit plastic body at datum plane H.
4. To be determined at seating plane C.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable mold protrusion is 0.254mm per side on D1 and E1 dimensions.
6. “N” is the total number of terminals.
7. These dimensions to be determined at datum plane H.
8. Package top dimensions are smaller than package bottom dimensions and top of package will not overhang bottom of package.
9. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located at the lower radius or the foot.
10. Controlling dimension: millimeter.
11. Maximum allowable die thickness to be assembled in this package family is 0.38 millimeters.
12. This outline conforms to JEDEC publication 95 Registration MS-026, variations BHA & BHB.
13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
14. Dimensions D2 and E2 represent the size of the exposed pad. The actual dimensions may be reduced up to 0.76mm due to mold flash.

Revision History

DATE	CHANGE
January 14, 2010	• Page 15: Add current ranges to the Test Conditions column for all FV (POST CALIBRATION) tests. • Page 18: Update all '0' current test points to be (+Imax/10) or (-Imax/10). • Page 69: Update D2 and E2 in Package Drawing
February 26, 2020	• Page 15: Spec #14090 Test Conditions - Changed upper test point to VCC-1.5V. • Page 15: Spec #14200 Test Conditions - No-Load test points only tested in IR5 and IR0.
January 22, 2020	• Page 10: Updated Recommended Operating Conditions for GANG#_IN and GANG#_OUT pins to (VCC-1.5V) and (VEE+1.5V) • Page 13: Spec #10800. Removed 0V Test Point. Updated Test Points to: VCC - 1.5V and VEE + 1.5V • Page 13: Spec #10801. Removed 0V Test Point. Updated Test Points to: VCC - 1.5V and VEE + 1.5V • Page 28: Change EXT_MON_OE Symbol to be a pin, not a register • Page 31: Corrected the GBL-CPU-OT-DIS name • Page 52: Corrected Kelvin-Th# register name • Page 62: Corrected the Kelvin-Th# register names • Page 65: Corrected the GBL-CPU-OT-DIS register name
June 16, 2019	• Page 31: Correct the GBL_CPU_OT_DIS name. Correct the CI-Reset# name. • Page 34: Figure 2. Correct the CPU-OV/OI-En# and OV/OI# names. • Page 39: Updated Table 23. Add table 24 and 25. • Page 39: Table 22. Update IR5 Resolution • Page 48: Update resistor values in Table 44.
February 11, 2019	• Page 16: Spec #14200 Test Conditions - No-Load Test Point changed from -2V to -1.5V • Page 64: Updated per-channel MUR registers to add #
June 27, 2018	• Page 16: Table 1 - Add separate IR0 specs, add TPI2 column • Page 17: change spec 14100 to 14100A; change min and max values; add spec 14100B

DATE	CHANGE
April 10, 2018	• Page 11: Update Test Conditions, min and max values and spec #s. • Page 13: Analog Pins Table - Spec #20210, add CAP_A_# to parameter • Page 14: Spec #s 16220, 16230, 16310, change min from -2 to -3; Spec #16320, change from min/max -2/+2 to -3/+4; Spec #16330, change from min/max -5/+5 to -6/+6 • Page 15: Spec #14200 Test Conditions - change calibration points from 0V, 3V to 0V, 2.5V; Full-Load Test Points, change from 0V, 3.5V to 0V, 3V. • Page 17: Spec #s 14100 through 14105B - Add FV_MODE = 1 or FV_MODE = 0 to Test Conditions • Page 18: Table 4, TPI for IR0-IR4- change +Imax/2 and +Imax/5 to -Imax/2 and -Imax/5 • Page 19: Update all min/max values for FI and MI (Post Calibration) • Page 20: Table 5 - Update Cal Points and TPO columns, remove TPI1 and TPI2 columns • Page 20: DC Electrical Specs Current Clamps - Remove TP1 and TP2 Test Points, update min and max values • Page 20: DC Electrical Specs Voltage Clamps, Spec #14430, update min/max values • Page 24: Add spec #s for Span and Resolution • Page 25: Add spec #s for Setup Time; remove spec #s from rest of table • Page 30: Change Sel-Mon0_OE to Sel-Mon0-OE and CPU_Mon0-OE to CPU-Mon0-OE • Page 31: Update diagram • Page 32: Update diagram • Page 33: Current Ranges - Add sentence to end of second paragraph • Page 37: Table 19 updated • Page 38: Move Programmable Voltage Clamps section after Table 23. Change “Clamp Source” to “Current Clamp Source. • Page 39: Method 2, change Connect F_S to Connect FORCE_# to SENSE_# (Con-FS# = 1) • Page 52: Move and revise last 2 paragraphs under Temperature Sensing after Table 59 • Page 60: Register Read Cycle and Memory Read Cycle - change “write cycle” to “read cycle”. • Page 66: Add Solder Profile to Manufacturing Information section • Page 83: Section 10.3.2, #9, change (Level2 - Vmid) to (Level2 - Vmid) - DUT_GND • Page 90: 10.4.3.1, #7 & 8 - Change I-Cl-Src# to Cl-Vch-Isrc# • Page 91: Table 6 - update values • Page 91: Change all I-Cl-Src# to Cl-Vch-Isrc# • Page 92: Add 10.4.4 Force Current Calibration Section
May 30, 2017	• Page 1: Remove “Target” • Page 10: IR0-IR5: Change to VEE + 3.0 to min of (VCC0–1.5) or (VCC–2.5) to VEE + 4.0 to min of (VCC0–1.5) or (VCC–3.0) • Page 17: Add Bbias = 0 to Test Conditions for Spec #s 14100 - 14102; Add Bbias = 1 to Test Conditions for Spec #s 14102A - 14105B; add typical values for MI Temperature Coefficient lines • Page 18: Tables 3 & 4 - Cal Points and TPI values updated • Page 19: Delete Spec #s 15103B, 15104B & 15105B; Spec #s 15100 - 15105: Add Bbias = 0 to Test Conditions, replace TBDs with values • Page 21: Voltage Clamps Table: Spec #14430, change Min/Max from -100/+100 to -500/+500 • Page 22: Spec #14713, change Max from 175 to 200 • Page 23: Spec #14410, change Max from 300 to 350 • Page 28: Updated diagram • Page 33: Table 1 - Line 3, change FI/FV*# from 0 to 1, change Cl-En# from 1 to N/A; delete line 4 • Page 36: Figure 4 updated • Page 37: Delete last paragraph in Voltage Range Selection section • Page 39: Method 2, 2nd paragraph - change IR#<X> to IR#<5:0>; add new paragraphs after Table 24 • Page 50: Figure 20 updated • Page 55: Offset & Gain section - Add sentence to end of first paragraph • Page 70: Update part # from ELE58VE1A-NEJ01 to ELEVE2A-NEJ01 • Page 87: Add Section 10.4.3

DATE	CHANGE
February 7, 2017	• OT-Alarm changes to OT-Alarm# in all cases. MI-S# changes to MI-Raw# in all cases. • Page 10: IR0-IR5: Change to VEE + 1.5 to min of (VCC0–0.15) or (VCC–1.0) and VEE + 3,0 to min of (VCC0–1.5) or (VCC–2.5) • Page 15: Spec #14090 Test Conditions - add Tightloop*# = 1 • Page 16: Change Force and Measure Current to Measure Current • Page 17: Remove Force from title and Parameters - Spec #s 14103B, 14104, 14104B, 14105 and 14105B Test Conditions updated • Pages 18 & 19: Add Force Current Tables and Force Current DC Spec Table • Page 21: Table 6 - remove 4V and 8V lines • Page 22: Spec # 19112 - change max from 150 to 1000 • Page 23: Delete ESP Table • Page 24: Add Central Level Gain and Offset Table • Page 25: Add CPU Port Table • Page 28: Per Channel Diagram updated • Page 31: OI, OT and Kelvin Alarm diagram updated • Page 35: DPS Channel diagram updated • Page 37: Delete High Density DPS Connectivity section - Page 37: Table 19 updated • Page 38: Programmable Voltage Clamps - add note to end of section • Page 49: Over-Temperature Alarm Section, last paragraph - change GBL-CPU-DIS to CPU-OT-DIS • Page 50: Over-Current/Voltage diagram updated • Page 52: Diagnostic Circuitry diagram updated - Table 58: Columns 1 and 2 updated - Table 59: Channel 6 - change TJ to V-Temp - Temperature Sensing Section rewritten • Page 63: Change ESP Resistance to Not Used - Page 71: Scope, second sentence - remove ESP function. - Page 72: Remove ESP from diagram
August 11, 2015	• Page 1: Features: Update last bullets of “Per Channel DPS” and “Package/Power Dissipation” sections • Page 10: Recommended Operating Conditions- IR0-IR5 (FV Mode # = 0): change ((VCC0-0.15), (VCC-1.0))V to (VCC0-1.0), (VCC-2.5))V • Page 11: Power Supply Current Table - replace TBDs with values. Change note. • Page 18: Current Clamps - Add new section above spec table. • Page 20: Monitor Table: Add spec numbers and replace TBDs with values. • Page 26: add AN D gate to diagram • Page 34: Short Circuit Limit Section: change … 200% max of either IR4 or IR5 to … 200% of IR4 or 50% of IR5. • Page 36: Measure Voltage Section - update equation section • Page 44: Over-Temperature Protection - Add paragraph after Table 49; add 2 paragraphs after Table 50. • Page 46: Figure 23 - add AND gate to diagram • Page 47: Update Figure 25 - Temperature Sensing Section - update entire section. • Page 48: Figure 26 updated. • Page 56: Status Read Back line updated • Page 57: Upper DAC Bit Calibration line updated.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ELE58VE2A-NEJ01	ELE58VE2A-NEJ01	Tj = 25°C to 100°C	128 Ld, 14 x 20mm LQFP	Q128.14x20F

Appendix A

Vesuvius Calibration Procedure

1. Calibration Overview

Calibration is the process of transferring accuracy standards from one measurement or source instrument to another. In an ideal case, a voltage applied to the input of a unity gain amplifier would equal the output voltage of the amplifier. In reality, there are several factors that will have an impact of the accuracy of the amplifier and introduce errors. Some of the errors introduced are: input offset voltages, gain errors, and linearity errors. To reduce these types of errors in the amplifiers and their surrounding circuitry, calibration is performed. This accuracy transfer aids in the process of verifying the performance of an instrument is within a set of pre-defined specifications.

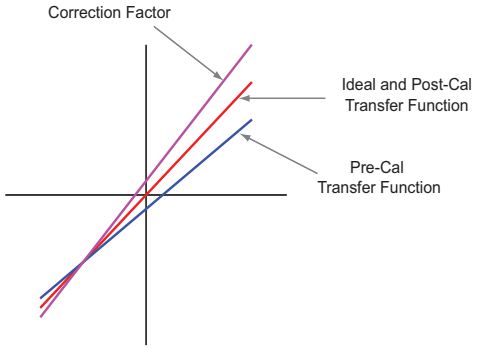

FIGURE 1. CALIBRATION

2. Calibration Basics

1. The basic calibration formula that is used for the Vesuvius calibration routines is the "slope intercept" or straight line equation: Y = (M * X) + B; where M=Gain or slope; B=Offset or y-intercept, X=Input or Independent Variable; Y=Output or Dependent Variable.
   - In the context of this document the variables from the slope intercept equation are referred to as follows: M=Gain; B=Offset; X=Input; Y=Output
   - To calculate the Gain and Offset using 2 Input points and 2 Output points
     - -Gain = (Y2 - Y1) / (X2 - X1)
     - -Offset = Y2 - (Gain * X2)
   - To solve for Y if X is known Y = Gain * X + Offset
   - To solve for X if Y is known
     - -X = (Y - Offset) / Gain
2. Each Path requires its own calibration factors
3. Each op-amp has some gain/offset error contribution
4. Only need 1 calibration factor even if multiple op-amps are in the same path

5. Resistive paths (i.e. muxes, switches) typically don't require additional calibration factors; however could cause gain error (voltage divider)

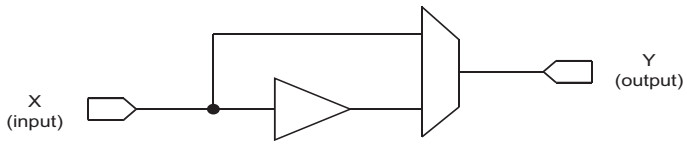

FIGURE 2. CALIBRATION BASICS

3. DC Calibration

Proper calibration is essential to ensure that the Vesuvius is operating with the accuracy expected by the user. The Vesuvius is designed and tested to meet DC accuracy specifications in this datasheet with either a two or four point calibration. The actual calibration points are different for each voltage range, and may even be different for the same voltage range but for different functional blocks (ForceA#, ForceB#, Cl-Vch-Isrc#, Cl-Vcl-Isnk#). In general, most calibration points are at 20% and 80% of the full-scale value for that range for a 2-point calibration. For measure current calibration, a common 4-point/2-segment technique is used with calibration points at +/-80% and +/-20% of the Imax (maximum current) range. The calibration points used for ATE testing are listed separately for each functional block by range in the DC Electrical Specifications section.

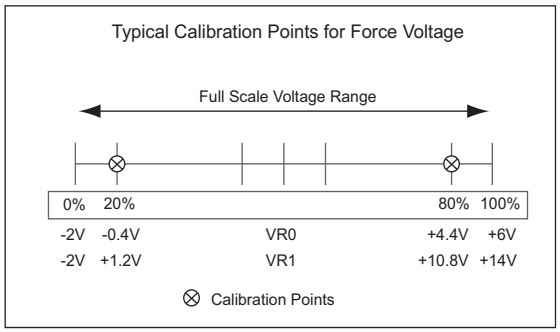

FIGURE 3. TYPICAL FORCE VOLTAGE CALIBRATION POINTS

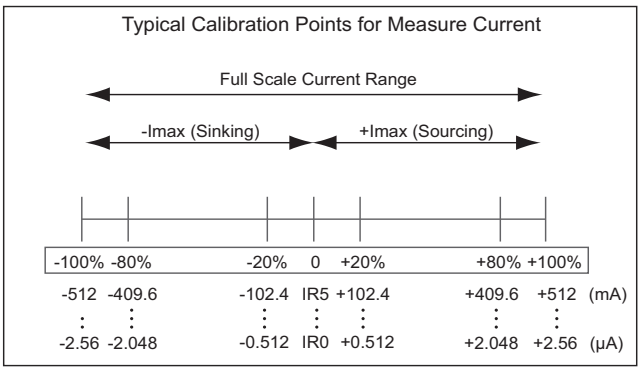

FIGURE 4. MEASURE CURRENT CALIBRATION POINTS

Scope

This document is meant as a basic calibration document for one channel and does not encompass all aspects of the chip. Certain aspects of the calibration have been purposely omitted such as the ganging, Force Current (Using current clamps), Current Clamps, and the per-channel Central Gain and Offset to limit the complexity and length of the calibration documentation. The calibration for these and more complex features will be covered at a later date with Elevate Application Notes.

The calibration methods in the document describe how the Vesuvius has been calibrated in the EVM(Evaluation Module)/ATE (Automated Test Equipment) environment. In an actual customer environment, the Vesuvius would typically be calibrated via the EXT_FORCE/EXT_SENSE pins that would be connected to one main central calibration resource. Due to the limitations of resources in the EVM/ATE environments, the FORCE_# pin or SENSE_# pin were used for some calibration.

Equipment Needed

Analog to Digital Converter, Source Voltage/Current Measurement Unit, Power Supplies

System Level DC Accuracy Limits

Alternate calibration procedures and techniques using more or fewer calibration points may also be employed in order to achieve the desired system level accuracy and make trade-offs between accuracy and calibration time. The resulting system level accuracy may be superior or inferior to the techniques listed below and will be dependent on the specific details of a particular application. To meet the DC specifications in this datasheet, the calibration procedures listed were used.

4. Vesuvius DPS Channel Overview

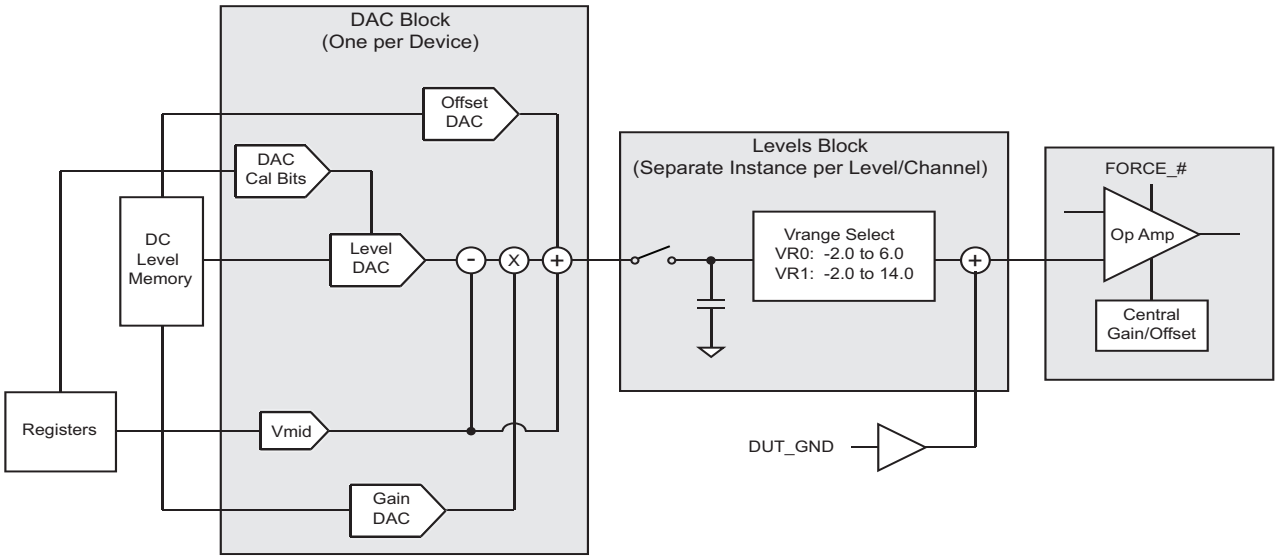

FIGURE 5. Vesuvius DPS CHANNEL

The Vesuvius DPS channel is comprised of several blocks as shown in Figure 5 above. There is one on-chip sample and hold 16-bit DAC that creates the required output voltage levels for all on-chip level functionality. The DAC circuit is comprised of a main Level DAC and has registers and logic which allow for on-chip calibration of this main Level DAC via the Offset and Gain correction DACs. Each Level DAC, Offset DAC, and Gain DAC has addressable registers which are accessible to the user through the CPU port. The values programmed into the Offset and Gain registers are calculated during a calibration procedure. The Gain/Offset DACs are calibrated independently and the calibration values are globally applied to all Functional Blocks. The Level DAC, voltage range select, and output forcing amplifiers are calibrated together to obtain specific per level calibration values. Vmid corresponds to a Value DAC code of 0x7fff and is the value at which the level Pivots. The Offset DAC and Gain DAC provide a hardware correction and allow an application to broadcast the same Level DAC code to many separate parts or channels at one time. The Sample and hold portion of the DAC will not be covered in this section, but to get more information see the DAC Sample and Hold (S/H) State Machine section of this data sheet. Following the S/H cap is the Voltage Range select section of the channel. There are 2 voltage range options for the Vesuvius: 8V and a 16V Range. DUT_GND (DUT Ground) is then added to the level to make sure the output voltage level of the Vesuvius is relative to the DUT. A central Gain/Offset can then added to the voltage level at the output Op-Amp to compensate for any errors when sharing one level among multiple channels.

5. Hardware/Software Calibration Distinction

A Hardware Calibration nomenclature implies a software algorithm is used to calibrate and determine the calibration values. The calibration values are then loaded into the Vesuvius (hardware registers/RAM) which then applies the calibration correction factor. The Vesuvius contains Gain and Offset calibration registers for all of the DC Levels. In addition, the Vesuvius contains calibration registers for the DAC MSB (Most Significant Bit) Calibration Bits, DAC LSB (Least Significant Bit) Auto-Calibration, and CME (Common Mode Error) Adjust.

The Software Calibration nomenclature implies a software algorithm is used to calibrate and determine the calibration values. Software is then required to apply the calibration correction factor to determine the actual result and store the calibration values until use. These include the calibration for the Gain DAC, Offset DAC, MV (Measure Voltage), and MI (Measure Current).

6. Total Chip Calibration Procedure Outline

The DC calibration for the Vesuvius consists of the following steps which are also in the recommended calibration order. An (HW) or (SW) is included next to each section of calibration to distinguish between a Hardware and Software calibration.

6.1 Monitor/Measure Voltage (MV) (SW) - One Per Chip

Need to calibrate each Measurement Unit Range (MUR).

6.2 DAC Calibration - One Per Chip

6.2.1 DAC LSB Auto Calibration (HW)

6.2.2 DAC Cal Bits (HW)

6.2.3 Offset DAC (SW)

6.2.4 Gain DAC (SW)

6.3 DC Levels Calibration – Per Channel

6.3.1 Central Level Gain/Offset – per Voltage Range (HW)

6.3.2 FV Force Voltage (FV) – per Voltage Range (HW)

6.3.3 Current clamps (Iclamps) – per Current Range (HW)

6.3.4 Force Current (FI) – per Current Range (HW)

6.3.5 Voltage Clamps - per Voltage Range (HW)

6.4 Measure Current (MI) – Per Channel

6.4.1 Common Mode Error (CME) (HW) – per Current Range (IR). IR3/IR4 are also per FV-Mode.

6.4.2 Measure Current (SW) – per Current Range (IR)

7. DC Level Output Equation for Force Voltage DAC Level

Vout = (Value-Vmid) * Gain + Vmid + Offset + DUT_GND. This equation will also be discussed in the Level programming section of this document.

1. Vmid = 2V (8V range, FVR# = 0). Vmid = 6V (16V Range, FVR# = 1). Vmid corresponds to a Level DAC code of 0x7FFF and is the pivot point of the gain for the Level DAC.
2. Value = Voltage Level corresponding to value written to Level DAC location.
3. Gain = Gain corresponding to value written to Gain DAC location.
4. Offset = Offset corresponding to the value written to the Offset DAC location.
5. DUT_GND = Voltage at DUT_GND# pin corresponding to ground at DUT (device under test).

This equation is included early in the calibration section because it is used prior to the actual DC Level Calibration section.

Note: This DC level equation is a little different than the "slope-intercept" equation discussed at the beginning of this document. This equation represents how the DAC is implemented in hardware.

8. DC Level Memory RAM Code Calculation

8.1 Level DAC

- Level.Value = (DAC Code / 0xFFFF) * Level.FS + Level.Vmin
- Level.Value = Output Voltage of Level DAC
- Level.Vmin (Minimum Output Voltage Level) = Vmid - (Level.FS /2)
- Level.FS (Full Scale Output Voltage) = 8V (FVR#=0) or 16V (FVR#=1)
- Vmid (DAC Mid Voltage) = 2V (8V range, FVR#=0), 6V (16V Range, FVR#=1)

8.2 Offset DAC

- Offset.Value = (DAC Code / 0xFFFF) * Offset.FS + Offset.Vmin
- Offset.Value = Output Voltage of Offset DAC
- Offset.Vmin (Minimum Offset Voltage Level) = -5.4% * Level.FS
- Offset.FS (Full Scale Offset Output Voltage) = abs(2*Offset.Vmin)

8.3 Gain DAC

- Gain.Value = (DAC Code / 0xFFFF) * Gain.FS + Gain.Vmin
- Gain.Value = Amount of Gain
- Gain.Vmin (Minimum Gain) = 0.75
- Gain.FS (Full Scale Gain Span) = 0.50 (0.75 to 1.25)

9. Basic Force Voltage Setup

The following setup will be used as the basic setup for many of the calibration procedures listed in this document. Any changes required to this basic setup will be noted in each calibration section. This setup also assumes channel 0 is used for calibration.

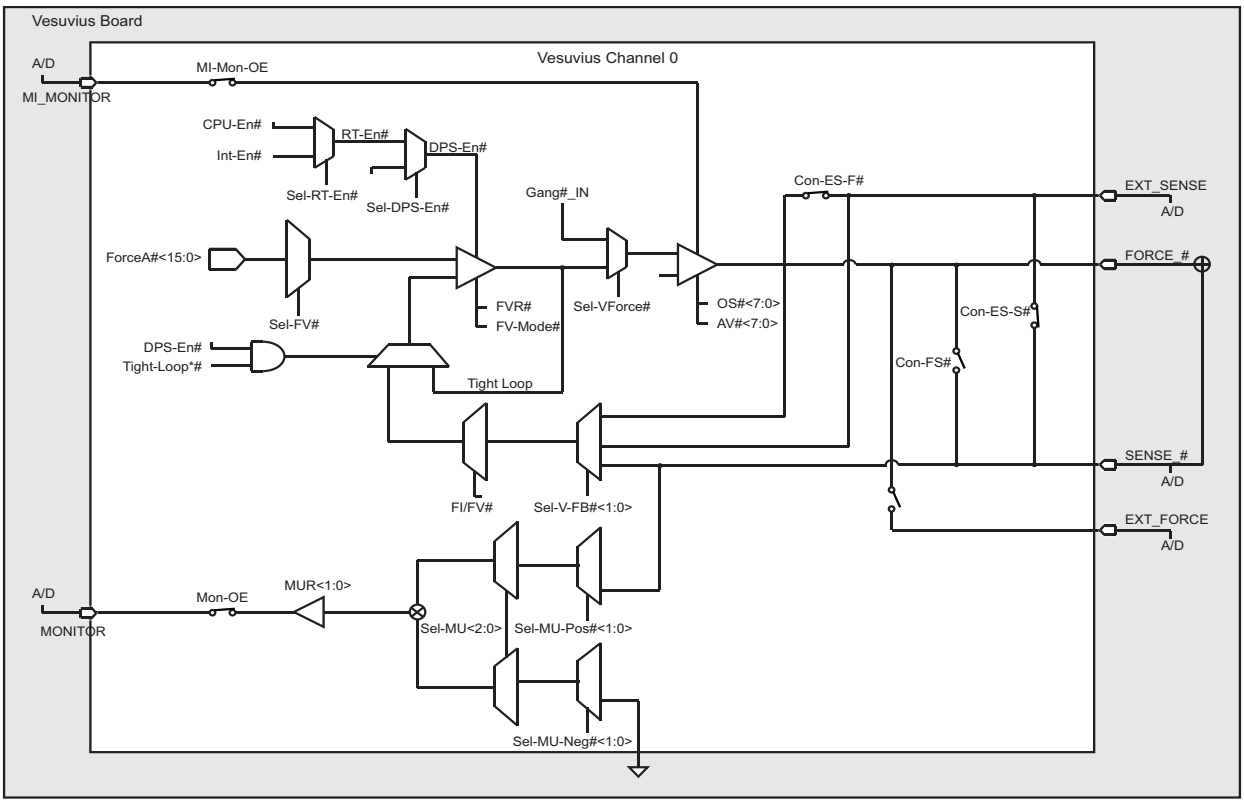

FIGURE 6. BASIC FORCE VOLTAGE SETUP

Force Voltage Setup:

1. CPU-Reset = 1 (This will reset the Vesuvius and places all internal registers into a low state, but does not affect the DC Level Memory locations). Only registers that need to be changed from a '0' to '1' will be shown below.
2. FV Mode# = 1 (Low Current Mode)
3. FVR # = 0x01 (FVR#=16V Range)
4. MU-Pos# = 0x02 (Sense)
5. MUR<1:0> = 0x03 (16V Measurement Range)
6. IR<5:0> = 0x08 (IR3, 2.56mA)
7. ForceA# Level = 0x7FFF (Voltage = 6V, DC Level Memory Address 0x0000)
8. ForceA# Offset = 0x7FFF (Offset = 0V, DC Offset Memory Address 0x0010)
9. ForceA# Gain = 0x7FFF (Gain = 1, DC Gain Memory Address 0x0020)
10. CPU-Mon-OE = 1 (MONITOR Output Enabled)
11. CPU-MI-Mon-OE = 1 (MI_MONITOR Output Enable)
12. Con-ES-F# = 1 (Connect External Sense to Force)
13. Con-ES-S# = 1 (Connect External Sense to Sense)
14. CPU-En# = 1 (Channel Enabled)

10. Total Chip Calibration Detailed Procedure

The calibration procedure below follows the steps as listed above in the Total Chip Calibration Procedure Outline.

10.1 Monitor/Measure Voltage Calibration Procedure – Once per Chip

Each channel can route an analog voltage to the Central-MU (measurement unit) which can be used to measure various voltages, currents, or internal diagnostic nodes. There are 4 MU ranges of which there are three measure voltage ranges (4V, 8V, and 16V), and one measure current range.

The Monitor/MV calibration is used to compensate for any error in the MV range buffer, monitor output buffer, measurement unit mux selects, or any other path that could introduce errors. The Force Voltage level of the Vesuvius is used to provide the voltage source during calibration. An external voltage reference such as an external SMU (Source Measurement Unit) could also be used to perform this calibration. This calibration procedure performs a relative measurement between the EXT_SENSE pin and the MONITOR and uses the EXT_SENSE measure voltage as the input voltage to the MU path. Absolute accuracy of the Force Voltage level is not essential here since the output voltage is measured on the EXT_SENSE pin which is compared to the voltage measured at the MONITOR pin. The example below is for the 16V range (-2V to +14V). This calibration is applied in software and therefore no hardware registers are used. MUR 1, 2 and 3 should be calibrated, but there is no need to calibrate MUR 0 since it will be calibrated in the measure current section.

Note: In an actual application, the output voltage can optionally measured at FORCE, SENSE, EXT_FORCE, or EXT_SENSE depending on which is most convenient to the system.

10.1.1 Calibration Setup

1. Use Basic Force Voltage Setup

10.1.2 Calibration Procedure for MUR 2

1. Set ForceA# Level = 0x1FFF (Voltage = 0V, DC Level Memory Address 0x0000)
2. Low_out = Measure Voltage at Monitor
3. Low_set = Measure Voltage at Ext-Sense
4. Set ForceA# Level = 0xBFFF (Voltage = 10V, DC Level Memory Address 0x0000)
5. High_out = Measure Voltage at Monitor
6. High_set = Measure Voltage at Ext-Sense
7. Calculate MV Gain = (High_out - Low_out) / (High_set - Low_set)
8. Calculate MV Offset = (High_out)-Gain*(High_set)
9. Store software calibration values for later use.
10. Calibrate all measure voltage ranges using same method. Force Voltage calibration levels can be chosen for optimum performance.

10.1.3 Calibration Value Usage for MUR 2

1. Measure Voltage at Monitor: (VMon)
2. Apply Calibration Values: Measured Voltage = (VMon - Offset)/Gain.

10.2 DAC Calibration – Once per Chip

10.2.1 DAC LSB Calibration (Level DAC Only)

The Level DAC has 16-bit resolution and can be used in either the 8V or 16V range. The nominal resolution in the 8V range is 122uV/code and in the 16V range is 244uV/code. The Vesuvius has a built in LSB (Least Significant Bit) calibration to minimize the amount of DNL (Differential Non-Linearity) error at the Level DAC output (This calibration has no affect on the Gain or Offset DAC). This calibration is performed 1 time per chip since there is only one Level DAC on the Vesuvius that is shared for all levels of the Vesuvius. A write to the LSB-Auto-Cal bit using the CPU port initiates this auto-calibration sequence to optimize for LSB DNL error. The DNL error for a particular LSB code transition is simply the difference between the actual LSB transition step and the ideal measured step. Upon completion of this calibration, the calibration values are stored in Central Resource Registers in the DAC-P/DAC-N (central resource address 6) section in DAC-P<6:0> bits and DAC-N <6:0> bits. The auto-cal will get close to the correct value for the two registers, but for optimum performance 2 additional options are mentioned below. These are listed below in order of best results with the 3rd option giving the best results.

10.2.1.1 LSB Auto Calibration

The calibration sequence is started by writing a 1 to the LSB-Auto-Cal bit in the Central Resource Registers. This bit is can then be polled and when the on-chip hardware is done determining values for the DAC-P and DAC-N registers, the bit will read back as a 0. This process takes about 50ms.

10.2.1.2 Modified LSB Auto Calibration

Perform Auto-Calibration as mentioned in step 10.2.1.1 above. After the calibration has completed, read the calibration values as stored in DAC-P<6:0> and DAC-N<6:0> registers. Add three (+3) to the value read back from DAC-N<6:0> and write back to the same register location. Subtract three (-3) from the value read back from the DAC-P<6:0> and write back to the same register location.

10.2.1.3 Manual LSB Calibration

This procedure examines the DNL error of DAC codes near the midpoint of the Level DAC range and then selects the values for the DAC-P<6:0> and DAC-N<6:0> registers that give the best DNL performance over that range. The actual LSB steps would then be compared to this average step value to determine the DNL error.

Procedure (The details of this procedure will be left to the user):

Configure in Force Voltage Mode. Perform Auto-Calibration as in step 1 above. This will get close to the correct values for the DAC-P<6:0>/DAC-N<6:0> register values. Next a search of one of the DAC LSB calibration register values (DAC-P<6:0> or DAC-N<6:0>) will be performed while holding the other constant. Look at the LSB transition over a range of Level DAC codes. For example: Code 0x7FE5 to Code 0x801C. As a note, since the MSB calibration is calibrated following the LSB calibration step, the 0x7FFF to 0x8000 code transition should be ignored. Once those have been measured, the average LSB step can be calculated and the DNL error for each LSB step determined. The DNL is the average LSB step minus the actual LSB step. Once the DNL errors are known, the measure of goodness is done by summing the absolute value of the magnitude of each DNL error. The register value that produces the lowest sum is the best one. Since the sum is not a signed value, a linear search must be performed starting with the register value the hardware came up with. The search should proceed in the direction that causes the sum of the errors to decrease. Continue searching until the sum starts to increase again, this will find the best value. One register would be searched until the best value is found. That value would be written into that register. Then the other register (DAC-P<6:0>/DAC-N<6:0>) would be searched for the best value.

Note: This can be a very time consuming process.

10.2.2 DAC Cal Bits Calibration (Level DAC Only)

The DAC cal bits are used to correct for any D11-D15 MSB Step errors in the Level DAC and has no affect on the MSB steps for the Gain DAC and Offset DAC. The DAC Cal Bits calibration is only performed once per part since there is only one Level DAC that is shared for all levels on the chip. The lower bits starting with D11 must be calibrated first since they affect the higher DAC Cal Bits. For the following calibration setup to work, the Measure Voltage path needs to be calibrated. For each DAC Cal Bit, the Level DAC is programmed to 2 different cal points to determine the code which gives the best MSB step. In this example, the DAC Cal Bits are calibrated through the MONITOR/MV path using the DPS Force Voltage. The MONITOR Calibration Values computed earlier need to be applied to the raw Monitor output Voltage. The EXT_SENSE, FORCE_#, or SENSE_# pins could also have be used to make the measurement. In this example, the DAC Cal bits are adjusted until they are approximately equal to an LSB step size.

TABLE 1. RECOMMENDED DAC CAL BITS CALIBRATION POINTS

D# Cal Bit	Level DAC Cal Points	High_Code	Low_Code
D11	Do not calibrate (set to code 0x0)	N/A	N/A
D12	Do not calibrate (set to code 0x0)	N/A	N/A
D13	0x1FFF/0x2000	+8	–8
D14	0x3FFF/0x4000	+16	–16
D15	0x7FFF/0x8000	+32	–32

10.2.2.1 Calibration Setup

Use Basic Force Voltage Setup.

10.2.2.2 Determine Actual LSB Step Size

1. Set ForceA# Level = 0x4000.
2. Meas_4000 = Measure calibrated voltage at MONITOR
3. Set ForceA# Level = 0xC000.
4. Meas_C000 = Measure calibrated voltage at MONITOR
5. Expected_LSB_Step (Volts/Code) = (Meas_C000 - Meas_4000) / (0xC000 - 0x4000)

.

10.2.2.3 Calibration Procedure

The following example uses a binary search algorithm to search for optimum calibration values for the DAC Cal bit Codes. Use the following procedure for each of the DAC Cal Bits D13-D15, starting with D13.

Minimum_Step = Absolute value of the minimum DAC MSB step measure. (For first loop in the binary search set artificially to a high value).

Mimimum_Code = DAC MSB Code corresponding to the Minimum_Step measured above.

1. Set DAC Cal Code: Code = (High_Code - Low_Code)/2)
2. Set ForceA# Level = CalPt1.
3. Meas1 = measure voltage at MONITOR
4. Set ForceA# Level = CalPt2.
5. Meas2 = measure voltage at MONITOR
6. Actual_LSB_step = (Meas2 -Meas1) /(CalPt2 - CalPt1)
7. Compare the expected LSB step to the actual LSB step measured:
   DNL_Step = (Actual_LSB_Step - Expected_LSB_Step)
8. Adjust DAC Cal Bit based on step error to search for smallest error:
   If (abs(DNL_Step) < abs(Minimum_Step))
   Minimum_Step = DNL_Step
   Minimum_Code = Code
9. Adjust High_Code or Low_Code based on error:
   If DNL_Step = 0: Search is complete, break out of loop (Set High_Code=Low_Code).
   If DNL_Step < 0: Low_Code = Code.
   If DNL_Step > 0: High_Code = Code.
10. Loop to top while (High_Code - Low_Code) > 1.
11. Use Minimum_Code as the calibration value.

10.2.3 Offset and Gain DAC Calibration

Each DC Level (ForceA#, ForceB#, Cl-Vch-Isrc#, Cl-Vcl-Isnk#) of the Vesuvius has a 16 bit Offset and Gain correction that allows the Level to be programmed to its true post calibrated value. The Offset and Gain DACs are not ideal and have gain and offset errors of their own. A software calibration is used to correct this.

The Offset and Gain DAC use a 4-segment (8-pt) software calibration algorithm to compensate for any potential D14/D15 MSB steps. The Level DAC has hardware to calibrate for MSB steps as mentioned earlier in the calibration section, but it does not affect the Offset or Gain DAC. Since the offset and gain DAC's are 16-bit, the 4-segments chosen are as follows:

TABLE 2. RECOMMENDED OFFSET/GAIN DAC CALIBRATION SEGMENTS

Segment	Low Code	High code	Calcode1 (10% of Range)	CalCode2 (90% of Range)
0	0x0000	0x3FFF	0x0666	0x3998
1	0x4000	0x7FFF	0x4666	0x7998
2	0x8000	0xBFFF	0x8666	0xB998
3	0xC000	0xFFFF	0xC666	0xF998

Note: A 1-segment (2-pt) software algorithm could also be used to simplify the calibration, but a 4-segment calibration algorithm was used for calibration and testing in compliance with the datasheet specs.

This calibration algorithm takes into consideration 3 types of steps: no step, negative step, and positive step. It is also possible to have more than one type of step for any given DAC.

1. No Step: Different segments will have the same (similar) gain/offset correction values.
2. Negative Step: Segments will overlap therefore there are multiple codes to achieve a given value. This algorithm can handle large negative steps without any impact on overall performance.

3. Positive Step: There is a hole (gap) between the segments; therefore, there are certain values that don't have a corresponding code. If the final value happens to fall into this hole, the algorithm should pick the segment end-point closest to the value; this will directly result in an accuracy error.

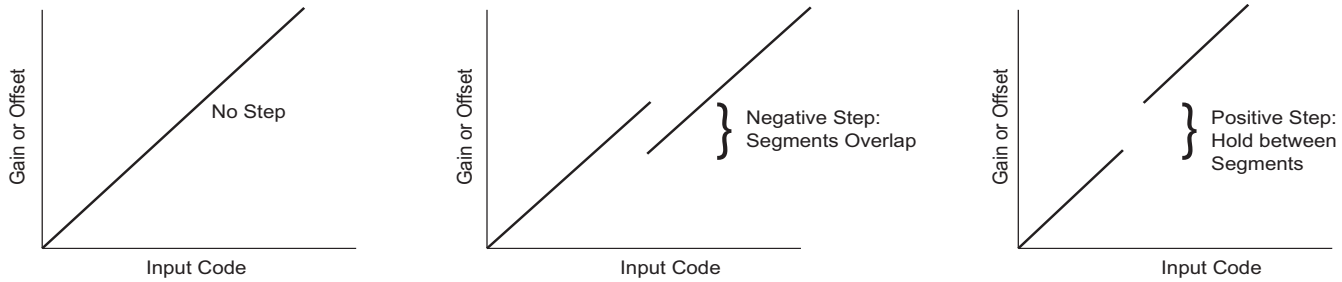

FIGURE 7. OFFSET/GAIN DAC MSB STEP: NO STEP, A NEGATIVE STEP, AND A POSITIVE STEP

10.2.4 Offset and Gain DAC Calibration

10.2.4.1 Offset DAC Equation

1. The calibration equation used for the each of the 4 segments of the offset DAC is as follows:

   Vos = (Offset.Value * OffsetDacCal.gain) + OffsetDacCal.Offset (This is the basic slope intercept formula)

   Vos: the desired offset voltage

   - Offset.Value = the value written to the per-level Offset Ram
   - Offset.Value = (DAC Code / 0xFFFF) * Offset.FS + Offset.Vmin
   - Value.FS = (Full-Scale Voltage Range: 8V or 16V depending on Voltage Range Selected)
   - Offset.FS = 2 * Offset.Vmin
   - Offset.Vmin = Minimum offset voltage
   - Offset.Vmin = -5.4% * Value.FS

2. There are separate offset and gain calibration factors for each segment of the Offset DAC.
3. When programming the device for a desired offset, use the following equation:

   Offset.Value= (Vos-OffsetDacCal.Offset)/OffsetDacCal.Gain

10.2.4.2 Offset Calibration Setup

1. Use Basic Force Voltage Setup
2. Only calibrated in 16V Force Voltage range then divided by 2 for the 8V range. Can be calibrated in both 8V and 16V ranges if desired.
3. Measure Voltage should be calibrated.
4. To minimize the affect of Gain and Voltage level in the following equation:

   Vout = (Value - Vmid) * Gain + Offset + Vmid + DUTGND (as shown in section 7)

   - Set ForceA# Level = 0x7FFF (6V in 16V Range). Since Vmid = 6V in the 16V range, this will cancel out any contributions from the Gain DAC.
   - Set ForceA# Gain = 1.0 (0x7FFF)

10.2.4.3 Offset DAC Calibration Procedure

For each of the 4 offset segments

1. Set ForceA# Offset = CalCode1
2. Meas_low = (Measure Calibrated Voltage at MONITOR) - Vmid
3. Set ForceA# Offset = CalCode1
4. Meas_high = (Calibrated Voltage Measured at MONTOR) -Vmid

5. Calculate Offset DAC Gain: OffsetDacCal.gain = (Meas_high-Meas_low)/(Vhigh-Vlow)
   - Vhigh = Theoretical offset corresponding to CalCode2
   - Vhigh = (CalCode2 / 0xFFFF) * Offset.FS + Offset.Vmin (Section 10.2.4.1)
   - Vlow = Theoretical offset corresponding to CalCode1
   - Vlow = (CalCode1 / 0xFFFF) * Offset.FS + Offset.Vmin (Section 10.2.4.1)
6. Calculate Offset DAC Offset:
   OffsetDacCal.Offset = (Meas_high) - OffsetDacCal.gain * Vhigh

10.2.5 Gain DAC Calibration

10.2.5.1 Gain DAC Equation – The basic calibration equation used for each segment of the Gain DAC is as follows:

1. The basic calibration equation used for each segment of the Gain DAC is as follows:
   Gain = (Gain.Value-GainDacCal.Mid) * GainDacCal.Gain + GainDacCal.Offset + GainDacCal.Mid
   - Gain: the desired gain
   - Gain.Value: the value written to the per-level Offset Ram
   - Gain.Value = (DAC Code/0xFFFF) * Gain.FS + Gain.Vmin
   - Gain.Vmin = 0.75
   - Gain.FS = 0.50 (0.75 to 1.25)
   - GainDacCal.Mid = 1.0 (Mid value of the Gain DAC)
2. There are separate offset and gain calibration factors for each segment of the Gain DAC.
3. When programming the device use the following equation:
   Gain.Value = ((Gain – GainDacCal.Mid – GainDacCal.Offset) / (GainDacCal.Gain)) + GainDacCal.Mid

10.2.5.2 Gain DAC Calibration Setup

1. Use Basic Force Voltage Setup
2. Set FVR # = 0x00 (8V Range)
3. To maximize Gain and minimize Offset in the following equation:
   Vout = (Value-Vmid) * Gain + Vmid + Offset + DUT_GND (as shown in section 7)
   - Set ForceA# Level = Vmax= 6V(0XFFFF).
   - Set ForceA# Offset = 0.0V (This is the post-cal Offset DAC Code).

10.2.5.3 Gain DAC Calibration Procedure

For each of the 4 gain setments

1. Set ForceA# Gain = CalCode1
2. Meas_low= Measure Calibrated Voltage at MONITOR
3. Gain_low= (Meas_low-Vmid-Offset-DUT_GND) / (Vmax-Vmid)
4. Set ForceA# Gain = CalCode2
5. Meas_high= Measure Calibrated Voltage at MONITOR
6. Gain_high= (Meas_high-Vmid-Offset-DUT_GND) / (Vmax-Vmid)
7. Calculate Gain DAC Gain:
   GainDacCal.gain = (Gain_high-Gain_low)/(GainSetHigh-GainSetLow)
   - GainSetHigh = Theoretical gain corresponding to CalCode2
   - GainSetHigh = (CalCode2 / 0xFFFF) * Gain.FS + Gain.Vmin (Section 10.2.5.1)
   - GainSetLow = Theoretical gain corresponding to CalCode1
   - GainSetLow = (CalCode2 / 0xFFFF) * Gain.FS + Gain.Vmin (Section 10.2.5.1)
8. Calculate Gain DAC Offset:
   GainDacCal.Offset = (Gain_high- GainDacCal.Mid) - (GainDacCal.gain * (GainSetHigh - GainDacCal.Mid))

10.3 DC Level Calibration

DC level calibration involves calibration of the gray section in the figure below. It is assumed that all previous calibration has been completed prior to this point.

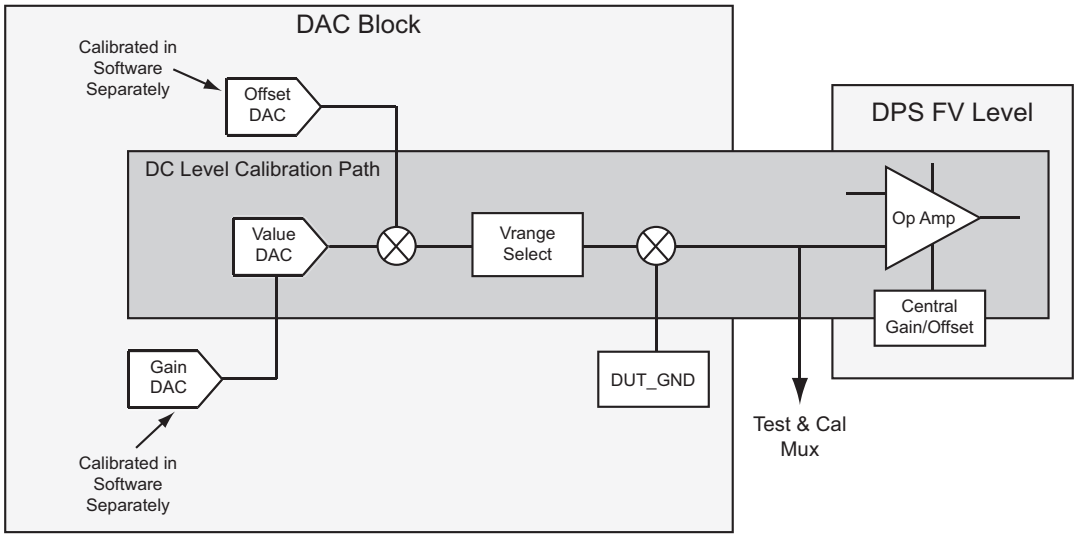

FIGURE 8. DC LEVEL CALIBRATION

The following procedure will produce an Offset/Gain value for the main DC Level DAC. The Offset and Gain DAC values are programmed in the RAM space of the Vesuvius. The actual calibration value written to the Offset/Gain RAM location will use the software Offset DAC and software Gain calibration values found earlier in the DAC calibration section to determine the correct value to be written. In a typical system, the DC calibration would use the EXT_SENSE and EXT_FORCE pins connected to a central PMU and Analog to Digital Converter (A/D).

10.3.1 General DC Level Equation for all DC Levels (Same as Section 7 above)

Vout = (Value-Vmid) * Gain + Vmid + Offset + DUT_GND.

1. Vmid = 2V (8V range, FVR# = 0), 6V (16V Range, FVR# = 1) Corresponds to A Level DAC code of 0x7FFF and is the pivot point of the gain for the Level DAC.
2. Value = Level corresponding to value written to Level DAC location.
3. Gain = Gain corresponding to value written to Gain DAC location.
4. Offset = Offset corresponding to the value written to the Offset DAC location.
5. DUT_GND = Voltage at DUT_GND# pin corresponding to ground at DUT (device under test) .

Note: This DC level equation is a little different than the "slope-intercept" equation discussed at the beginning of this document. This equation represents how the DC Level is implemented in hardware.

10.3.2 General DC Level Calibration Procedure

1. Select DC Level Mode (FV, ICL, etc.)
2. Set Calibrated Gain = 1.0; (Use software Gain DAC calibration value)
3. Set Calibrated Offset = 0.0 (Use software Offset DAC calibration values)
4. Set Output Level1 = Cal Point1
5. Measure Output1
6. Set Output Level2 = Cal Point2
7. Measure Output2
8. Gain = (Output2 - Output1)/(Level2 - Level1)
9. Offset = (Output2 - Vmid) - Gain * (Level2 - Vmid) – DUT_GND
10. Set Offset RAM location = -Offset/Gain
11. Set Gain RAM location = 1.0/Gain

10.3.3 DC Level Calibration: Per Channel

10.3.3.1 Per Channel Central Gain and Offset – Central Resource Mode

The central Gain/Offset calibration will not be discussed in this document and is only needed when using the Central Resource Mode (a DC level is shared between multiple channels). The details of this feature can be viewed in the Central Resource Mode section of this datasheet. For the purpose of the DC level calibration since level sharing is not being used, set the central level Gain (OS#<7:0>) and Offset (AV#<7:0>) to code 0x00.

Note: The Central Gain and Offset registers will automatically be set to 0x00 after a part reset.

10.3.3.2 Force Voltage Calibration

The Vesuvius has 2 separate DAC sources: ForceA# and ForceB# each with 2 voltage ranges (8V and 16V). In addition, there are 2 separate FV modes: Low Current (IR0-IR4) and High Current (IR0-IR5). The High Current mode (FV-Mode=0) uses the VCCO supply to power the output stage and can support all current ranges. The Low Current mode (FV-Mode=1) uses the VCC supply to power the output stage and can support all current ranges except IR5 (512mA Range).

The DAC sources ForceA# and ForceB# for each channel are calibrated separately with a separate calibration value required for each per voltage range and per FV-Mode. The output voltage is measured at the SENSE# pin in the example shown. The EXT_FORCE, EXT_SENSE, or FORCE_# pins could also be used to measure the output voltage or the output voltage could be routed to and measured at the MONITOR pin. The FV only is required to be calibrated in one current range (IR); this same calibration value is applied on all other current ranges.

10.3.3.2 Calibration Setup

Use Basic Force Voltage Setup.

10.3.3.4 Calibration Procedure: The calibration points of 0V and 10V have been arbitrarily chosen for this example and can be changed to fit the needs of the user.

1. Set ForceA# Offset = 0.0V(post-calibration)
2. Set ForceA# Gain = 1.0 (post-calibration)
3. Set ForceA# Voltage Level (Addr 0x0000)= CalPt1 0V (0x1FFF)
4. Vdout1 = Measure Voltage at SENSE_# pin
5. Set ForceA# Voltage Level (Addr 0x0000) = CalPt2 10V (0XBFFF)
6. Vdout2 = Measure Voltage at SENSE_# pin
7. Gain = (Vdout2 - Vdout1) / (CalPt2 - CalPt1)
8. Offset = (Vdout2 - Vmid) - [Gain * (CalPt2 - Vmid)] : For the 16V Range Vmid = 6V
9. Set ForceA# Offset = - Offset/Gain (Convert to hex code using equation is section 8.2)
10. Set ForceA# Gain = 1.0/Gain (Convert to hex code using equation in section 8.1)

10.4 MI (Measure Current) Calibration

The MI calibration is used to compensate for any error in the MI instrument op-amp, MONITOR/MI_MONITOR output buffer, or any other circuitry in the measure current path. This calibration converts a voltage measured at the MONITOR or MI_MONITOR pin and converts it into a current using a linear transfer function. In order to calibrate the full MI path, the Vesuvius needs a load connected either to each FORCE_# pin or the EXT_FORCE pin. Either a central precision SMU(source measurement unit) or precision resistors can be used. In the example used in this section a central precision SMU is used. The MI calibration consists of the following 2 steps:

1. Common Mode Error (CME) calibration -
   - Per channel
   - Per FV-Mode (applies to IR3 and IR4)
   - Per current range
   - CME is a Hardware calibration
   - Can be calibrated through the MONITOR or MI_MONITOR
2. MI calibration
   - Per channel
   - Per current range
   - MI calibration is a software calibration
   - Can be calibrated through the MONITOR or MI_MONITOR

As mentioned earlier in the datasheet, the BBias# bit is used to control the turn-on point of the second stage of the multi-stage output buffer. The following settings are recommended:

TABLE 3. RECOMMENDED BBIAS# BIT SETTINGS

BBias#	Current Range	Comment
0	IR0, IR1, IR2	N/A
1	IR3	N/A
0 or 1	IR4, IR5	Use same BBias# setting for calibrating CME, calibrating MI and measuring current

10.4.1 CME (Common Mode Error)

The purpose of the CME calibration is to compensate for any Measure Current error that exists at the MONITOR/MI_MONITOR due to the variations of the FORCE voltage output level. As the FORCE# output voltage varies up and down along the common mode output range (with the current flow constant), this may cause a common mode voltage error on the measure current instrumentation amplifier. This will show up as a measure current error. In a traditional measure current application shown below, the current flow across a known resistor will give the transfer function of the current forced at the output. This isn't exactly how the Vesuvius works, but it gives a good conceptual view.

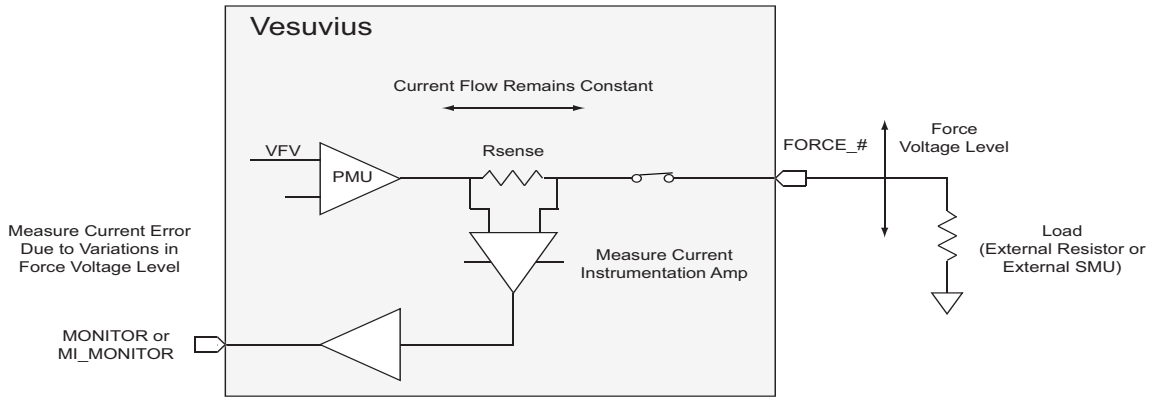

FIGURE 9. TRADITIONAL MEASURE CURRENT APPLICATION

By setting the CME register correctly, the actual transfer function can more closely track an ideal transfer function as shown below.

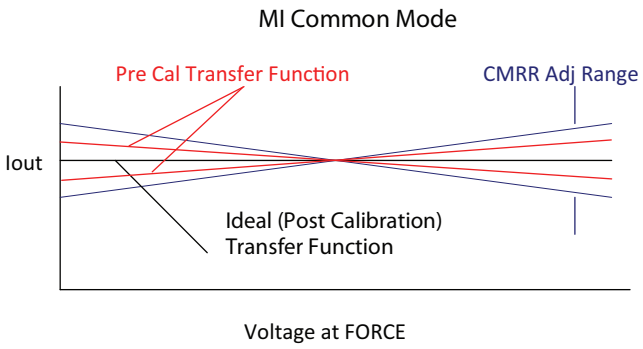

FIGURE 10.

10.4.1.1 CME Calibration Setup

To calibrate the CME, the Vesuvius must be placed in the Force voltage mode with no load on the output. To accomplish this, either remove the load from the circuit or set the SMU to 0 current.

In the following procedure, the MI_MONITOR output is used for the calibration.

1. Use FV Basic setup as shown earlier
2. If Using MONITOR pin instead of MI_MONITOR, MUR = 0 must be selected.
3. Set appropriate BBias# bit

10.4.1.2 CME Calibration Procedure

The common mode error registers are 8-bit, giving 256 codes of adjustment. In the example below, a binary search is performed converging on 2 adjacent codes. The purpose of this procedure is to find the CME code which causes the measure current output at the MONITOR or MI_MONITOR to remain unchanged while adjusting the Force Voltage output level and leaving the current constant. The current in this case is 0mA.

The following example uses a binary search to find the ideal CME code:

Code_hi = 127 (Highest CME Code)

Code_lo = -127 (Lowest CME Code)

Vload = ((VCC + VEE)/2) for FV-Mode=1 (If FV-Mode = 0, Vload = ((VCCO+VEE) / 2))

Volt_low = Vload - 3.0V (Use output voltage 3V below Vload)

Volt_high = Vload + 3.0V (Use output voltage 3V above Vload)

MIN_CME = 999 (Minimum Measured CME - Set Arbitrarily high to begin search)

While (Code_hi - Code_lo > 1) /* Binary Search Until two Adjacent codes are found */

{

Code = (Code_hi - Code_lo) / 2

Write Code to CME register

Set ForceA# Level = Volt_low

MI_ low = Measure voltage at MI_MONITOR

Set ForceA# Level DAC = Volt_high

MI_high = Measure voltage at MI_MONITOR

CME = (MI_high - MI_low) / (Volt_high - Volt_low) /* CME at MI_MONITOR */

If (fabs(CME) < fabs(MIN_CME)) {

```
            CME_Adj = Code;
            MIN_CME = CME;
        }
        if ( CME == 0 ) /* Flat */
        {
            /* Done. Set High=low to break out of loop */
            Code_hi = Code_lo;
        } else if ( CME < 0 )
        {
            /* Raise CME Adj code to increase slope */
            Code_lo = Code;
        } else
        {
            /* Lower CME Adj code to decrease slope */
            Code_hi = Code;
        }
    }
    CME_Adj = Calibrated CME code
```

10.4.2 MI (Measure Current) Calibration

Measure current is calibrated in Force Voltage mode using either the ForceA# or ForceB# level. A separate calibration value is needed for each current range. As mentioned earlier in this document, the measure current calibration factors are applied and stored in software. For Measure current, a positive current indicates sourcing current (flowing out of Vesuvius) and a negative current indicates sinking current (flowing into Vesuvius).

To calibrate the MI, a load must be connected to the FORCE_# or EXT_FORCE output pin. To accomplish this, either an SMU or precision resistors can be used as the load. To measure current, a voltage is measured at the MONITOR or MI_MONITOR pin and this voltage is converted to a current.

The transfer function for measure current (as stated in Table 3 of the datasheet) is as follows: (Imax is the maximum measured current for each current range).

TABLE 4.

Current # FORCE_#	Voltage at MONITOR or MI_MONITOR
+Imax (Vesuvius Sourcing Current)	+2.033V
0	+1.5V
–Imax (Vesuvius Sinking Current)	+0.967V

This table shows theoretical voltages that correspond to the measure current, therefore the actual values will have to be measured and calibration values computed.

MI equation (per current range and per channel): y = mx + b.

1. y = MI_V (Amps): Voltage at MI_MONTOR which is converted to current.
2. x = MI (Amps): Actual current forced at the FORCE_# pin
3. m = MI Gain
4. b = MI Offset

For measure current, a 4-pt/2-segment calibration method was chosen for all current ranges. These segments were chosen to exploit the linear region of the measure current transfer curve in the IR4 (25.6mA) and the IR5 (512mA) current ranges. The MI transfer curve for IR5 is shown below in figure 10. The linear region for the IR4 and IR5 ranges is approximately +10% to +90% of Imax for sourcing current and approximately -10% to -90% of Imax for sinking current. Although a 2-pt/1-segment calibration could have been chosen for IR0-IR3, the same calibration routine was used for all ranges. For the region -10% to +10% of Imax on IR4 and IR5, it is recommended to switch to the next lower current range to measure current. This can be accomplished due to the glitchless range changing capability in all current ranges except IR0.

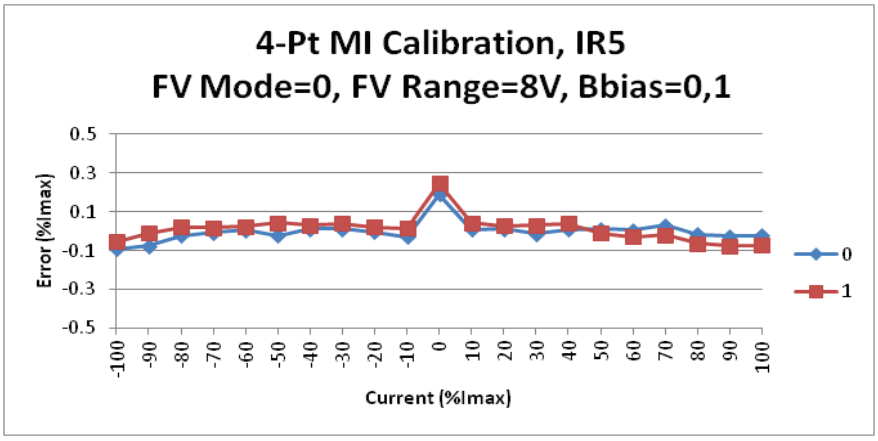

FIGURE 11. MI Transfer Curve IR5 (512mA)

TABLE 5. MI CALIBRATION POINTS

Range	Imax	CalPt1	Calpt2	CalPt3	CalPt4
IR0	±2.56µA	-0.512µA	-2.048µA	+0.512µA	+2.048µA
IR1	±25.6µA	-5.12µA	-20.48µA	+5.12µA	+20.48µA
IR2	±256µA	-51.2µA	-204.8µA	+51.2µA	+204.8µA
IR3	±2.56mA	-0.512mA	-2.048mA	+0.512mA	+2.048mA
IR4	±25.6mA	-5.12mA	-20.48mA	+5.12mA	+20.48mA
IR5	±512mA	-102.4mA	-409.6mA	+102.4mA	+409.6mA

10.4.2.1 MI Calibration Setup

1. Use FV Basic setup as shown earlier.
2. Connect load to FORCE_# pin. In this example, an external SMU is used as the load in Force Current Mode.
3. The EXT_FORCE output could also be used to calibrate MI if a central resource is used for calibration for all pins.
4. Set appropriate BBias# setting.
5. If using the MONITOR pin instead of MI_MONITOR, MUR 0 must be selected.

10.4.2.2 MI Calibration Procedure

1. Set ForceA# Level = 6V
2. Set SMU Force Current to CalPt1
3. MI_1 = Measure MI_MONITOR
4. Set SMU Force Current to CalPt2
5. MI_2 = Measure MI_MONITOR
6. Set SMU Force Current to CalPt3
7. MI_3 = Measure MI_MONITOR

8. Set SMU Force Current to CalPt4
9. MI_4 = Measure MI_MONITOR

10.4.2.3 Apply Calibration Values

1. Gain_sink = (MI_1 - MI_2) / (Iload_1 - Iload_2)
2. Offset_sink = MI_1 - (Gain_sink * Iload_1)
3. Gain_src = (MI_4 - MI_3) / (Iload_4 - Iload_3)
4. Offset_src = MI_4 - (Gain_src * Iload_4)
5. If Sinking current:

   V_Mi = Measure Voltage at MI_MONITOR

   MI = (V_Mi - Offset_sink)/Gain_sink (Use equation in 10.4.2)
6. If Sourcing current:

   V_Mi = Measure Voltage at MI_MONITOR

   MI = (V_Mi - Offset_src)/Gain_src (Use equation in 10.4.2)

10.4.3 Current Clamps Calibration

Each channel of the Vesuvius has current clamps that limit the amount of current that can flow out of or into each of the 8 channels. The current clamps only impact internally generated currents (source or sink current) produced by the output stage of the Vesuvius. These clamps are not intended to be used as a current protection from any externally generated current sources.

When the current clamps are on, the current flow of the output stage is limited internally by reducing the force voltage level of the force voltage DAC until the output current is within the programmed values of the current clamp settings. The sink and source clamps have independent settings.

Changing measure current ranges does not affect source/sink current capability of the Force Voltage output stage. Due to the special architecture of the measure current circuitry, there is no series sense resistor (except IR0) used to measure current from the output stage for ranges IR1 through IR5 (each measure current range can output the same amount of current). The purpose of the measure current range is to set the range of the measure current circuitry and to set the range of the current clamps. As mentioned above, IR0 is different from the other ranges. IR0 uses a 100KΩ resistor in series with the output to measure fine current, but this does not limit the ability of IR0 to output full current. All current ranges have a maximum current flow of approximately 768mA when the clamps are disabled.

The current clamps have very low gain by design. As a user, this means the following:

1. The clamps are very fast and can respond very quickly to a change in current. This prevents a fast current glitch above the current clamp setting.
2. Since the clamps are low gain, they do not operate consistently across the force voltage common mode range. This shows up as an error as the force voltage level changes with the same current clamp setting. For example: If the clamp is engaged at 1uA, the current sourced by the part could be approximately 1µA at 2V, but 1.2µA at 3V, and 1.4µA at 4V.
3. The clamps were designed to be for basic bulk protection for the DUT and not a precision feature.

Current clamps in IR1 have a known stability issue and are not recommended for use. The current clamps can be used in all other ranges.

Current Clamp Calibration:

There are several methods for calibrating the current clamps. Listed below a few that are used in practice:

1. Calibrate the clamp by looking for a predetermined change in the output force voltage level as the current clamp is starting to engage. As stated above, the clamps work by reducing the force voltage level on the output stage when the clamps are on. This calibration method involves measuring the output voltage at the load as the shown in the figure below:

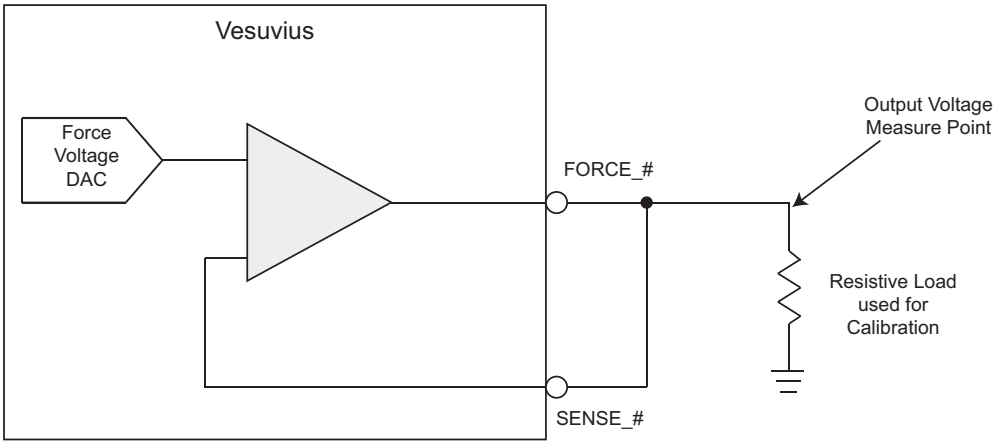

FIGURE 12.

Example: If calibrating IR0, the user would place a resistor (1MΩ in this example) at the output, turn on the clamps, and set the clamp calibration value (example 2µA). Next, the force level is moved until the output voltage error changes by a predetermined amount (15mV in this case). This will provide the user with the level at which the clamps start to affect the force voltage level. This will not however, give the user a hard turn off value for clamping. The gain and offset registers for the current clamp are designed for this type of calibration.

2. Calibrate very similar to the above method, but use the current alarm to provide the feedback when the clamps engage. The amount of change in output voltage depends on the current range selected, but the output voltage typically will change approximately 200mV before the over current alarms turn on.
3. Clamp the current at a hard clamp value. This calibration technique does not look for a change in output voltage, just a fully clamped current.

When using method 3 above, the offset and gain DACs are not used in the calibration and are just set to a default value and not used.

Example Calibration for IR0:

10.4.3.1 Calibration Setup

1. Use Basic Force Voltage Setup (as shown in figure 6 of appendix A in the Datasheet).
2. Set Sel-MI-CI# = 1
3. Set-C-En# = 1
4. Set IR#<5:0> = 0x01 (IR0, 2.56µA)
5. Connect a load on the FORCE_# pin. The load can either be a Source Measurement Unit or an actual resistor. If a resistor is chosen, it must be a precision resistor or calibrated to the resistance.
6. Set the Feedback option using the Sense pin.
7. Set CI-Vch-Isrc#<15:0> Offset = 0x7FFF (Offset = 0uA, DC Offset Memory Address 0x0012)
8. Set CI-Vch-Isrc#<15:0> Gain = 0x7FFF (Gain = 1.00, DC Gain Memory Address 0x0022)

10.4.3.2 Calibration Procedure

The procedure in this example looks for a force voltage output change from the expected value at the load. This is Method 1 mentioned above, and in this example the calibration looks for a 10mV change in the programmed output voltage vs actual measured voltage. In this case, a resistor is used as the output load. This calibration focuses on the I-CI-Src#<15:0> level in current range IR0. The clamps are calibrated at 25% and 75% of full-scale value. As mentioned above, this is only one option for calibration.

Please refer to the following table for the current clamp ranges according to current clamp range. (Minus sign (-) denotes sinking into the Vesuvius). The current clamps are sized to 1.5 * measure current range.

TABLE 6.

Current Range	Measure Current Range	Cl-Vch-Isrc#<15:0> or Cl-Vcl-Isnk#<15:0> = (0x0000)	Cl-Vch-Isrc#<15:0> = (0xFFFF)	Cl-Vcl-Isnk#<15:0> = (0xFFFF)	Offset DAC Range –5.4%FS to +5.4%FS	Gain DAC Range
IR0	±2.56µA	0.00µA	+3.84µA	–3.84µA	±0.207µA	0.75 to 1.25
IR1	±25.6µA	0.00µA	+38.4µA	–38.4µA	±2.07µA	0.75 to 1.25
IR2	±256µA	0.00µA	+384µA	–384µA	±20.7µA	0.75 to 1.25
IR3	±2.56MA	0.00µA	+3.84mA	–3.84mA	±0.207mA	0.75 to 1.25
IR4	±25.6MA	0.00µA	+38.4mA	–38.4mA	±2.07mA	0.75 to 1.25
IR5	±512MA	0.00µA	+768mA	–768mA	±41.47mA	0.75 to 1.25

1. Calibrate the Force Voltage output level. (See section 10.3.3.4 of appendix A in the datasheet).
2. Set ForceA# Level = 0x5FFF (Voltage = 1V(8V Range), DC Level Memory Address 0x0000)
3. Connect 1MΩ resistor from FORCE_# output pin to ground.
4. Set Cl-Vch-Isrc#<15:0> Level = 0x4000 (DC Level Memory 0x0002). 0x4000 = 0xFFFF * 25%
5. Move the ForceA# Level up and down until the force level varies by 10mV from its expected value. ((Expected Voltage – Output Voltage) = 10mV implies that the clamps are starting to engage).
6. Measure the voltage at the SENSE_# pin using the MONITOR pin (SenseV_Low = Voltage measured at MONITOR pin).
7. Calculate the output current of the FORCE_# pin for the low calibration value (MeasI_Low = SenseV_Low/Resistance).
8. Set Cl-Vch-Isrc#<15:0> Level = 0xC000 (DC Level Memory 0x0002). 0xC000 = 0xFFFF * 75%
9. Move the ForceA# Level up and down until the force level varies by 10mV from its expected value. (Expected Voltage – Output Voltage) = 10mV. This implies the clamps are starting to engage.
10. Measure the voltage at the SENSE_# pin using the MONITOR pin (SenseV_High = Voltage measured at MONITOR pin).
11. Calculate the output current of the FORCE_# pin for the high calibration value (MeasI_High = SenseV_High/Resistance).
12. Calculate the gain and offset equation for the clamps.

Desired_current_clamp_setting (hex code) = (Gain * Cl-Vch-Isrc#<15:0>) + Offset

Gain = (MeasI_High - MeasI_Low)/(0xC000 - 0x4000) (mA/code)

Offset = MeasI_High - Gain*(0xC000) (mA)

13. To set a calibrated current clamp current, the user can use the following equation to set the register value. This equation provides a hex value that can be loaded into the Cl-Vch-Isrc#<15:0># register space (Address 0x0002).

    Code = (ClampSetting - Offset)/Gain

    ClampSetting = Desired current clamp value (mA)

Note: As the output current of the FORCE_# pin becomes equal with the calibrated clamp value, the clamps will start to turn on and the user will see the force voltage change by approximately 10mV. As the current gets bigger and bigger, the output voltage will drop more and more from the programmed value until the clamp starts to turn on hard. The hard clamping current is approximately 20% more than the programmed value. This calibration technique is sometimes used as some users are more worried about the absolute accuracy of the force voltage output level versus the clamped current value. Due to the low gain of this circuit as noted previously, the clamp current can vary across the common mode voltage range. A more comprehensive calibration technique can be employed to take the common mode voltage changes into account, but is not discussed in this appendix.

10.4.4 Force Current Calibration

As mentioned above in the datasheet, there are two ways to create a programmable current using Vesuvius:

1. Using current clamps: Force current is implemented by placing the part in Force Voltage mode and using the current clamps to set the current value supplied to the DUT. The force voltage output level is used as a voltage clamp in this method.
2. Using MI feedback to the FORCE amplifier: This method provides traditional FI functionality and improved accuracy versus method 1.

This example uses method 2 above to calibrate the Force Current Level.

General comments when calibrating FI (Force Current):

1. Voltage Clamps are available on the Vesuvius. The user needs to make sure when setting the part up in Force Current Mode that the Voltage Clamps are set to a proper level first so that if the Vesuvius output does go open loop (with no load), the voltage clamps will protect the DUT.
2. When changing to Force Current Mode always have a load connected to the Force_# output. If a load is not connected, the output level will go to one of the output supply rails unless the on-chip voltage clamps have been configured properly.
3. Each current range should be calibrated separately. (IR0-IR5)
4. An external load is needed for calibration. There are several options for this, including the following:
   a. External precision resistors. For this option an ADC/DMM is needed to measure the voltage across the precision resistors in order to calculate a current. This option might introduce some common mode errors to the measurement that need to be taken into account.
   b. External SMU/PMU. (Source/Parametric Measurement Unit)
   c. Use another calibrated channel of the device. (This channel must be calibrated for FV/MI)
5. Force Current uses Chip Ground as a reference. DUT_GND for the Force Current level is not used. Therefore, the general DC levels equation discussed above becomes: Vout = (Value-Vmid) * Gain + Vmid + Offset. Please note that Vout in this case is a voltage that corresponds to a desired force current value.
6. Vmid should also be set to 0 in the above equation. In the Force Current Ranges, Vmid is always 0. This results in the following equation: Vout = Value * Gain + Offset.
7. The EXT_FORCE pin can also be used as an option to connect to the central calibration mux. This path does have more resistance than the FORCE_# pin path, which should be taken into account.
8. As mentioned earlier, the Vesuvius product has 2 separate DAC sources: ForceA# and ForceB#. Either of the 2 levels can be used for Force Current.
9. For best overall accuracy, CME (Common Mode Error) adjust bits should also be calibrated prior to Force Current Calibration.

Below is an example of calibrating the Force Current Level in Vesuvius. This example uses the IR2 (2.56mA) current range. When connecting Vesuvius to an external SMU/PMU, Vesuvius is connected in Force Voltage mode and then switched to Force Current Mode after the parts are connected and enabled. When connecting Vesuvius to a SMU/PMU, the programmed voltage of the Vesuvius FORCE_# output should match the PMU/SMU. If the voltage is not known of the PMU/SMU, the voltage should be measured at the PMU/SMU output before enabling Vesuvius. The voltage can then be programmed into the Force Level before enabling the output. This will connect both outputs at the same voltage. This will reduce the glitch seen at the load (PMU/SMU). Vesuvius can also be connected in Force Current Mode with the Voltage Clamps enabled and set. The figure below shows the basic setup for the calibration procedure discussed.

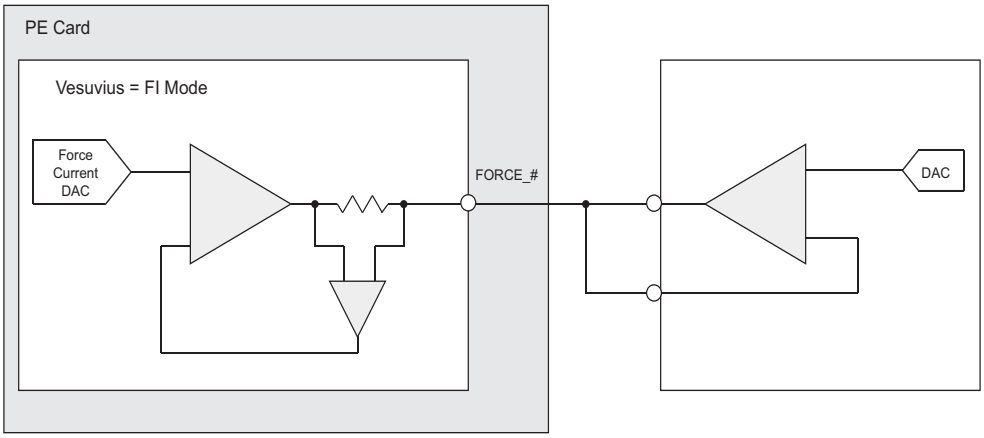

FIGURE 13. Calibration Setup Using External PMU/SMU

Calibration Setup:

1. Reset Vesuvius. This will place to part in HiZ and reset all the register values to '0'.
2. Connect an external SMU/PMU in Force Voltage mode to the DOUT pin of Vesuvius.
   a) Set the voltage of the external SMU/PMU to 0V.
   b) Set current range of the external PMU to match the range on the Vesuvius chip that is being calibrated.
   c) Enable the external SMU/PMU
3. Configure the Vesuvius for Force Current: A more detailed version of this configuration is available in the Vesuvius Quick Start App Note and in the Force Current section of this datasheet. All registers are assumed to be default after resetting Vesuvius. A reset does not however affect the Level DAC settings. Vesuvius will default to the 8V range, ForceA# Level selected, FV mode, output disable and Tight Loop feedback.
   a) Set the ForceA# level = 0V.
   b) Set the ForceB# level to be 0mA (0x7FFF).
   c) Set desired Current Range.
   d) Set ForceA# and ForceB# Offset DAC = 0 (post calibration).
   e) Set FV-Mode# = 1. This uses VCC as the supply for the output current when using IR0-IR4.
   f) Set ForceA# and ForceB# Gain DAC = 1 (post calibration).
   g) Set MUR#<1:0> = 3. This will set the measure voltage range to 16V, which is used by the Voltage Clamps when the part is switched to FI Mode.
   h) Set Voltage Clamp Hi and Voltage Clamp Low levels (Cl-Vch-Isrc# and Cl-Vcl-Isnk#).
   i) Enable the force voltage output (CPU-En#=1).
   j) Take Vesuvius out of Tight Loop (Tight-Loop*# = 1). This will use the Force# output as the feedback to the main amplifier.
   k) Set Vesuvius to Force Current and switch from ForceA level to ForceB level in same register write. (FI/FV*# = 1, CPU-D#<1:0> = 1). For example, using channel 0 write the following: Address = 0x8040/Data = 0x4980

Calibration Procedure:

1. Set the SMU/PMU voltage level to (VCC + VEE)/2. This is used when FV-Mode#=1. If FV-Mode#=0, set the level to (VCCO+VEE)/2.
2. Set ForceB# Level = CalPt1 (1.6mA). (Write 0xCFFF to DC level Memory Address 0x0041)
3. Measure Current = IDout1 (Current Measured at external PMU/SMU)
4. Set ForceB# Level = CalPt2 (-1.6mA). (0x2FFF to DC level Memory Address 0x0041)
5. Gain = (IDout1 - Idout2)/(CalPt1 - CalPt2)
6. Offset = (IDout2) - Gain * CalPt2
7. Write Calibration Values to Gain/Offset Registers. Gain and Offset registers should be programmed to produce an inverse Gain and negative Offset to the values calculated.
   a) Offset = Offset * (-1.0/Gain)
   b) Gain = 1.0/Gain

Note: Force Current DAC code calculation. This example uses IR2 for the calculation 2.56mA.

1. Force Current Level = -FS (Full Scale) to +FS (Full Scale)
2. 0x0000 = -FS Value (In IR2; -FS = 2.56mA)
3. 0XFFFF = +FS Value (In IR2; +FS = 2.56mA)
4. Level DAC Value = ((DAC Code/0xFFFF) * TotalSpan) + IMin
   a) TotalSpan (IR2) = 5.12mA
   b) IMin (IR2) = -2.56mA
5. For example: 1.6mA = ((0xCFFF/0xFFFF) * 5.12mA) + (-2.56mA)