Saturn Quick Start Application Note

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This document contains information on a product under development. The parametric information contains target parameters that are subject to change.

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1 Introduction

This document describes the steps to perform an initial system check-out of the Saturn device.

These instructions assume the customer system can set the Saturn supplies, provide a PLL Clock, has a mechanism to read/write registers, has the ability to measure voltages (either using an external DMM or system resource), provide a simple DATA stream, and so on.

Important Note: The steps described below illustrate a cause and effect to demonstrate how to interface with the device. In a normal application; sequencing, calibration and other factors may require the registers to be written in a different order. Please refer to the Elevate Semiconductor Software Driver documentation for details.

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1.1 Reset State

Whenever a Hardware or Software reset is issued, the device is configured into the following state.

Note: The examples rely on the default (reset) configuration to demonstrate the minimum register transactions to achieve the desired configuration. In a customer application, a Reset should only be issued on first power-on. When reconfiguring the device for different modes, the application should only change the pertinent registers. There are some registers (i.e. PLL Config) that only need to be set one time after power on; otherwise if the Reset was issued while reconfiguring for a different mode, it could be possible the PLL to become momentarily unlocked and could cause unexpected results.

- RAM – Unknown at power ON. Left unchanged if reset issued from a previous configuration
  - SRC/SNK, see section 1.1.2
- Registers – all registers are initialized to ‘0’; which implies:
  - Driver (PMU) Block
    - Driver is in Hi-Z mode
    - Tight loop
    - DriverBias = Mid code
    - SR-Adj = Min code; see section 1.1.1
    - Data/En sourced from CPU control
    - Deskews disabled
    - All switches and IR open
    - Data/En Input Termination none
    - Voltage Range 0
    - Monitor/MonGndRef is in Hi-Z
    - CBits HiZ
  - Comparator Blocks
    - COMP pins sourced from CPU control
    - Deskews disabled
    - Voltage Range 0
    - Active Load HiZ (all switches open)
  - Central Registers
    - Vmid = 0 (which allows for -1.875V to 2.125V in VR0)
    - No PLL input termination
    - PLL FClamps set to ‘0’.
    - DAC Cal Bits uncal’ed
    - Diff-Z open

1.1.1 Slew Rate Adjust (SR-Adj)

The default Slew Rate Adjust (SR+/SR-) code is 0x00 (min code). This setting can cause unpredictable Driver levels and is not supported. It is recommended to set SR-Adj to the mid code or higher.
Mid code = 0x0F and Max code = 0x1F.

1.1.2 SRC/SNK Value DAC RAM Contents

The RAM contents do not have a power on default state and will come up randomly. Therefore the SRC and SNK may power up in a high than expected power state. The application should write the RAM contents to a proper default value after the reset is issued.

1.2 Set Saturn Supplies

The first step is to apply the appropriate voltage. After power is applied, it is recommended to toggle the hardware reset (active high) on Saturn device or issue the Software Reset (register 0xC002).

Verify the voltage at the Saturn pins or within close proximity to ensure there are no IR drops. In addition, the customer should verify the approximate current flow for each supply.

Note: In most systems, it may not be possible to measure the supply currents.

Table 1: Power-ON Current Values

Supply	Voltage (V)	Approximate Current (mA) (3)	
		Reset State	SR-Adj = 0x0F (mid)
VCC (1)	27	110	130
VEE (1)	-5.0	130	150
VDD	3.3	180	180
VREF	3.0	0	0
VOH (2)	3.3	0	0
VOL (2)	0.0	0	0

Notes:
1) VCC and VEE supply voltages are application dependant
2) The VOH and VOL should have minimal current since the COMP pins are in a static state.
3) The current values assume the SRC & SNK Value DAC was programmed to 0x0000.

1.2.1 Measure REXT and CAP_PLL Voltages

The next step is to measure voltage of the REXT and CAP_PLL pins.

REXT voltage should track the VREF voltage within approximately 25mV.

The CAP_PLL voltage is a function of the PLL_CK. In addition, the CAP_PLL voltage is dependant on the Fclamp registers. Table 2 lists the CAP_PLL vs PLL_CK assuming the power-ON default Fclamp (00b) settings.

Table 2: Default CAP_PLL Voltages

PLL_CK (MHz)	CAP_PLL (V)
50.0	1.15
75.0	1.4
100.0	1.65

1.3 Register/RAM Access (CPU Port Transactions)

The following steps perform simple register/RAM access (write/read) to verify to CPU port is functioning.

1.3.1 Read Die ID Register

Read the Die ID registers (address = 0xC07F); Table 3 lists the expected return values for different silicon revisions.

Table 3: Die ID Register Values

Rev	Read-back Data (HEX)
8	0x0788
#	0x078#

1.3.2 Register Access

Follow Table 4 to verify the basic ability to write/read registers. The following bullet items highlight some key aspects of a register access:

- Address bit D15 (Register Bit) must be ‘1’ to access a register
- Address bit D14 (Central Bit) is used to distinguish between Per-Chan and Central Registers
- WE bit must be ‘1’ for the corresponding Data Group bits to be written
- WE bits (typically) read back ‘0’
- Writing to Undefined Data bits has no effect
- Undefined Data bits (typically) read back ‘0’
- A RESET sets all registers to a default value of ‘0000’ (except Read-Only registers)
- Refer to the CPU Protocol Timing diagram for details

Table 4: Write/Read Registers

Description	Address (HEX)	Write Data (HEX)	Read Data (HEX)
Ch#0: Set SR-Adj (+/-) = Max (0x1F) And DrvBias = Mid (0)	0x8001	0x8FFF	0x07DF
Ch#0: Set SR-Adj+ = Mid (0x0F) DrvBias and SR- not changed	0x8001	0x0BC0	0x03DF
Ch#0: Set SR-Adj- = Mid (0x0F) DrvBias and SR+ not changed	0x8001	0x002F	0x03CF
Central Reg: Software RESET	0xC002	<don’t care>	0x0000 (all registers)

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1.3.3 RAM Access

Follow Table 4 to verify the basic ability to write/read RAM. The following bullet items highlight some key aspects of a RAM access:

- The Read-back Data matches the Written Data
- Address bit D15 (Register Bit) must be ‘0’ to access the RAM
- A RESET does NOT set the RAM contents to a default value. They are left unchanged
- A RAM read-back requires 2 additional clock cycles
- Refer to the CPU Protocol Timing diagram for details

Table 5: Write/Read Registers

Description	Address (HEX)	Data (HEX)
Ch#0: DVH Value DAC	0x0000	0xFFFF
Ch#0: DVH Offset DAC	0x0020	0xAAAA
Ch#0: DVH Gain DAC	0x0040	0x5555
Ch#1: CVA Value DAC	0x0082	0xABCD
Parallel Write: DVL Offset DAC (need to set ‘Parallel Load’ bit)	0x0021	0x1234 (read on all chans)

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1.4 Set Driver (DVH/DVL) Level

The following steps are used to output a Driver voltage at DOUT_#. The CPU-Data/En register control bits are used to set the driver state: Set CPU-Data high for DVH and low for DVL.

Notes:
1) The DVH voltage must be greater than the DVL voltage otherwise the Driver Levels will not match the expected value.
2) The 'Output Voltage' is the approximate voltage since these are un-calibrated settings.
3) The achievable output voltage will be a function of VCC/VEE headroom.

Table 6: Set Driver DVH/DVL Levels

Description	Address (HEX)	Data (HEX)	DOUT Output Voltage
Software Reset	0xC002	<don't care>	High-Z
Set SR-Adj (+/-) = Max (0x0F) And DrvBias = Mid (0)	0x8001	0x8BEF	High-Z
Ch#0: Set DVH = 1.0V (default is VR0, Vmid code=0)	0x0000	0xB7FF	High-Z
Ch#0: Set DVH Offset = 0.0	0x0020	0x7FFF	High-Z
Ch#0: Set DVH Gain = 1.0	0x0040	0x7FFF	High-Z
Ch#0: Set DVL = -1.0V	0x0001	0x37FF	High-Z
Ch#0: Set DVL Offset = 0.0	0x0021	0x7FFF	High-Z
Ch#0: Set DVL Gain = 1.0	0x0041	0x7FFF	High-Z
Ch#0: Set CBitA (close Relay2) (Route DOUT to EVM SMA; this step may vary depending on customer hardware configuration)	0x8006	0x5000	High-Z
Ch#0: Enable Driver (CPU-En = 1) and set Driver High (Data = 1)	0x8000	0x012D	1.0 (DVH)
Ch#0: Set DVH = 2.125V	0x0000	0xFFFF	2.125
Ch#0: Set Voltage Range 1 (VR1)	0x8044	0x0005	4.25 (RAM contents don't change)
Ch#0: Set Voltage Range 2 (VR2)	0x8044	0x0006	8.5 (RAM contents don't change)
Ch#0: Set Driver Low (Data = 0)	0x8000	0x0004	-4.0 (DVL)
Ch#0: Set DVL = -2.0V Driver already in VR2	0x0001	0x57FF	-2.0
Central: Set Vmid = code 4 (-5.5V to +11V in VR2)	0xC003	0x0014	0.0 (output shifted up by 2V)

Note: Repeat the above steps for other channels.

1.5 Driver/Comparator Outputs (Real Time DATA)

The following steps configure the Driver (DATA) and Comparator paths for real-time data. The EN path is enabled using the CPU Enable control bit.

Table 7: Driver/Comparator Output Waveforms

Description	Address (HEX)	Data (HEX)	DOUT_# Output	COMPA/B_# Output
Software Reset	0xC002	<don't care>	High-Z	Digital Low
Set SR-Adj (+/-) = Max (0x0F) And DrvBias = Mid (0)	0x8001	0x8BEF	High-Z	Digital Low
Central: Set Fclamp & PLL Term based on PLL_CK	0xC004	See Datasheet	High-Z	Digital Low
Central: Set Vmid = code B (-0.5V to +3.5V in VR0)	0xC003	0x001B	High-Z	Digital Low
Ch#0: Set DVH = 3.0V (Driver defaults to VR0)	0x0000	0xDFFF	High-Z	Digital Low
Ch#0: Set DVH Offset = 0.0	0x0020	0x7FFF	High-Z	Digital Low
Ch#0: Set DVH Gain = 1.0	0x0040	0x7FFF	High-Z	Digital Low
Ch#0: Set DVL = 0.0V (Driver defaults to VR0)	0x0001	0x1FFF	High-Z	Digital Low
Ch#0: Set DVL Offset = 0.0	0x0021	0x7FFF	High-Z	Digital Low
Ch#0: Set DVL Gain = 1.0	0x0041	0x7FFF	High-Z	Digital Low
Ch#0: Set CVA = 1.5V (Comparator defaults to VR0)	0x0002	0x7FFF	High-Z	Digital Low
Ch#0: Set CVA Offset = 0.0	0x0022	0x7FFF	High-Z	Digital Low
Ch#0: Set CVA Gain = 1.0	0x0042	0x7FFF	High-Z	Digital Low
Ch#0: Set CVB = 1.5V (Comparator defaults to VR0)	0x0003	0x7FFF	High-Z	Digital Low
Ch#0: Set CVB Offset = 0.0	0x0023	0x7FFF	High-Z	Digital Low
Ch#0: Set CVB Gain = 1.0	0x0043	0x7FFF	High-Z	Digital Low
Ch#0: Set CBitA (close Relay2) (Route DOUT to EVM SMA; this step may vary depending on customer hardware configuration)	0x8006	0x5000	High-Z	Digital Low
Ch#0: Set DATA Term=100ohms (setting may vary based on customer hardware config)	0x8006	0x0005	High-Z	Digital Low
Ch#0: Enable Driver (CPU-En=1) and source Driver from DATA pin	0x8000	0x012D	Matches DATA_0 input	Digital Low
Ch#0: Set Real-Time Comparator	0x8040	0x0030	Matches DATA_0 input	Matches DOUT_0 state

Note: Repeat the above steps for other channels.

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1.6 Monitor Output

The following steps use the internal Test & Cal diagnostic mux to output a known voltage at the MONITOR pin.

Note: The ‘Output Voltage’ is the approximate voltage since these are un-calibrated settings.

Table 8: Monitor Output

Description	Address (HEX)	Data (HEX)	MONITOR Output
Software Reset	0xC002	<don’t care>	High-Z
Set SR-Adj (+/-) = Max (0x0F) And DrvBias = Mid (0)	0x8001	0x8BEF	High-Z
Central: Set Vmid = code B (-0.5V to +3.5V in VR0)	0xC003	0x001B	High-Z
Ch#0: Set DVH = 3.5V (defaults to VR0)	0x0000	0xFFFF	High-Z
Ch#0: Set DVH Offset = 0.0V	0x0020	0x7FFF	High-Z
Ch#0: Set DVH Gain = 1.0V	0x0040	0x7FFF	High-Z
Ch#0: Set Sel-Diag mux to source from DVH DAC (code 17) and Enable Monitor	0x0007	0x031C	3.0V

1.6.1 Measure Junction Temperature

The following steps show how to measure and calculate the junction temperature using the internal temperature sensors.

$Tj = (Va - Vb) * 1637 - 221$

The measured temperature will be dependant on if there is a heat sink and/or air-flow present.

Table 9: Measure Junction Temperature

Description	Address (HEX)	Data (HEX)	MONITOR Output
Software Reset	0xC002	<don’t care>	High-Z
Set SR-Adj (+/-) = Max (0x0F) And DrvBias = Mid (0)	0x8001	0x8BEF	High-Z
Ch#0: Set Sel-Diag mux to source from Va-Tj (code 2) and Enable Monitor	0x0007	0x022C	Measure Va (expect ~2.2V)
Ch#0: Set Sel-Diag mux to source from Va-Tj (code 3)	0x0007	0x0230	Measure Vb (expect ~2.0V)
Apply above formula			

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1.7 PMU Force Current (FI) Mode

The following steps configure Channel#0 into PMU FI mode and current range IR2 (2mA). In this range, the internal Rsense is located between the DOUT and DIN pin so the current flows out the DIN pin. The Relay2 relay is open so that DOUT and DIN are not connected externally.

The I-Alarm High DAC is used as the reference voltage when in FI mode and the DATA source must be set High (either using CPU control or from DATA pin). The IAH DAC Voltage to Current relationship is:
+/-1V = +/-Imax where Imax = 1 / Rsense

A load needs to be connected to the DIN_0. If no load is present then the FI will cause the PMU to output a voltage at one of the supply rails. The PMU is connected to the DIN_0 prior to switching into FI mode to prevent a large glitch.

Notes:
1) if the part is put into FI mode before connecting to the DIN pin then the internal voltage will go to one of the supply rails, therefore when the PMU is connected it will cause a glitch on DIN#.
2) The 'Output Current' is the approximate current since these are un-calibrated settings.

Table 10: PMU Force Current (FI) Mode

Description	Address (HEX)	Data (HEX)	DIN_# Output
Software Reset	0xC002	<don't care>	High-Z
Set SR-Adj (+/-) = Max (0x0F) And DrvBias = Mid (0)	0x8001	0x8BEF	High-Z
Ch#0: Set IAH (FI) = 0.0V (0uA)	0x0008	0x7FFF	High-Z
Ch#0: Set IAH (FI) Offset = 0.0	0x8028	0x7FFF	High-Z
Ch#0: Set IAH (FI) Gain = 1.0	0x8048	0x7FFF	High-Z
Ch#0: Set FI mode to 2mA (IR2). This sets IR, MI+/-, & Sel-FB=7 (PMU will be connected to DIN)	0x8005	0x3F6C	High-Z
Ch#0: Set EN=High and DATA=High (CPU control)	0x8000	0x002D	~0.0V (FI Mode)
Ch#0: Set IAH (FI) = 1.0V (2mA)	0x0008	0xFFFF	voltage depends on load

1.8 Elevate Semiconductor Software Driver and Documentation

At this point, the customer has demonstrated the basic ability to configure the device, set some levels, make some measurements, and output a driver waveform. This should imply the Saturn device has been properly designed and assembled into the customer system.

The next step is to integrate the Elevate Semiconductor software driver (reference/example code) which allows the customer to:

- Configure the device for different modes
- Perform DC calibration
- Set Levels as a function of voltage rather than HEX codes
- Set Deskews
- Configure the PMU for different modes; including proper sequencing
- And more

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2 Document Revision History

Revision	Date	Description
A01	07/31/2007	Initial Draft

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