Low Cost, Dual Channel, 15V Pin Electronics Driver/Window Comparator

The Kilimanjaro is a dual-channel pin electronics driver and window comparator product fabricated in a wide voltage Bi-CMOS process. It is designed specifically for Test During Burn-In (TDBI) applications and low cost testers where cost, functional density, and power are all at a premium.

The Kilimanjaro incorporates two channels of programmable drivers and window comparators into a small 5mm x 5mm QFN package. Each channel has per pin driver levels, data, and high impedance control, along with per-pin high and low window comparator thresholds levels.

The Kilimanjaro was specifically designed to offer a low cost, high density driver and window comparator solution with excellent small swing performance and stable timing characteristics.

A 15V driver output and receiver input range allow the device to interface directly with TTL, ECL, CMOS (3V, 5V, and 7V), LVCMOS, and custom level circuitry, as well as high voltage levels required for many special test modes in Flash Devices and for stressing devices under test.

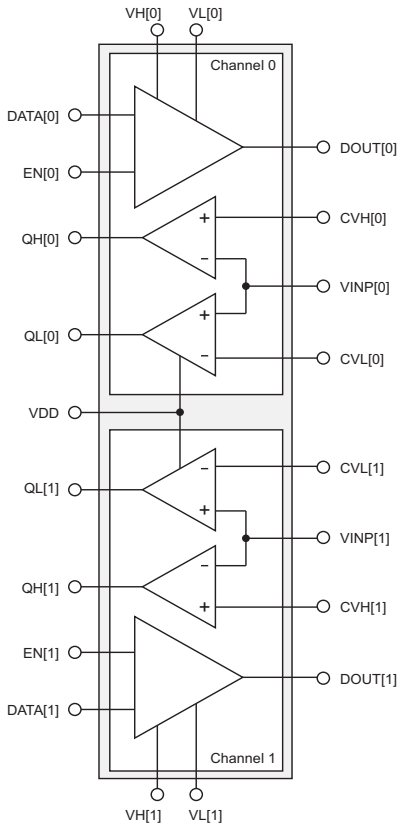
Applications

- Burn-In ATE
- Low Cost ATE
- Instrumentation

Features

- 15V I/O Range
- 125mA DC Current Capability
- 100MHz Operation
- Per-Pin Flexibility
- Programmable Input Thresholds
- LVTTL Compatible I/O
- Small Footprint 5mm x 5mm QFN with Exposed Heat Slug
- Improved Small Signal Swing and Timing Performance
- Low Preshoot/Overshoot/Undershoot
- Pin and Functionally Compatible with E7801 and E7802

Functional Block Diagram



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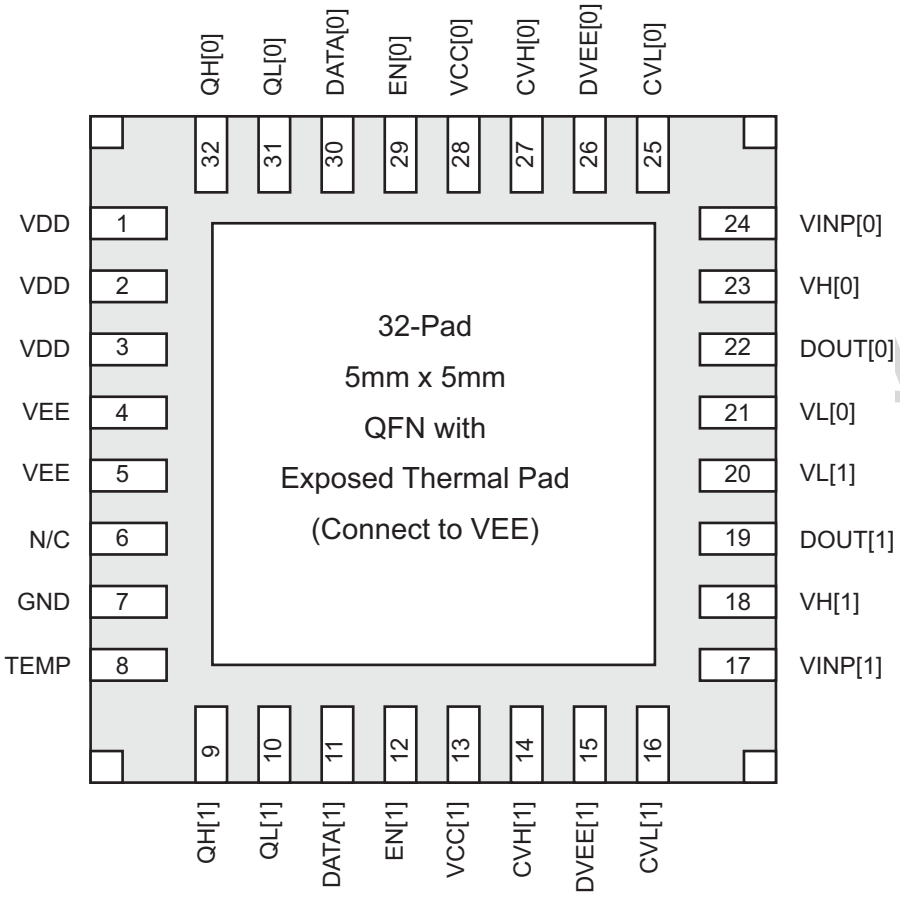
Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
30, 11	DATA[0:1]	Digital inputs which determine the high/low output state of the driver when it is enabled.
29, 12	EN[0:1]	Digital input which enables/disables the driver.
32, 9	QH[0:1]	Comparator digital outputs.
31, 10	QL[0:1]	Comparator digital outputs.
22, 19	DOUT[0:1]	Driver outputs.
24, 17	VINP[0:1]	Comparator inputs.
23, 18	VH[0:1]	Unbuffered analog inputs that set the driver high voltage level.
21, 20	VL[0:1]	Unbuffered analog inputs that set the driver low voltage level.
27, 14	CVH[0:1]	Analog inputs that set the threshold for the high comparator.
25, 16	CVL[0:1]	Analog inputs that set the threshold for the low comparator.
1, 2, 3	VDD	Digital Supply
7	GND	Ground pad. Connect to 0V.
28, 13	VCC[0:1]	Positive power supply.
4, 5, Center Pad	VEE	Negative power supply.
26, 15	DVEE[0:1]	Driver negative supply.
6	N/C	No connection.
8	TEMP	Connected to anode of temperature sensing diodes.

Pin Configuration



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VCC	–0.5		DVEE + 16	V
Negative Analog Supply	VEE	–6.0		+0.5	V
Negative Driver Supply	DVEE	VEE		+0.5	V
Digital Power Supply	VDD	–0.5		+6.0	V
Digital Input Voltages	EN[0:1], DATA[0:1]	–0.5		VDD + 0.5	V
Driver Pins	VH[0:1], VL[0:1], DOUT[0:1]	DVEE – 0.5		VCC + 0.5	V
Comparator Pins	CVH[0:1], CVL[0:1], VINP[0:1]	VEE – 0.5		VCC + 0.5	V
Storage Temperature	TS	–65		+150	°C
Junction Temperature	Tj			+150	°C
IR Reflow Conditions	Tpkg			+260	°C

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VCC	DVEE + 9	DVEE + 14.5	DVEE + 15	V
Negative Analog Supply	VEE	–5.25	–5	–4.75	V
Negative Driver Supply	DVEE	–3.6		0	V
Digital Power Supply	VDD	3.0		3.6	V
Thermal Resistance - Junction to Case Junction to Top-Center of Case Junction to Bottom-Center of Heat Slug	θjc		 4 1		 °C/W °C/W
Thermal Resistance - Junction to Ambient Still Air	θja		26		°C/W
Junction Temperature	TJ	25		100	°C

DC Electrical Specifications

For all of the following DC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

DC Electrical Specifications - Driver

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

SPEC #	PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
11005	Driver "High Level" Range	VH	VL		VCC	V
11010	Driver "Low Level" Range 10.4V < VCC ≤ 15V 5.4V ≤ VCC ≤ 10.4V		 DVEE DVEE		 VCC – 8.4 2	 V V
11015	Driver Output Swing	DOUT	0.2		15	V
11020	Driver Output Impedance VCC = 11.5V, VEE – 5V, DVEE = –3V, Tj = 65°C ± 3°C Across Recommended Operating Conditions	Rout	 6 4.4	 8	 12 16	 Ω Ω
11025	Offset Voltage	|VH, VL – DOUT|		0.5	2.5	mV
11030	Driver Digital Input Logic Levels (DATA, EN) Logic Input "High" Level Logic Input "Low" Level	 VIH VIL	 2.0 	 	 0.8	 V V
11035	Driver Digital Input Current Data, EN	 IIH, IIL	 –200	 	 +200	 nA
11040	Hi-Z Leakage Current at DOUT (DVEE ≤ DOUT ≤ VCC)	ILEAK	–135		+75	nA
11045	DC Output Current (Note 1)	IOUT (DC)	–125		+125	mA
11050	AC Output Current (Note 2)	IOUT (AC)	–1.5		+1.5	A

NOTES:

1. DC output current is specified per individual driver, $V_{VL} \le V_{DOUT} \le V_{VH}$.
2. Surge current capability with 1000pF lumped capacitive load on DOUT defined as the maximum output current during a 15V step.

DC Electrical Specifications - Comparator

Test conditions (unless otherwise specified): "Recommended Operating Conditions".

SPEC #	PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Inputs						
11105	CVH Input Voltage Range (Note 3)	VCVH	VCVL		VCC – 3	V
11110	CVL Input Voltage Range (Note 3)	VCVL	VEE + 3		VCVH	V
11115	CVH, CVL Input Current	I_{IN}	–15		+15	µA
11120	VINP Voltage Range	V_{VINP}	VEE + 2		VCC	V
11125	VINP Input Current DVEE ≤ VINP ≤ VCC – 3V Across Full VINP Range		 –30 –200		 +30 +200	 µA µA
11130	Hysteresis	VHY		30		mV
11135	Offset Voltage	VOS	–50		+50	mV
Digital Outputs						
11140	Output "High" Voltage @ +5mA	VOH	2.4			V
11145	Output 'Low" Voltage @ –5mA	VOL			0.4	V

NOTES:

3. Comparator threshold inputs (CVH, CVL) can be overlapped (i.e. VCVH < VCVL), but comparator output logic will be inverted and functionality of the comparators is not guaranteed under this condition.

DC Electrical Specifications - Power Supply Current (Quiescent)

SPEC #	PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Analog Inputs						
11200	Positive Supply Current	ICC	11	24	40	mA
11205	Driver Negative Supply Current	IDEE	1.5	7	12	mA
11210	Negative Supply Current	IEE	11	16	26	mA
11215	Digital Supply Current	IDD	2	6	14	mA

AC Electrical Specifications

For all of the following AC Electrical Specifications, compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

AC Electrical Specifications - Driver

Driver AC specifications are with Tj = 65°C ± 3°C, VCC = 15V, VDD = 3.3V, DVEE = 0V, VEE = –5V, VL = 0V, VH = 3V, into 20 inches of 50Ω transmission line unless otherwise noted.

SPEC #	PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Propagation Delay						
11500	DATA to DOUT (Figure 2)	Tpd	13.6		15.6	ns
11505	EN to DOUT (Active to HiZ) (Figure 3)	Tz	8		24	ns
11510	EN to DOUT (HiZ to Active) (Figure 3)	Toe	8		14	ns
11515	Propagation Delay Matching	|Tpd+ – Tpd–|			1	ns
11520	Propagation Delay Tempco (ΔTj = 25°C to 100°C)	ΔTpd/ΔT			30	ps/°C
11525	Driver Propagation Delay Dispersion vs. Amplitude (VL = 0, 0.2 < VH < 3.0)	ΔTpd(swing)			1	ns
Rise/Fall Times (50Ω Termination, Figure 1a)						
11550	1V Programmed Swing (20% - 80%)	Tr/Tf		2.5	4.5	ns
11555	3V Programmed Swing (10% - 90%)	Tr/Tf		3	5	ns
11560	5V Programmed Swing (10% - 90%)	Tr/Tf		3.5	5.5	ns
Maximum Operating Frequency (50Ω Termination, Figure 1a, Figure 4)						
11600	1V Programmed Swing	Fmax	100			MHz
11605	3V Programmed Swing	Fmax	100			MHz
11610	5V Programmed Swing	Fmax	100			MHz
Maximum Operating Frequency (1KΩ Termination, Figure 1b, Figure 4)						
11650	1V Programmed Swing	Fmax	100			MHz
11655	3V Programmed Swing	Fmax	100			MHz
11660	5V Programmed Swing	Fmax	100			MHz
11665	15V Programmed Swing	Fmax	100			MHz
11685	DOUT Capacitance	CDOUT		15		pF
11690	Driver Overshoot/Preshoot/Undershoot (3V) (1KΩ Termination, Figures 1b, 9) (Note 1)	Vovershoot			100	mV
11695	Glitch (HiZ to Active, Active to HiZ, 1KΩ Termination, Figure 1b) (Note 2)				365	mV
Minimum Pulse Width (Figures 1a, 5)						
11700	1V Programmed Swing	Mpw			5	ns
11705	3V Programmed Swing	Mpw			5	ns
11710	5V Programmed Swing	Mpw			5	ns

NOTES:

1. Measured with 33pF at end of transmission line. See “Optimizing Driver Waveforms” Section for characteristics and different capacitive loads.
2. VCC = 11.5V, DVEE = –3V, VEE = –5V, VH = 3V, VL = 0V, VL = 0V, Tj = 65°C ± 3°C, Cload = 3pF.

AC Electrical Specifications - Comparator

Comparator AC specifications are with Tj = 65°C ± 3°C, CVH = 1.5, CVL = 1.5, VINP = 0 to 3V @ 10MHz, VCC = 15V, VDD = 3.3V, DVEE = 0V, VEE = –5V unless otherwise noted.

SPEC #	PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
11800	Comparator Propagation Delay (Figure 6, Note 5)	Tpd+/–	3.5	5	6.5	ns
11805	Propagation Delay Matching (Note 5)	|(Tpd+) – (Tpd–)|		0.5	1.5	ns
11810	Propagation Delay Tempco (ΔTj = 25°C to 100°C)	ΔTpd/ΔT		15	20	ps/°C
11815	Propagation Delay Dispersion vs. Overdrive (Figure 7, Note 6) 100mV to 1V Overdrive 1V to 2.5V Overdrive	ΔTpd/Δ(VINP – VCH(L))		 2.5 0.25	 3.5 0.5	 ns ns
11820	Propagation Delay Dispersion vs. Common Mode (Figure 8, Notes 3, 6)	ΔTpd(cm)			0.5	ns
11825	Comparator Bandwidth (Note 4)	Fmax	100			MHz
11830	Minimum Pulse Width	CMPW			5	ns
11835	VINP Capacitance	CVINP		3		pF

NOTES:

3. V_{VINP} = 5Vpp, 0.5 ≤ $V_{CVH/L}$ ≤ 1.5V.
4. Comparator bandwidth is the maximum frequency under which the comparator will switch with CVH/CVL = 1.5V, VINP = 0 to 3V.
5. V_{VINP} = 5Vpp, VCVH, L = 2.5V.
6. CVH, CVL and Calibrated Threshold Values (i.e., “Switching Point”).

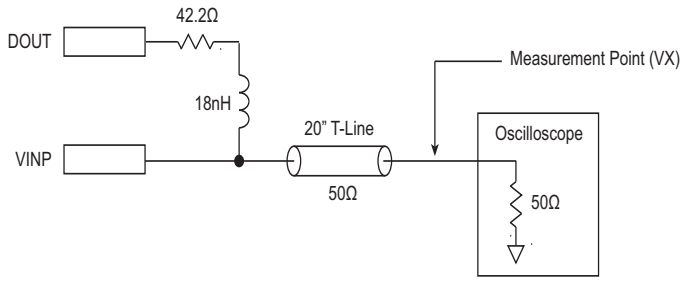


FIGURE 1a. Driver Output/Comparator Input, 50Ω Load

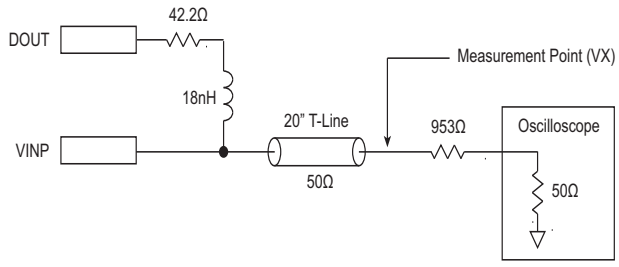


FIGURE 1b. Driver Output/Comparator Input, 1KΩ Load

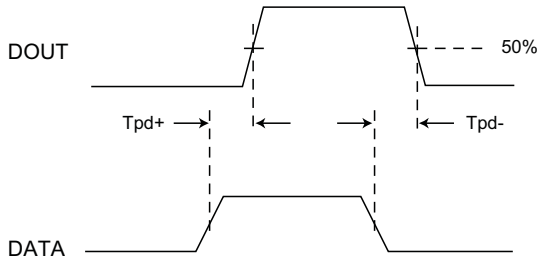


FIGURE 2. Driver Propagation Delay Measurements

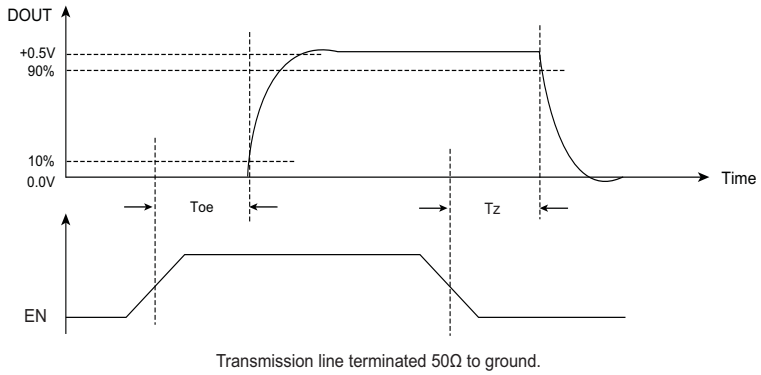


FIGURE 3. Driver HiZ Enable/Disable Delay Measurement Definition

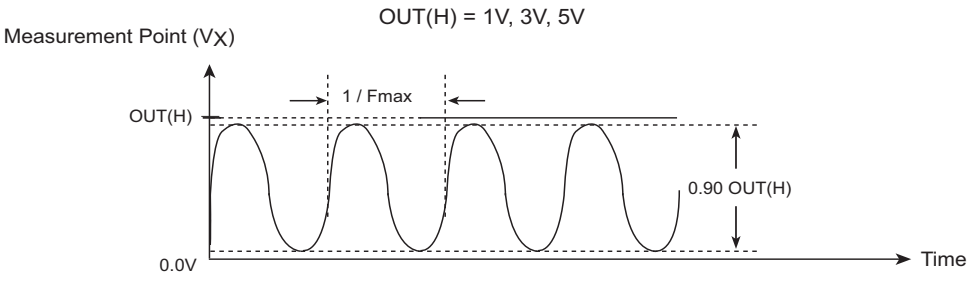


FIGURE 4. Driver Fmax Measurement Definition

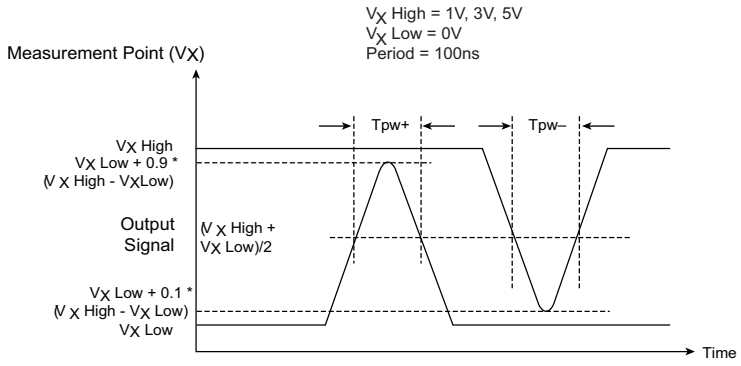


FIGURE 5. Driver Minimum Pulse Width Measurement Definition

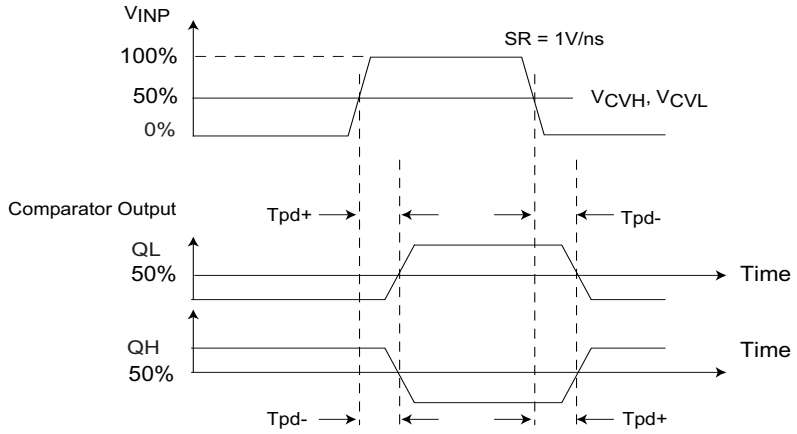


FIGURE 6. Comparator Propagation Delay Measurements

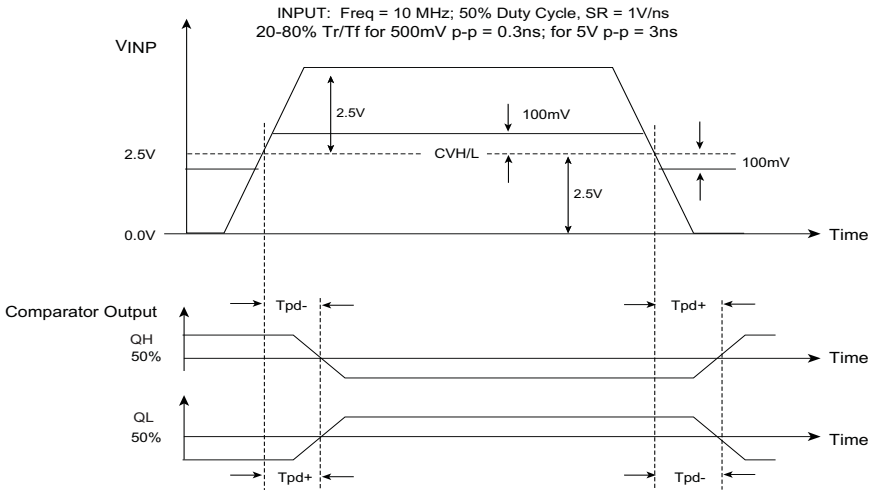


FIGURE 7. Comparator Dispersion: Overdrive Measurement Definition

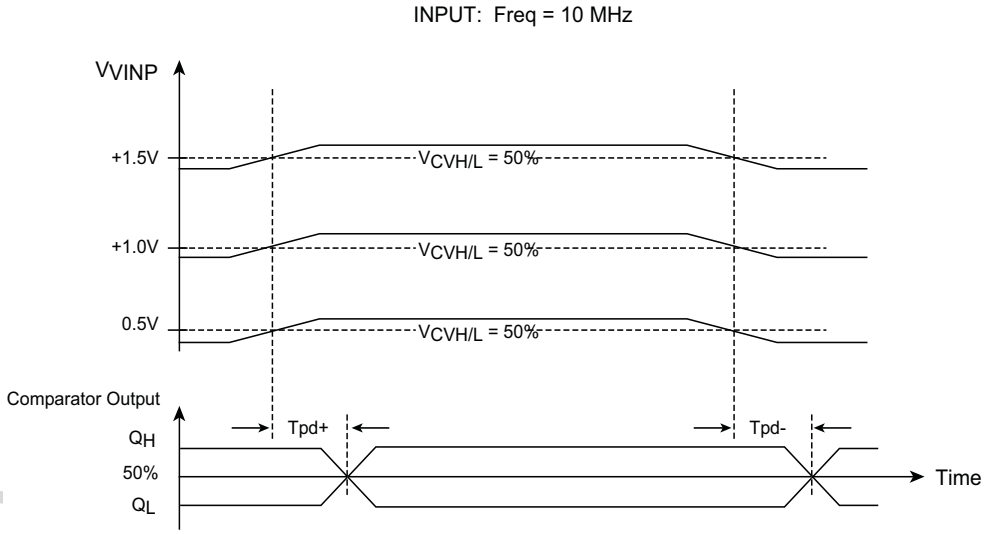


FIGURE 8. Comparator Dispersion: Common Mode Definition

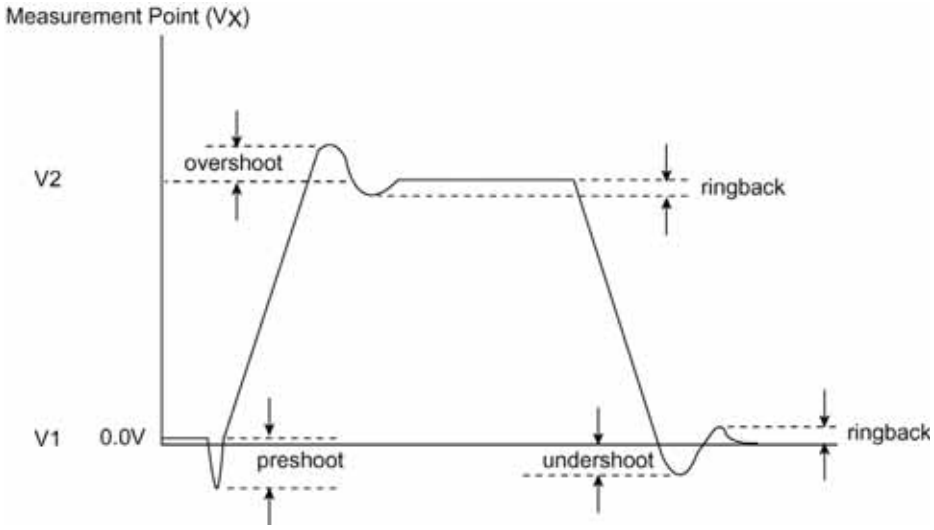


FIGURE 9. Driver Overshoot, Undershoot, and Ringback

Description

The Kilimanjaro supports independently programmable driver high and low levels as well as tristate per channel. There are no shared lines between the two drivers. The EN and DATA signals are inputs that are used to control the output of the driver as shown in Table 1. Each channel of the Kilimanjaro features a window comparator with separate high and low threshold levels (CVH, CVL), as well as independent digital outputs (QH, QL).

TABLE 1. Driver Functionality

EN	DATA	DOUT
0	0	HiZ
0	1	HiZ
1	0	VL
1	1	VH

NOTE: The voltage at DOUT needs to stay at DVEE ≤ DOUT ≤ VCC at all times (HiZ/Active).

Drive High and Low

VH and VL define the logical “1” and “0” levels of the driver, and can be adjusted to produce driver output swings from 200mV to up 15V.

The VH and VL inputs are unbuffered. They provide the driver output current (see Figure 10), so the source of VH and VL must have ample current drive capability.

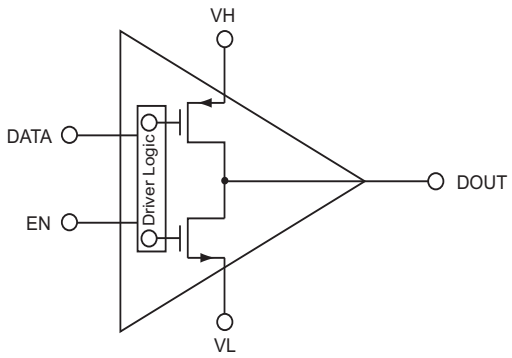


FIGURE 10. Driver High and Low

Window Comparator

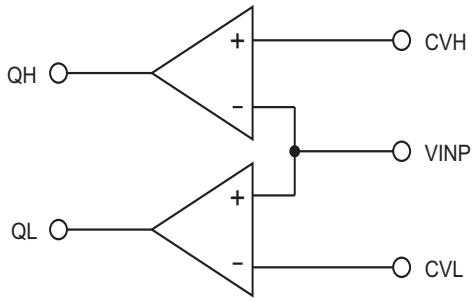


FIGURE 11. Window Comparator

Each channel of the Kilimanjaro features two comparators connected in a window comparator configuration. CVH and CVL are high impedance analog voltage inputs that establish the upper and lower thresholds for the window comparator. CVH should always be greater than or equal to CVL for normal comparator operation. QH and QL are digital outputs that indicate where a voltage measurement lies in relation to the CVH and CVL thresholds.

TABLE 2. Comparator Output Truth Table

Condition	QH	QL
Measurement is within the range established by CVH and CVL	1	1
Measurement is above the range established by CVH and CVL	0	1
Measurement is below the range established by CVH and CVL	1	0
Invalid State	0	0

The receiver thresholds can be used over a range of VEE + 3V to VCC – 3V. The VINP input of the receiver is designed to withstand voltages from VEE + 2V to VCC such that the comparator input can be directly connected to the driver output without being damaged.

NOTE: DVEE must be set appropriately in order to accommodate VINP input voltages of VEE + 2V when DOUT and VINP are connected in an application.

Thermal Diode String

The Kilimanjaro features an internal diode string connected between EN[1] and TEMP that can be used to perform device junction temperature measurements as shown in the figure below.

NOTE: EN[1] must be asserted “low” when making temperature measurements.

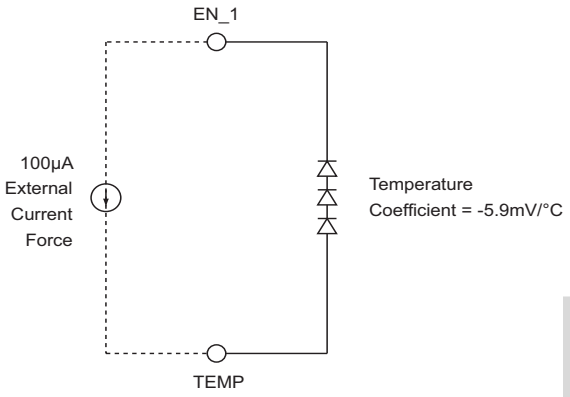


FIGURE 12. Thermal Diode String

Application Information

Power Supply Decoupling

VCC, VEE, and DVEE should be decoupled to GND with a .1µF chip capacitor in parallel with a .001µF chip capacitor for best AC performance. A VCC, VEE, and DVEE plane, or at least a solid power bus, is recommended for optimal performance.

VH and VL Inputs

As the VH and VL inputs are unbuffered to the driver and need to supply the output current, which can be quite large during edge transitions, bypass capacitors for these inputs are needed to supply the transient currents in proportion to the output current requirements.

For applications where VH and VL are shared over multiple channels, a solid power plane to distribute these levels with local bypassing is recommended for best AC performance.

Power Supply Sequencing/Latch-Up Protection

In order to avoid the possibility of latch-up when powering this device up (or down), be careful that the conditions listed in the Absolute Maximum Ratings are never violated. The power supplies should never be in reverse-polarity with respect to ground, and the input signals should never go beyond the power supply rails.

Furthermore, the lower-voltage supplies should never be greater than the higher-voltage supplies. This can easily be implemented by utilizing the diode circuit depicted in Figure 13 for each PCB utilizing the Kilimanjaro. The following conditions must be met at all times during power-up and power-down.

1. VEE ≤ DVEE ≤ VDD ≤ VCC
2. VEE ≤ Analog Inputs ≤ VCC
3. GND ≤Digital Inputs ≤ VDD

The following sequencing can be used as a guideline when powering up:

1. VEE
2. DVEE
3. VCC
4. VDD
5. Digital Inputs
6. Analog Inputs

As a general rule, ensure the VEE ≤ DVEE ≤ GND ≤ VDD ≤ VCC.

The four diode configuration shown in Figure 13 should be used on a once-per-board basis to help ensure that proper supply polarities are maintained.

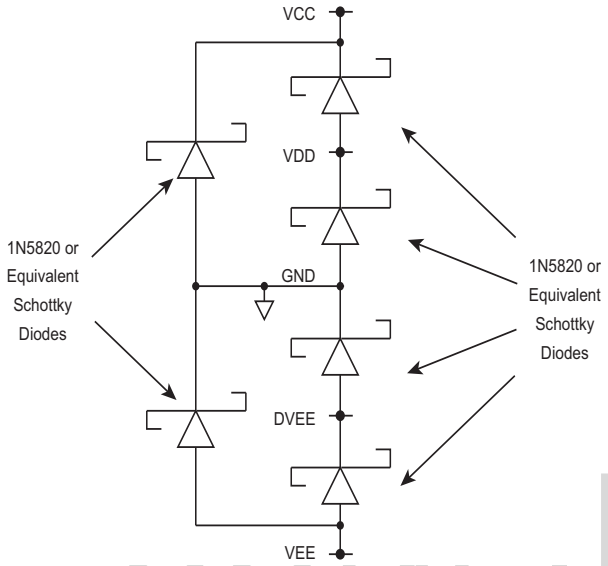


FIGURE 13. Power Supply Protection Scheme

Warning: It is extremely important that the voltage on any device pin does not exceed the range of VEE –0.5V or VCC +0.5V at any time, either during power-up, normal operation, or during power-down. Failure to adhere to this requirement could result in latch-up of the device which could be destructive if the system's power supplies are capable of supplying large amounts of current. Even if the device is not immediately destroyed, the cumulative damage caused by the stress of repeated latchup may affect device reliability.

Computing Maximum Power Consumption

The power consumption of the Kilimanjaro increases with increasing frequency and output voltage swing. The diagram below shows the power consumption of the Kilimanjaro at a couple of different voltage swings across the frequency range with both channels toggling.

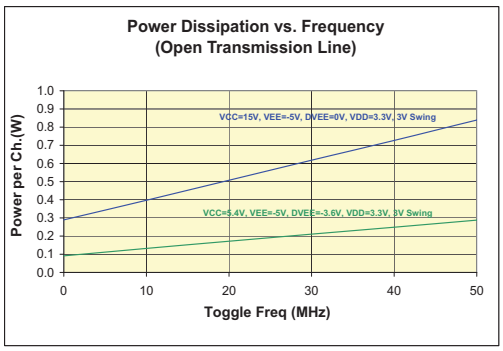


FIGURE 14. Computing Max Power Consumption

Cooling Considerations

Depending on the maximum operating frequencies and voltage swings the Kilimanjaro will need to drive, it may require the use of an external heatsink to keep the maximum die junction temperature within a safe range and below the specified maximum of 100°C.

The Kilimanjaro package has an external heat slug located on the bottom side of the package to efficiently conduct heat away from the die to the package surface. The thermal resistance of the package to the slug is the θjc (junction-to-case) and is specified at <1°C/W.

Additional cooling capability can be attained through the use of a heat sink on the top of the package. The plastic on the top of the Kilimanjaro's package is extremely thin and has an effective thermal impedance of <4°C/W.

In order to calculate what type of heatsinking should be applied to the Kilimanjaro, the designer needs to determine the worst case power dissipation of the device in the application. The graph above gives a good visual relationship of the power dissipation to the maximum operating frequency (all channels simultaneously) and driver output voltage swings. Another variable that needs to be determined is the maximum ambient air temperature that will be surrounding or blowing on the device and/or the heatsink system in the application (assuming an air cooled system).

A heatsinking solution should be chosen to be at or below a certain thermal impedance known as the Rθ in units of °C/W. The heatsinking system is a combination of factors including the actual heatsink chosen and the selection of the interface material between the Kilimanjaro package and the heatsink itself. This could be a thermal grease or thermal epoxy, each of which has its own thermal impedance.

The heatsinking solution will also depend on the volume of air passing over the heatsink and at what angle the air is impacting the heatsink. There are many options available in selecting a heatsinking system. The formula below shows how to calculate the required maximum thermal impedance for the entire heatsink system. Once this is known, the designer can evaluate the options that best fit the system design and meet the required Rθ.

Rθ (heatsink system) = (Tjmax – Tambient – P * θjc)/P where:

Rθ (heatsink_system) is the thermal resistance of the entire heatsink system.

Tjmax is the maximum die temperature (100°C).

Tambient is the maximum ambient air temperature expected at the heatsink (°C).

P is the maximum expected power dissipation of the Kilimanjaro (Watts).

θjc is the thermal impedance of the Kilimanjaro junction to case (<1°C/W through bottom, <4°C/W through top).

The value of the thermal resistance of the Kilimanjaro package junction to air with 400 linear feet per minute (LFPM) of airflow is specified at 28°C/W. At operating points greater than or equal to this value, no additional heatsinking is needed to keep the die temperature below the maximum 100°C as long as the ambient temperature of the 400 LFPM air does not exceed 70°C.

More information on heatsink system selections can be read on heatsink vendors' websites.

Driving a Resistive Load

In addition to the VCC and VEE power supply levels, the "driver high" (VH) and "driver low" (VL) levels used in an application also have an effect on the total power dissipation of the device illustrated using Figure 15.

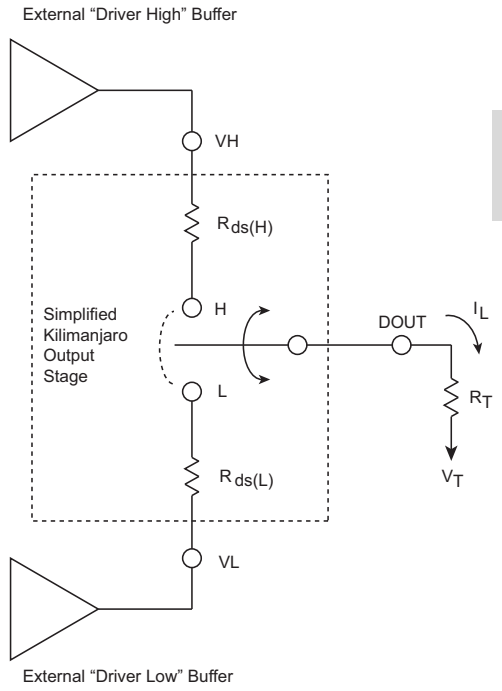


FIGURE 15. Simplified Functional Schematic of Kilimanjaro Output Stage and External Buffers

The CMOS switches of the Kilimanjaro's output stage have on-resistance values (depicted by $R_{ds(H)}$ and $R_{ds(L)}$ in Figure 15) that vary as a function of VH and VL voltage levels. The amount of current required by the load impedance, RT, is also a function of the VH and VL voltage levels as follows:

Switch in Figure 15 is in position "H":

$$I_{L(H)} = \frac{VH - V_T}{R_{ds(H)} + R_T}$$

Switch in Figure 15 is in position "L":

$$I_{L(L)} = \frac{VL - V_T}{R_{ds(L)} + R_T}$$

Therefore, the per-channel power dissipation due to the Kilimanjaro driving resistive load is:

$P = [I_L{}^2{}_{(H)} \times R_{ds(H)} \times D] + I_L{}^2{}_{(L)} \times R_{ds(L)} \times (1 - D)]$ where:

P is the total power dissipated by Kilimanjaro as a result of the resistive load, R_L[Ω].

$I_{L(H)}$ is the amount of current required by R_L during a logic "high" state [A].

$R_{ds(H)}$ is the output impedance of the Kilimanjaro driver when driving a logic "high" state [Ω].

D is the normalized amount of time that logic "high" is driven (Duty Cycle).

$I_{L(L)}$ is the amount of current required by RL during a logic "low" state [A].

$R_{ds(L)}$ is the output impedance of the Kilimanjaro driver when driving a logic "low" state [Ω].

Driving Currents Larger than 125mA

The driver channels of the Kilimanjaro can be connected in parallel to drive currents larger than the rated 125mA per individual driver.

Optimizing Driver Waveforms

OVERSHOOT/UNDERSHOOT/PRESHOOT

Kilimanjaro driver overshoot, undershoot and preshoot are functions of the DOUT edge rate. Slower DOUT edge rates are associated with smaller overshoot, undershoot and preshoot amplitudes. The DOUT edge rate is influenced by the amount of capacitance that is present on the driver output with larger capacitance resulting in slower edge rates and less overshoot as shown in Figure 16 below.

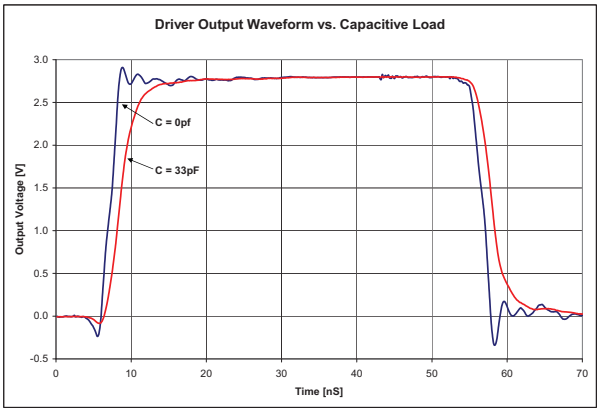


FIGURE 16. Driver Waveform vs. Capacitive Load

Overshoot, undershoot and preshoot are also influenced by power supply levels. In general, lower VCC levels are associated with less overshoot and better small-swing performance.

OUTPUT IMPEDANCE MATCHING

1. *Real Component:* Accounts for the resistive (DC) portion of the driver output impedance and is matched to a transmission line by using an external "backmatch" resistor. Using empirical methods in our lab, we have determined that a 42.2 backmatch resistor offers the best real impedance matching for a 50Ω transmission line.
2. *Reactive Component:* Accounts for the reactive or "AC" component of the output impedance and is matched to a transmission line by using external inductors and/or capacitors. Using empirical methods in our lab, we have determined that an 18nH series inductor offers the best impedance matching for a 50Ω transmission line (see Figure 17).

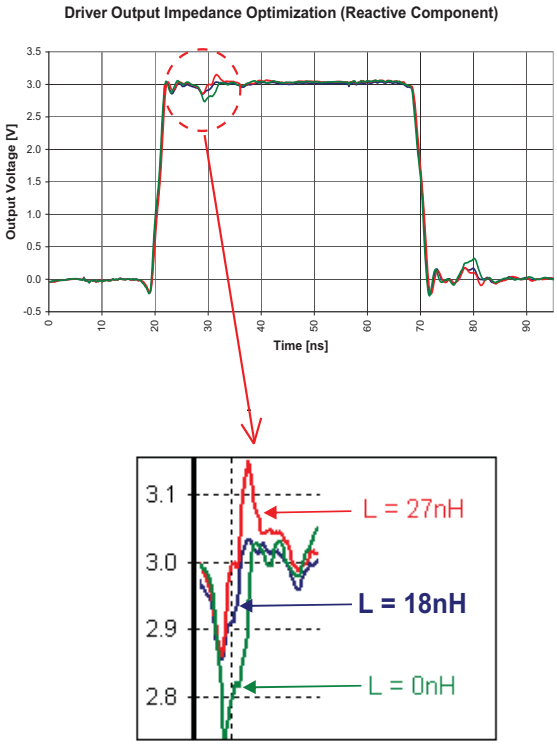
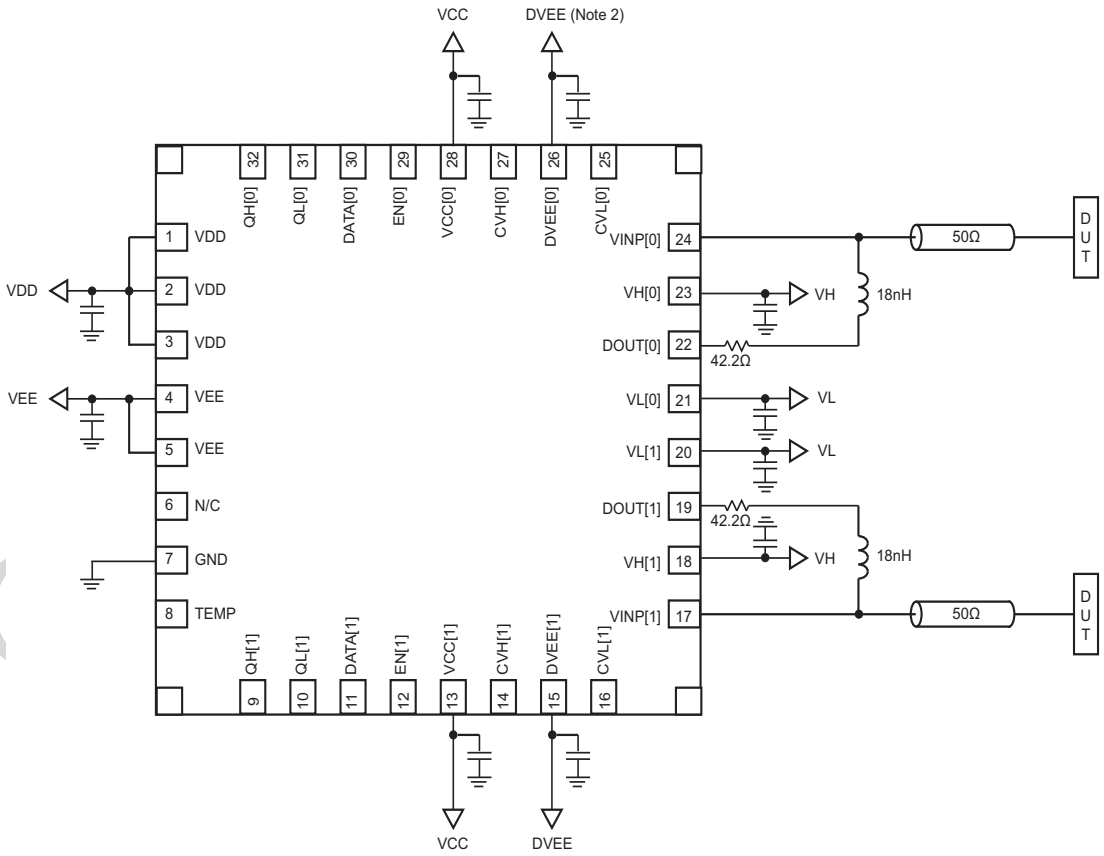


FIGURE 17. Driver Output Impedance Optimization

External component connections are illustrated in the Kilimanjaro Hookup Diagram (Figure 18).



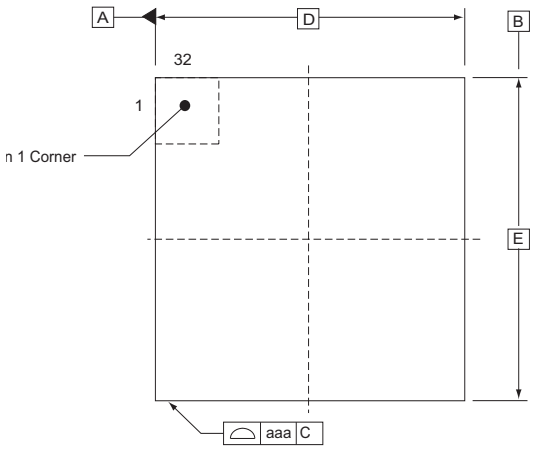
Note 1: All capacitors are 0.1µF unless otherwise noted.

Note 2: DVEE supply can be connected to GND if DOUT does not need to swing below 0V.

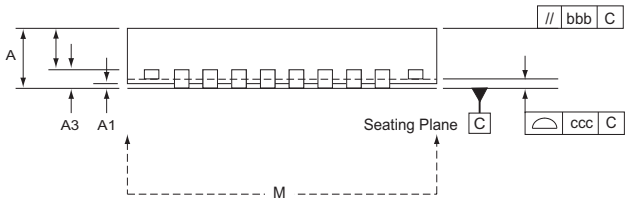
FIGURE 18. Hookup Diagram

Package Information

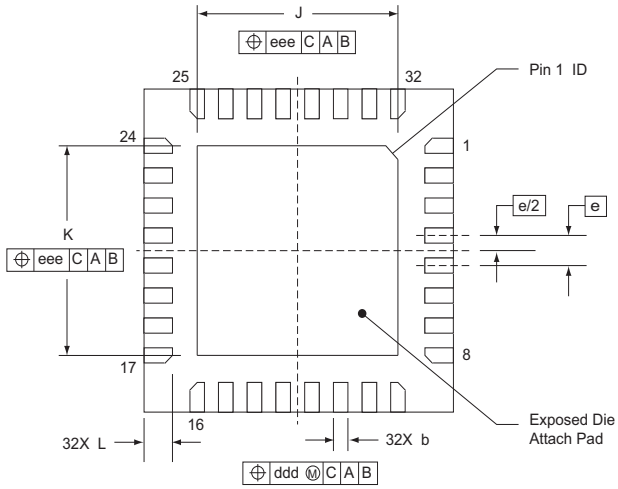
32 Pad
5mm x 5mm QFN



TOP VIEW



SIDE VIEW



BOTTOM VIEW

		SYM	MIN	NOM	MAX
Total Thickness		A	0.85	0.9	0.95
Stand off		A1	0	0.035	0.05
Mold Thickness		A2	-	0.7	-
L/F Thickness		A3	0.203 REF		
Lead Width		b	0.2	0.25	0.3
Body Size	X	D	5 BSC		
	Y	E	5 BSC		
Lead Pitch		e	0.5 BSC		
EP Size	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
Lead Length		L	0.35	0.4	0.45
Package Edge Tolerence		aaa	0.1		
Mold Flatness		bbb	0.1		
Coplanarity		ccc	0.08		
Lead Offset		ddd	0.1		
Exposed Pad Offset		eee	0.1		

NOTE:

1.0 Coplanarity applies to leads, corner leads and die attach pad.

Revision History

Date	Page	Description of Change
February 6, 2018	2	List of Figures: change 50C Load to 50Ω Load
	4	Change MLP to QFN
	5	Ab Max Ratings, Driver Pins: change min from DVEE + 0.5 to DVEE– 0.5
	6	Comparator Specifications: Change Digital Inputs to Digital Outputs
	22	Update ordering information
August 18, 2016	Various	Notes and figures renumbered
	2	Change Driving Currents Larger than 200mA to 125mA. Add List of Figures
	5	Digital Input Voltages - delete SCP* from Symbol column
	6	Driver Table, Spec 11030 - delete SCP# Driver Table, Spec 11040 - change units from mA to nA
	10	Figure 4 - Change OUT(H) = 0.4V, 1V, 3V, 5V to OUT(H) = 1V, 3V, 5V
	11	Figure 5 - Change VX High = 0.4V, 1V, 3V, 5V to VX High = 1V, 3V, 5V
	13	Window Comparator - 1st para - delete everything after ... CVH and CVL thresholds Table 2 - Delete INT* column; change last row to read Invalid State
	16	Change Driving Currents Larger than 200mA to 125mA
March 10, 2016	1	Remove “Target”. Datasheet now final.
	8	3V Programmed Swing (10% - 90%) - add units “ns”
February 9, 2016	10	Figures 1a and 1b: Change 38 Ω to 42.2 Ω
	17	Figure 15 - update figure
	19	Output Impedance Matching - change 45.3 Ω to 42.2 Ω
January 8, 2016	17	Power Supply Sequencing Section: Change order of power supply sequence.

November 12, 2015	1	Features: Remove “Low Output Impedance” and “Driver Short Circuit Protection
	3	Change “INT” to N/C Remove SCP* and made Pin 1 VDD
	4	Change Pin 1 from SCP* to VDD, Change Pin 6 from INT* to N/C
	5	IR Reflow Conditions: Change from Max +250 to Max +260
	6	Driver Output Impedance: Change from Min 4.5 to 4.4 Offset Voltage: delete Min 0.5, add 0.5 Typ Remove SCP*, Short Circuit Protection Threshold, and INT* Output Low Voltage
	8	Change EN to DOUT (Active to HiZ) from Max 17 to 24 Remove Short Circuit Protection Activation Time, Rise/Fall Times (1000pF) and (100pF)
	9	Rise/Fall Times (50 Ω): Remove 0.4V Programmed Swing Change 1V Programmed Swing from Typ/Max 3/5 to 2.5/4.5 Change 3V Programmed Swing from Typ/Max 3.5/5.5 to 3/5 Change 5V Programmed Swing from Typ/Max 4/6.5 to 3.5/5.5 Remove all 0.4V Programmed Swing Change DOUT Capacitance from Typ 50 to 15 Add Glitch (HiZ to Active, Active to HiZ) Minimum Pulse Width: 1V Programmed Swing - change from Max 7.5 to 5 3V Programmed Swing - change from Max 8 to 5 5V Programmed Swing - change from Max 9 to 5 Add Note 4
	10	Remove Figure 1a, renumber remaining figures
	14	Remove Driver Output Protection section
	20	Update Figure 20
October 15, 2015	17	Update Power Up Sequence Add diode to Figure 15
	21	Update Package Outline Drawing
	22	Change Part # from ELE22KI1A-RBP01 to ELE22KI1A-RBJ01
March 20, 2014	20	Hookup diagram updated.

Ordering Information

PART NUMBER	PACKAGE (Pb-free)
ELE22KI2A-RBJ01	32 Pad, 5mm x 5mm QFN, shipped in JEDEC trays
ELE22KI2A-RBJ01-R	32 Pad, 5mm x 5mm QFN, shipped on Tape and Reel
ELE22KI2A-EVM	Kilimanjaro Evaluation Board

NOTES:

1. These Elevate Semiconductor Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Elevate Semiconductor Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020..