Elevate Semiconductor EVM User's Guide

Rev B00 : 1/05/2007

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1 Introduction

Congratulations on your purchase of a Elevate Semiconductor evaluation system. You will find that it serves as an invaluable development platform to help get your product to market in the shortest possible time. The Elevate Semiconductor EVM and Graphical User Interface (GUI) allow the customer to demonstrate and evaluate the device's performance and functionality.

1.1 Supported Products & Revisions

The Elevate Semiconductor EVM supports the following products and revisions.

Table 1: Supported Products and Revision

Product	Revision	# Chans	Feature Highlights
Venus	3+	2	133MHz per channel 3-Level Driver, Comparator, Coarse/Fine Deskews, PMU
VenusPlus	1+	2	166 MHz per channel 3-Level Driver, Comparator, Coarse/Fine Deskews, PMU
Venus2	1+	2	400 MHz per channel 3-Level Driver, Comparator, Coarse/Fine Deskews, PMU
Mercury	2+	8/16	50MHz per channel 2-Level Driver, Comparator, Coarse Deskews Independent Driver/Comparator per channel. Central PMU
Pluto	4+	8	Per channel PMU w/ DC Pin (Driver) capabilities
Neptune	4+	2	Per channel PMU and External DACs
Jupiter	6+	1	512mA Gangable DPS
Saturn	4+	2	Per channel Wide Voltage Pin Driver, Load, Comparator, Coarse Deskews, PMU
Triton	1+	8	Per channel Wide Voltage PMU and Active Load (LCD Driver Test Solutions)

A # following the board revision letter implies only a certain build code is supported. No # implies all build codes are supported

Table 2: Supported Hardware Revisions

Hardware	Revision
Venus Loadboard	B to F
Mercury Loadboard	A / B
Pluto Loadboard	C / D
Neptune Loadboard	A
Jupiter Loadboard	B / C
Saturn Loadboard	B
Triton Loadboard	A / B
Europa Loadboard	A
Motherboard	A4 / B4 / C / D
Octal FVMI	E4 / F / G / G2
USB Parallel Interface	A

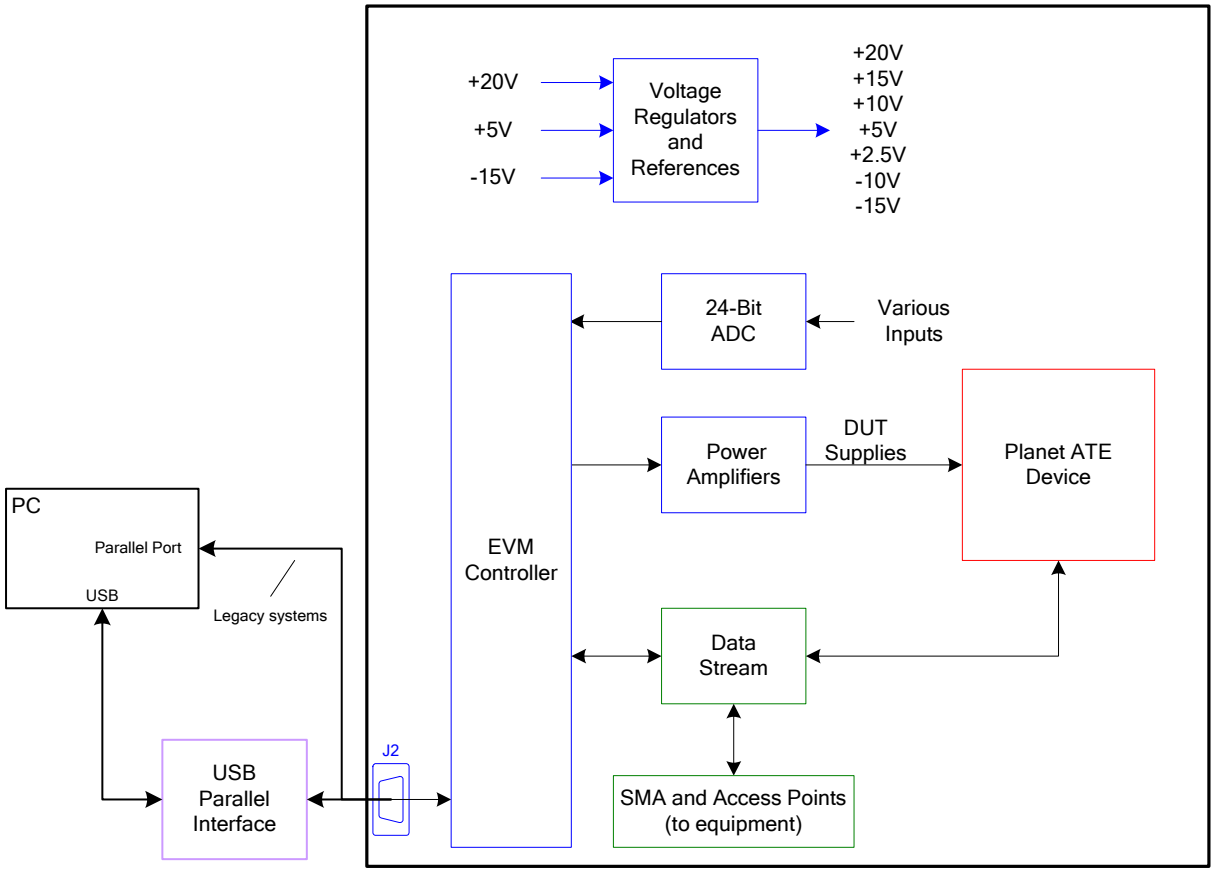
2 Elevate Semiconductor EVM Overview

Figure 1 illustrates the Elevate Semiconductor EVM overview diagram. The Elevate Semiconductor EVM is comprised of 3 boards:

- Device Loadboard – this is the top board and contains the Elevate Semiconductor device. Represented in red in the figure. Refer to the corresponding ***Getting Started*** document for the loadboard details.
- Motherboard – this is the middle board and contains the data stream and comparator output test access points. Represented in green in the figure.
- Octal FVMI Board – this is the bottom board and contains the power amplifiers, A/D converter, voltage regulators/references, and EVM controller. Represented in blue in the figure.
- USB to Parallel Interface Board – this provides a USB to Parallel translator. Represented in lavender in the figure.

To support legacy systems, the software and hardware still support connecting a parallel port cable directly from the PC to the FVMI board.

Figure 1: Elevate Semiconductor EVM Overview Block Diagram



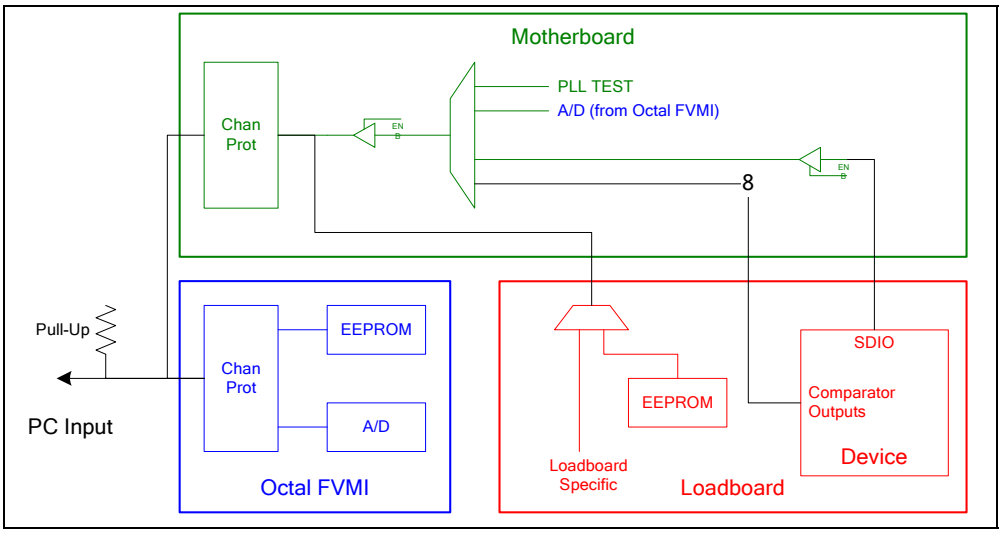
3 V100 FVMI and Motherboard Detailed Description

This section describes the Octal FVMI (DPS, bottom) board and Motherboard (middle). These 2 boards will work with any loadboard.

3.1 PC Readback Overview

Figure 1 illustrates the readback capabilities of the EVM system. Channel Protectors are used to isolate the PC from the EVM. A series of muxes, three-state buffers, and tri-stateable devices are used to support a single reackback node. The PC can readback the Device Registers, EEPROMs, Comparator Output State, A/D State (High or Low), and more.

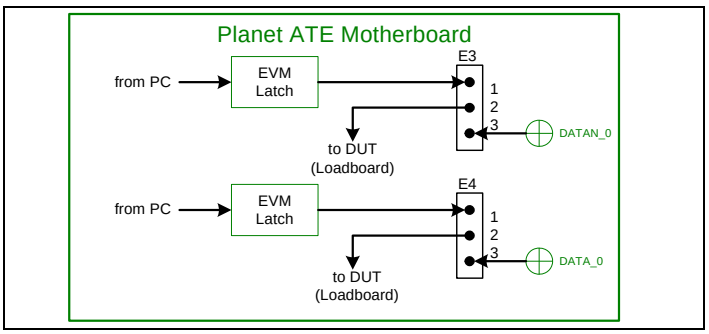
Figure 2: PC Readback Overview



3.2 Motherboard Latch and Jumper Overview

- PC via EVM controller – requires no additional equipment to drive data patterns but can not run at full speed. To select this option, set the jumper across pins 1 & 2 (towards top of board). The software defaults are digital inputs (EVM latches) to a low state (DATA = 0.0V and DATAN = 3.3V). This option should be selected whenever a digital differential input isn't used. If left floating, the inputs could oscillate and cause an undesirable output.
- Test Equipment via SMA connectors – Can source from either a pulse generator to provide full speed data stream. To select this option, set the jumper across pins 2 & 3 (towards front of board).

Figure 3: MB Digital Input Overview



3.3 TC# Connector Definition

Table 3 lists the TC# resource allocation. Most of the TC_# signals can be connected to an SMA on the EVM Motherboard.

Table 3: TC# Resource Allocation

TC#	Venus	Mercury	Pluto	Neptune	Jupiter	Triton	Saturn	Europa
1	TPIN	TPIN	TPIN	TPIN	TPIN	TPIN	TPIN	TPIN
2	CPU_SDIO	CPU_SDIO	CPU_SDIO	CPU_SDIO	CPU_SDIO	CPU_SDIO	CPU_SDIO	CPU_SDIO
3	CPU_STB	CPU_STB	CPU_STB	CPU_STB	CPU_STB	CPU_STB	CPU_STB	CPU_STB
4	RESET	RESET	RESET	RESET	RESET	RESET	RESET	RESET
5	COMPA0	COMPB0/4	COMPA0/4	COMPA0	DPS_EN*	MONITOR	COMPA0	GANG1_OUT
6	COMPAN0	COMPA0/4	COMPB0/4	Reserved	CAP_DIS*	MON_REF	COMPAN0	GANG3_OUT
7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
8	COMPB0	COMPB1/5	COMPA1/5	COMPB0	C_BIT	MON#	COMPB0	GANG5_OUT
9	COMPBN0	COMPA1/5	COMPB1/5	Reserved	ALARM*	MON_REF#	COMPBN0	GANG7_OUT
10	CPU_CK	CPU_CK	CPU_CK	CPU_CK	CPU_CK	CPU_CK	CPU_CK	CPU_CK
11	COMPA1	COMPB2/6	COMPA2/6	COMPA1	OT_ALARM*	EXT_FORCE#	COMPA1	EXT_FORCE
12	COMPAN1	COMPA2/6	COMPB2/6	Reserved	I_ALARM*	EXT_SENSE#	COMPAN1	EXT_SENSE
13	COMPB1	COMPB3/7	COMPA3/7	COMPB1	V_ALARM*	TJ	COMPB1	TJ
14	COMPBN1	COMPA3/7	COMPB3/7	Reserved	KEL_ALARM*	LB_AMUX	COMPBN1	
15	DUT_GND0	Various	Reserved	Reserved	Reserved	DUT_GND	Reserved	DUT_GND
16	DUT_GND1	PLL_ILOAD	Reserved	Reserved	Reserved	TEST_IN	Reserved	GANG#_IN
17	DATA0	DATA0/4	DATA0/4	EN_C0_F_MUX	EN	DATA0/4	DATA0	DATA0
18	DATAN0	DATA1/5	DATA1/5	COMP_IN	EXT_ADDER_CK	DATA1/5	DATAN0	DATA1
19	EN0	EN0/4	EN0/4	EN0	EXT_UD*	EN0/4	EN0	DATA2
20	ENN0	EN1/5	EN1/5	EN_C1_S_MUX	EXT_LD	EN1/5	ENN0	DATA3
21	SV0	DIG_BANK_SEL	DIG_BANK_SEL	Reserved	EXT_TJ_EN	SDI_RCK	SDI_RCK	SDI_RCK
22	DATA1	DATA2/6	DATA2/6	Reserved	Reserved	DATA2/6	DATA1	DATA4
23	DATAN1	DATA3/7	DATA3/7	EN_C1_F_MUX	EXT_MON_OE	DATA3/7	DATAN1	DATA5
24	EN1	EN2/6	EN2/6	EN1	Slave STB	EN2/6	EN1	DATA6
25	ENN1	EN3/7	EN3/7	EN_C0_S_MUX	Slave RESET	EN3/7	ENN1	DATA7
26	SV1	SDI_RCK	SDI_RCK	SDI_RCK	SDI_RCK	EXT_MON_SEL0	DOUT1	EN
27	EXT_SENSE	SDI_SCK	SDI_SCK	SDI_SCK	SDI_SCK	EXT_MON_SEL1	DOUT0	EXT_MON_OE
28	EXT_FORCE	SDI_DATA	SDI_DATA	SDI_DATA	SDI_DATA	EXT_MON_SEL2	LB_AMUX	
29	PLL_CKB	PLL_CKB	Reserved	Reserved	Reserved	Reserved	PLL_CKB	Reserved
30	PLL_CK	PLL_CK	Reserved	Reserved	Reserved	Reserved	PLL_CK	Reserved
31	DOUT1	DOUT_EVEN	Reserved	Reserved	Reserved	Reserved	DIN1	LB_AMUX
32	DOUT0	DOUT_ODD	EXT_FS	Reserved	Reserved	TEST_NODE	DIN0	TEST_NODE

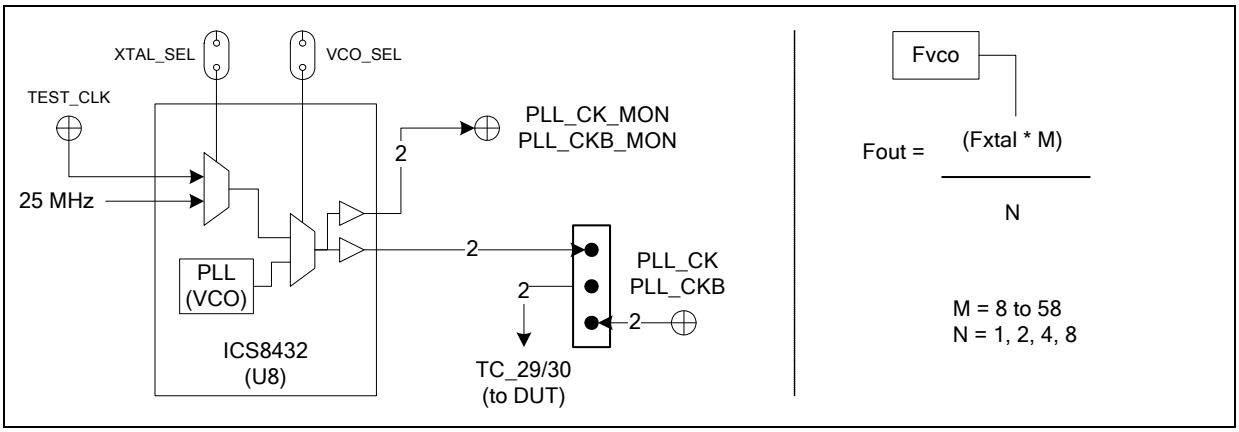
3.4 Motherboard PLL_CK Generator

Figure 4 illustrates the Motherboard PLL_CK generator and PLL formula. The PLL uses shifted LVPECL levels. The PLL has dual differential outputs where both outputs are identical. The PLL can operate from 25.0 MHz to 700.0 MHz. The GUI limits the upper end to 175.0 MHz when the ***Perform Range Check*** flag is set.

The PLL_CK_MON / PLL_CKB_MON SMAs are connected to the second output. These can be used as a DATA/EN input to the device by connecting a SMA cable from these SMAs to the appropriate DATA/EN SMA.

The Fvco must be between 200 and 700 MHz. This implies a different allowable **M** value depending on the Fxtal. The Fout range and resolution is dependant on the **N** divider, see Table 5. For applications that use an external TEST_CLK, the user must enter in the TEST_CLK (CLK_REF) into the GUI. The software calculates the optimal **M** and **N** values based on the desired PLL_CK and CLK_REF. The TEST_CLK input frequency range is from 12.0 to 25.0 MHz.

Figure 4: Motherboard PLL_CK Generator Overview



For products that don't require a PLL_CK (i.e. Pluto, Neptune, Jupiter, etc), shorting the VCO_SEL and XTAL_SEL jumpers may reduce board noise.

Table 4: Motherboard PLL_CK Jumper Options

Jumper	Name	Description
E16	VCO_SEL	Open – Use VCO Output (default) Short – Bypass VCO Output (use CLK_REF)
E17	XTAL_SEL	CLK_REF Open – Use 25 MHz XTAL (default) Short – Use TEST_CLK SMA

Table 5: Motherboard PLL_CK Specifications

XTAL Input (MHz)	N	Fout Range (MHz)	Resolution (MHz)
25	1	200 to 700	25
25	2	100 to 350	12.5
25	4	50 to 175	6.25
25	8	25 to 87.5	3.125

3.5 Octal FVMI EVM Detailed Description

Figure 5 illustrates the Octal FVMI EVM detailed block diagram. Figure 6 illustrates a detailed block diagram of the EVM Controller section.

Note: The turquoise nodes are new to Octal FVMI Rev F.

Figure 5: Octal FVMI EVM Overview Block Diagram

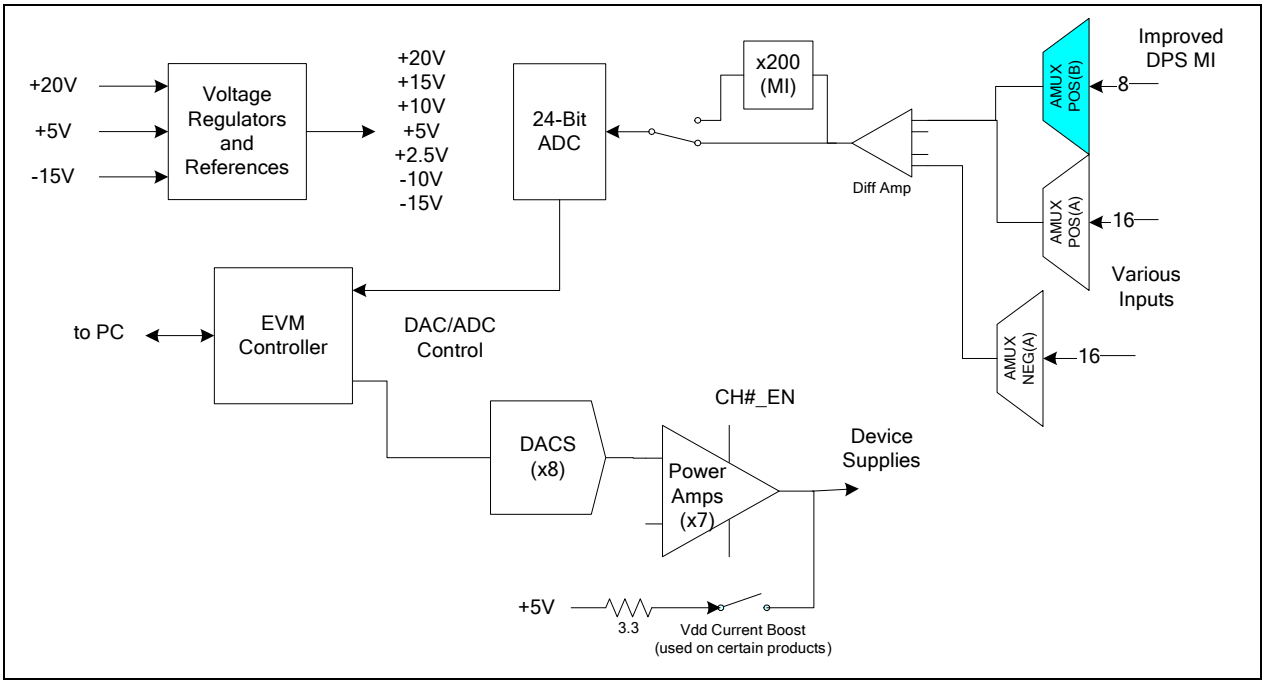
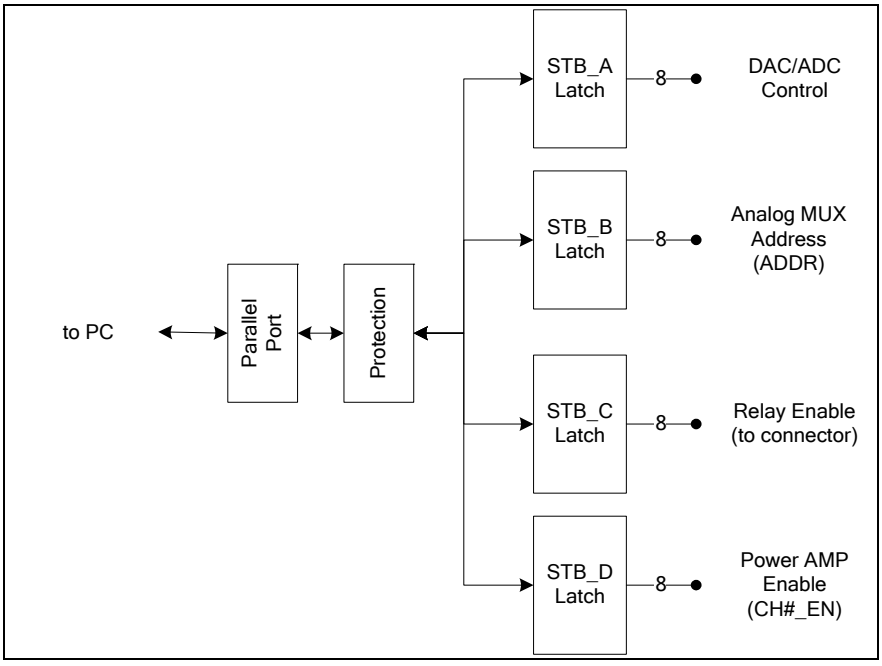


Figure 6: Octal FVMI EVM Controller Block Diagram



3.5.1 FVMI ADC and Analog Mux

The FVMI contains a 24-bit ADC and a couple of 16-channel analog muxes. **Error! Reference source not found.** list the Octal FVMI analog mux input sources. The signals travel between the different boards and might have more than one net name.

Color Coding:

1) The black signals originate from the Octal FVMI board.
2) The turquoise signals are new or modified to Octal FVMI Rev F.
3) The green originate from the loadboard. Refer to the product specific ***EVM Getting Started*** document

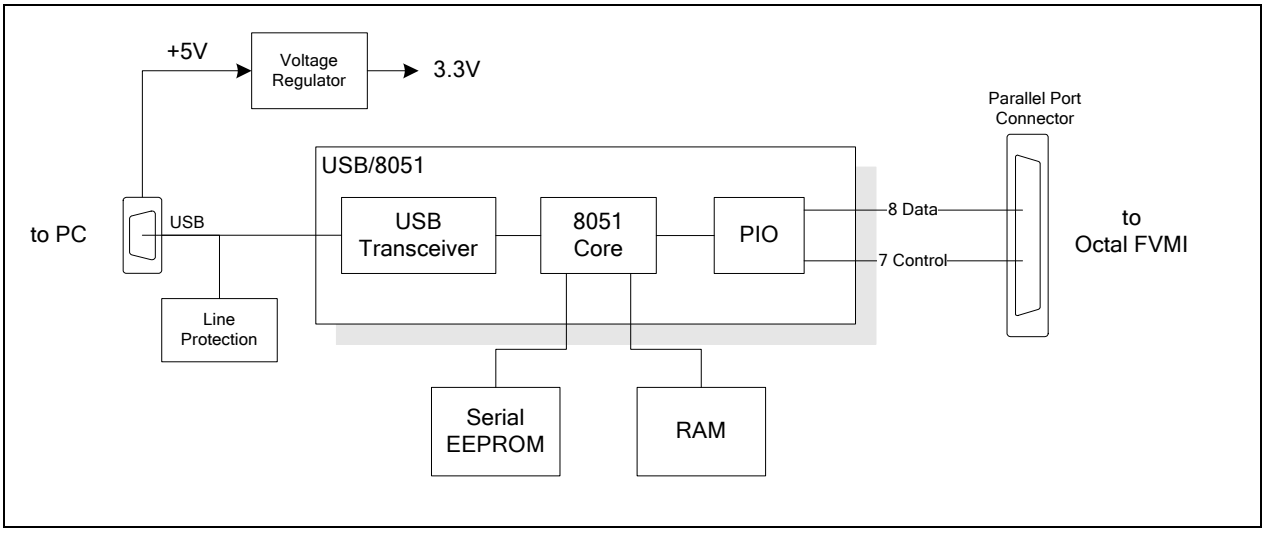
Table 6: FVMI Analog Mux – VINPOS(A) Mapping

Addr	VINP#	VINPOS(A)	VINPOS(B)	VINN#	VINNEG(A)
0x00		VSV Voltage Sense	VSV Force Sense		VSV Current Sense
0x01		VCC Voltage Sense	VCC Force Sense		VCC Current Sense
0x02		VDD Voltage Sense	VDD Force Sense		VDD Current Sense
0x03		VEE Voltage Sense	VEE Force Sense		VEE Current Sense
0x04		VOH Voltage Sense	VOH Force Sense		VOH Current Sense
0x05		VOL Voltage Sense	VOL Force Sense		VOL Current Sense
0x06		VREF Voltage Sense	VREF Force Sense		VREF Current Sense
0x07	VINP8	VCC Force / Reserved	No connect	VINN8	Loadboard Specific
0x08	VINP9	Loadboard Specific	No connect	VINN9	Loadboard Specific
0x09	VINP10	Loadboard Specific	No connect	VINN10	Loadboard Specific
0x0A	VINP11	Loadboard Specific	No connect	VINN11	Loadboard Specific
0x0B	VINP12	Loadboard Specific	No connect	VINN12	Loadboard Specific
0x0C	VINP13	Loadboard Specific	No connect	VINN13	Loadboard Specific
0x0D	VINP14	Loadboard Specific	No connect	VINN14	Loadboard Specific
0x0E		Ch #8 Output Voltage	No connect		Ch #8 Output Voltage
0x0F		DUTREF – Ground	No connect		DUTREF – Ground

3.6 USB to Parallel Interface Board Detailed Description

Figure 7 illustrates the USB to Parallel Interface board detailed block diagram. This board provides a USB to Parallel translator to support newer computers that no longer provide the Parallel Port. Refer to the ***USB_Parallel_Spec.doc*** for complete details

Figure 7: USB Parallel Interface Overview Block Diagram



4 Elevate Semiconductor EVM Port Interface Description

Table 7 lists the parallel port control signal to Octal FVMI mapping. The I/O column is relative to the PC parallel port; for example: PAPER_OUT is an input signal to the PC from the EVM.

Table 7: Port Driver Signal Mapping

FVMI Signal	I/O	Description	Parallel Port Name	USB/8051 Port
DATA[7:0]	Input/Output	Data Bus	DATA[7:0]	PortD[7:0]
Latch Addr En	Output	STB Decode Enable	~STROBE	PortA[0]
Latch Addr2	Output	STB Decode C	AUTO_FEED	PortA[6]
Latch Addr1	Output	STB Decode B	~INIT	PortA[5]
Latch Addr0	Output	STB Decode A	SELECT_IN	PortA[4]
ADCDATA	Input	FVMI ADC Data Output	~ACKNLG	PortE[0]
SDO_B	Input	FVMI DAC Serial Data Out	PAPER_OUT	PortE[1]
DATA_OUT	Input	FVMI EEPROM DO & V100 MB Data Out (1) & Loadboard EEPROM D0	~ERROR	PortE[2]
N/C			SELECT_OUT	
N/C			BUSY	

Notes:
1) The Venus MB Data Out is sourced from the Motherboard analog mux. This provides the ability to measure/monitor the state of any of the comparators and the device SDIO output.

4.1 EVM Latches

The Octal FV MI board contains four (4) 8-bit latches (registers). The STB_A, STB_B, STB_C, and STB_D control signals determine which latch is written.

The Mother board contains four (4) 8-bit latches (registers). The STB_E, STB_F, STB_G, and STB_H control signals determine which latch is written.

Refer to the corresponding loaboard ***Getting Started*** document for loadboard latch definitions.

Color Coding:
1) The black is present on all revisions
2) The turquoise is new or modified to Octal FVMI Rev F.
3) The grey is present on Octal FVMI Rev E only (not on Rev F).
4) The green is new or modified to Motherboard Rev C.
5) The pink is new or modified to Motherboard Rev D+.

Table 8: EVM Register Mapping Overview

STB	Board	Latch Description
STB_A	Octal FVMI	8-bit DAC & ADC control signals, see Table 9
STB_B	Octal FVMI	8-bit analog mux address bus (ADDR[7:0]), see Section 3.5.1
STB_C	Loadboard	CBit[8:1], refer to loadboard document
STB_D	Octal FVMI	7-bit power amplifier enable (CH[7:1]_ENB) + reserved (Cbit#9)
STB_E	Motherboard	DUT Control, see Table 12
STB_F	Motherboard	Data/En Stream, see Table 13
STB_G	Motherboard	Misc. Control see Table 14
STB_H	Motherboard	PLL Control, see Table 15

Table 9: STB_A (Octal FVMI DAC & ADC Control) Signal Definitions

STB_A Bit	Bit Name	Bit Description
0	SDI_A	DAC Serial Data Input
1	CLK	DAC Clock
2	LDAC	DAC LDAC Input
3	LOADB	DAC LOAD* Input
4	ADCCLK	ADC Clock
5	ADCCS	ADC Chip Select (begin measurement)
6	ADCRANGE	ADC Range Relay Select. 0 = Gain of 200. 1 = Unity Gain.
7	TPINSEL	ADC ATE Input Signal. VINPOS or AOUT. FVMI EEPROM CS

Table 10: STB_B (Octal FVMI AMux Control) Signal Definitions

STB_A Bit	Bit Name	Bit Description
3:0	ADDR_POS	Octal FVMI 4-bit VINPOS AMUX address. See section 3.5.1
7:4	ADDR_NEG	Octal FVMI 4-bit VINNEG AMUX address. See section 3.5.1

Table 11: STB_D (Octal FVMI DPS Supply Enable) Signal Definitions

STB_A Bit	Bit Name	Bit Description
6:0	CH[7:1]_EN	LT1206 Supplies Control. 0=Disable. 1=Enable
0	CH#_EN	LT1206 Supplies Control. 0=Disable. 1=Enable
1	AMUX_POSA	AMUX POS(A). 1=Disable. 0=Enable
2	AMUX_POSB	AMUX POS(B). 1=Disable. 0=Enable
6:3	Unused	
7	CBIT_9	VDD Current Boost. 0=Disable. 1=Enable

Table 12: STB_E (Motherboard Loadboard Control) Signal Definitions

STB_E Bit	Bit Name	Bit Description
0	SCLK	DUT CPU Interface Clock (CK)
1	STB	DUT CPU Interface Strobe (STB)
2	RESET	DUT Reset. Active High
3	TC_21	See Section 3.3
4	TC_26	See Section 3.3
5	CLK_SEL	DUT CPU-CK Source • 0 = 25MHz continuous clock. • 1 = Controlled by PC
6	SDIO_IN	DUT CPU Interface Data Input (SDIO) (PC to DUT)
7	SDIO_EN	DUT SDIO_IN Enable. • 0 = Enable SDIO_IN (PC to DUT) • 1 = Tri-state SDIO_IN (DUT to PC)

Table 13: STB_F (Motherboard Data/En Stream) Signal Definitions

STB_F Bit	Bit Name	Bit Description
0	TC_17	See Section 3.3
1	TC_18	See Section 3.3
2	TC_19	See Section 3.3
3	TC_20	See Section 3.3
4	TC_22	See Section 3.3
5	TC_23	See Section 3.3
6	TC_24	See Section 3.3
7	TC_25	See Section 3.3

Table 14: STB_G (Motherboard Misc. Control) Signal Definitions

STB_G Bit	Bit Name	Bit Description
0	TC_28	See Section 3.3
1	TC_27	See Section 3.3
2	Unused	
3	LB_RBMUX_EN	Loadboard Digital Mux Readback Enable. 0=Disable, 1=Enable Added on MB Revision D3
7:4	ADDR	Motherboard analog mux address. Address lines are swapped.

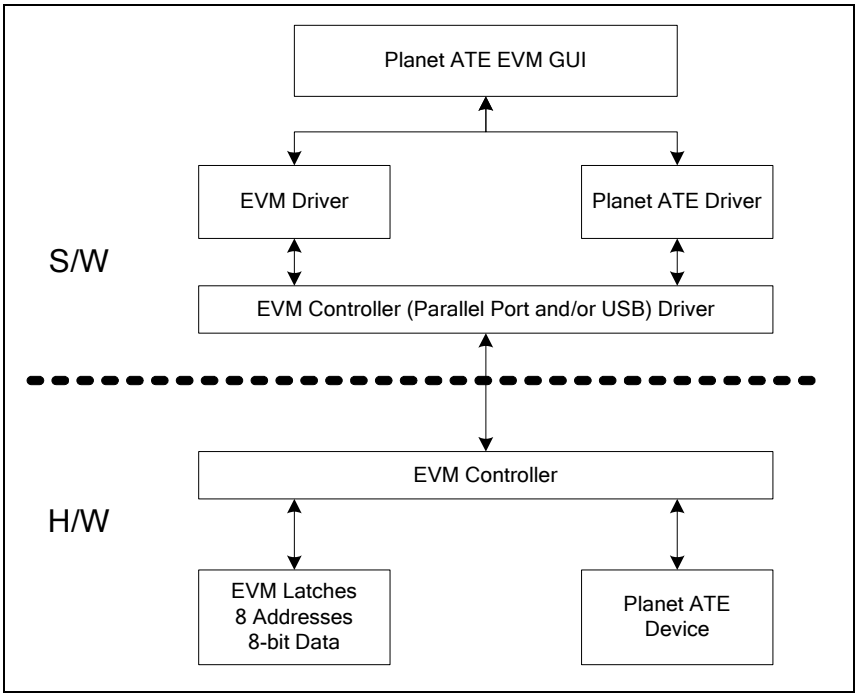
Table 15: STB_H (Motherboard PLL & LB EEPROM Control) Signal Definitions

STB_H Bit	Bit Name	Bit Description
0	PLL_S_CLK	Motherboard PLL S_CLK control signal
1	PLL_S_DATA	Motherboard PLL S_DATA control signal
2	PLL_S_LOAD	Motherboard PLL S_LOAD control signal
3	COMP_IN_EN	Neptune COMP_IN buffer enable
4	LPORT1_OUT2	Loadboard EEPROM chip select
5	LPORT1_OUT3	Loadboard EEPROM clock
6	LPORT1_OUT4	Loadboard EEPROM data in
4	DATA_OUT_EN	Motherboard DATA_OUT to PC buffer enable.

5 Elevate Semiconductor EVM GUI and Software Description

This section provides an overview of the Elevate Semiconductor EVM GUI software. Figure 8 illustrates a high-level software and hardware architect.

Figure 8: Software Architecture Overview



5.1 Elevate Semiconductor EVM GUI Interaction Overview

- More than 1 dialog box can be displayed at a time.
- On entry to a dialog box, the hardware is read to reflect the current values.
- Hardware is only updated when the **Apply** button is selected.
- **Cancel** button will cancel any edited fields since entering the dialog box or when the Apply button was selected.
- **Refresh** button will re-read the hardware and update the GUI. This is useful to undo GUI changes that weren't applied to the hardware.
- In general, the following Control types are used to represent different behaviors:
    - Button – Represent an Action field; i.e. Apply or Cancel
    - Check Box – Represent a Boolean field; i.e. Hold-D0 = enable/disable
    - Combo Box (menu) – Represent a MUX selection; i.e. SEL-DO = DATA0 or DATA1. See section 5.1.1 for more details.
    - Radio Box (menu) – another way to represent a menu (seldom used)
    - Text Box – Represent a double or integer field; i.e. Driver High Level

5.1.1 Combo Box (Menus) Order

The list menus are in sorted in numeric order starting from 0. This implies the first entry will return a 0, the second entry will return a 1, and so on. For example, the DR-MODE menu option is:

Menu Text Order	Value
High-Z	0
VTT	1

One exception to this rule is the R-Out (DVH, DVL, VTT) menus in the **Driver Path Config** dialog box. For these menus, the first entry represents a –8, second entry a –7, and so on. The R-Out register fields are defined as a 4-bit 2's complement number ranging from –8 (-5.0 Ohm) to +7 (+4.375 Ohm).

5.2 EVM Config Menu Dialog Boxes

This section provides an overview the of the EVM Config menu options.

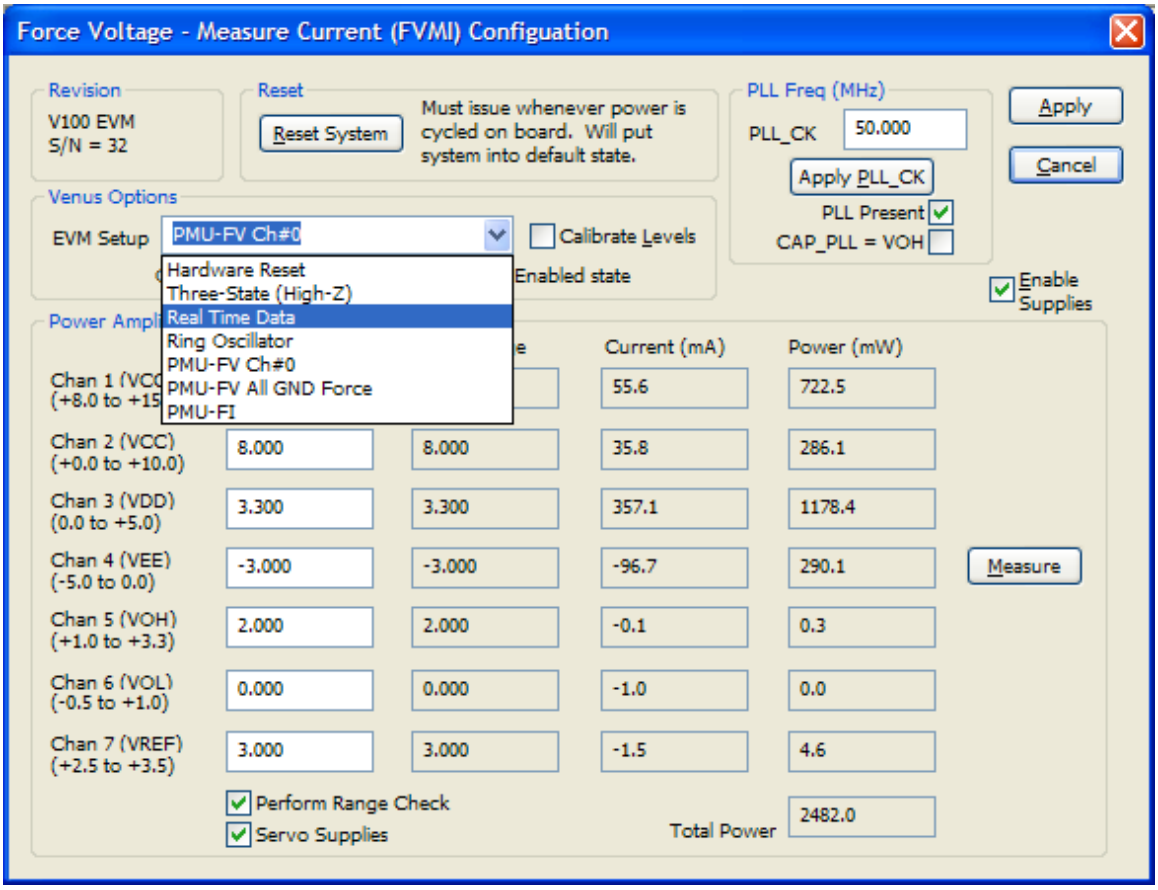
5.2.1 FVMI EVM Config Dialog Box

Figure 9 illustrates the FVMI EVM Config dialog box. This dialog box is used the set the Device supply voltages and configure the system based on the hardware setup.

The **Reset System** will put the EVM and Venus device into the default state. The **Reset System** should be issued whenever the power supply is powered OFF then ON. The **Reset System** is automatically performed when the program is initially launched.

The **Device Options (EVM Setup and Calibrate DAC Levels)** only take effect when the supplies transition to the enabled state.

Figure 9: FVMI EVM Config



5.2.2 FVMI EVM Measure Dialog Box

Figure 10 illustrates the FVMI EVM Measure dialog box.

- The **Chan A** and **Chan B** allows the user to select up to 2 different device channels.
- The **Analog Signals** and **Select VINPOS & VINNEG** groups use the FVMI EVM's on-board 24-bit ADC and analog muxes to measure the various voltage levels. Refer to Section 3.5.1.
- The **Temp. Sensing** group uses the Venus Test & Cal register via the MONITOR pin to measure and calculate the Venus junction temperature.
- The **EVM Comparator States** group uses the Motherboard's analog mux to measure the comparator output states.

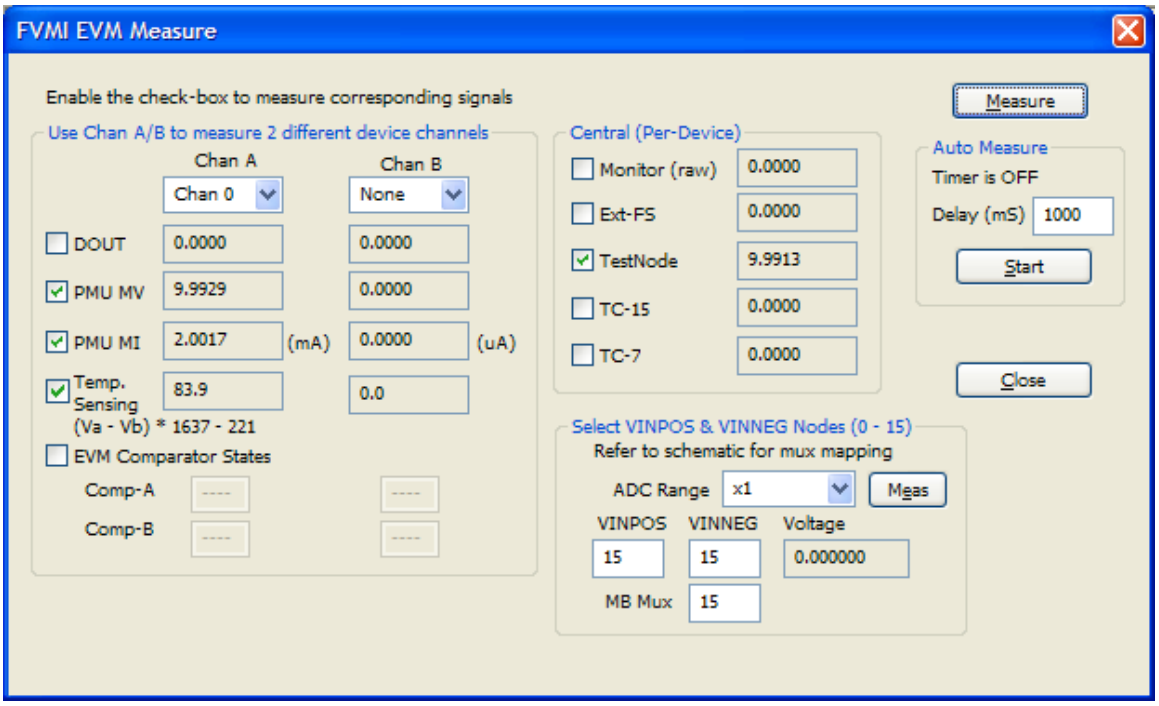
Notes:

1) Some analog signals are only valid if an EVM switch or SMA cable is connected to the desired node.
2) The Comparator States values may get corrupted if the associated comparator is loaded down. The PC's parallel port requires ~1V swings to differentiate between a 0 and 1.
3) The PMU MI (measure current) results are not calibrated.

The **Auto Measure** will continuously measure and update the GUI at the specified interval. The user can still access other dialog boxes but it is not recommended as the program will be sluggish while processing the background tasks.

Use the **Check** boxes to enable the measurement of the specified signal or group.

Figure 10: FVMI EVM Measure



6 Document Revision History

Rev	Date	Description
B01	InProgress	• Add support for USB to Parallel interface board • Add support for Europa
A04	2/7/2006	• Added support for Jupiter R5+, Saturn, and Triton • Update References on Table 18 and 19
A03	1/27/05	• Moved the Loadboard block diagrams and latch defintions to their corresponding ***Getting Started*** Document • Updated for Jupiter EVM support
A02	9/9/04	• Update Mercury block diagram: to match A02 schematic ▪ Redefine TC-32 SMA to be EXT_SENSE SMA ▪ Don't allow switch to connect EXT_SENSE to EXT_FORCE ▪ MONITOR: move A/D to SMA side of switch ▪ Redefine CON_TC16_TN to CON_EF_TN (always Ext-Force to be connected to Test Node) • Move Pluto Diagram to 'Pluto Getting Started' document
A01	9/19/03	Initial Draft. Started from Venus EVM User's Guide and internal EVM Design Document